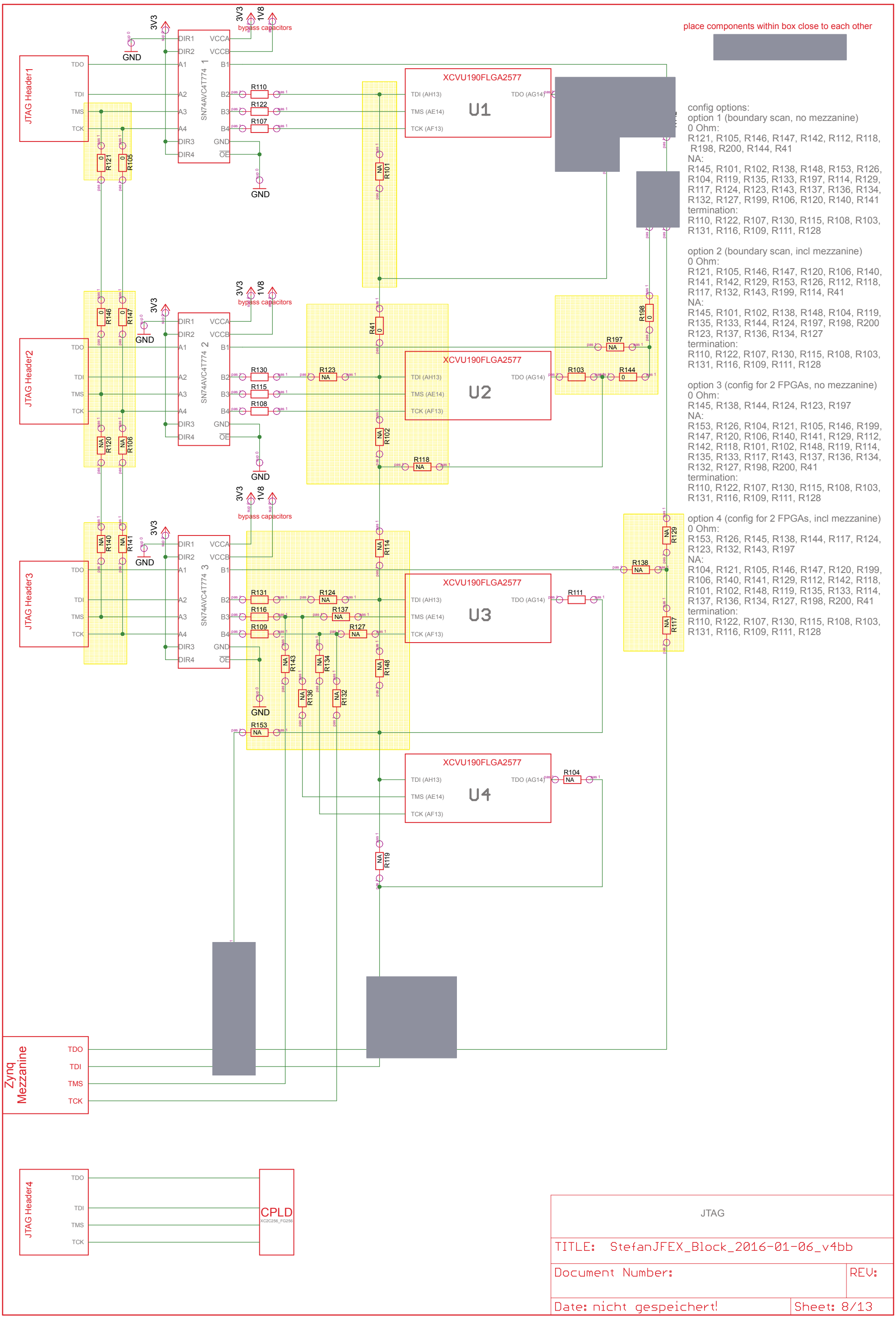
place components within box close to each other
JTAG Header1
JTAG Header2
JTAG Header3
JTAG Header4
Zynq Mezzanine
CPLD
XC2C256_FG256
SN74AVC4T774 1
SN74AVC4T774 2
SN74AVC4T774 3
XCVU190FLGA2577
U1
U2
U3
U4
TDI (AH13)
TMS (AE14)
TCK (AF13)
TDO (AG14)
bypass capacitors
3V3
1V8
GND
config options:
option 1 (boundary scan, no mezzanine)
0 Ohm:
R121, R105, R146, R147, R142, R112, R118, R198, R200, R144, R41
NA:
R145, R101, R102, R138, R148, R153, R126, R104, R119, R135, R133, R197, R114, R129, R117, R124, R123, R143, R137, R136, R134, R132, R127, R199, R106, R120, R140, R141
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 2 (boundary scan, incl mezzanine)
0 Ohm:
R121, R105, R146, R147, R120, R106, R140, R141, R142, R129, R153, R126, R112, R118, R117, R132, R143, R199, R114, R41
NA:
R145, R101, R102, R138, R148, R104, R119, R135, R133, R144, R124, R197, R198, R200 R123, R137, R136, R134, R127
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 3 (config for 2 FPGAs, no mezzanine)
0 Ohm:
R145, R138, R144, R124, R123, R197
NA:
R153, R126, R104, R121, R105, R146, R199, R147, R120, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R114, R135, R133, R117, R143, R137, R136, R134, R132, R127, R198, R200, R41
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 4 (config for 2 FPGAs, incl mezzanine)
0 Ohm:
R153, R126, R145, R138, R144, R117, R124, R123, R132, R143, R197
NA:
R104, R121, R105, R146, R147, R120, R199, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R135, R133, R114, R137, R136, R134, R127, R198, R200, R41
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
JTAG
TITLE: StefanJFEX_Block_2016-01-06_v4bb
Document Number:
REV:
Date: nicht gespeichert!
Sheet: 8/13