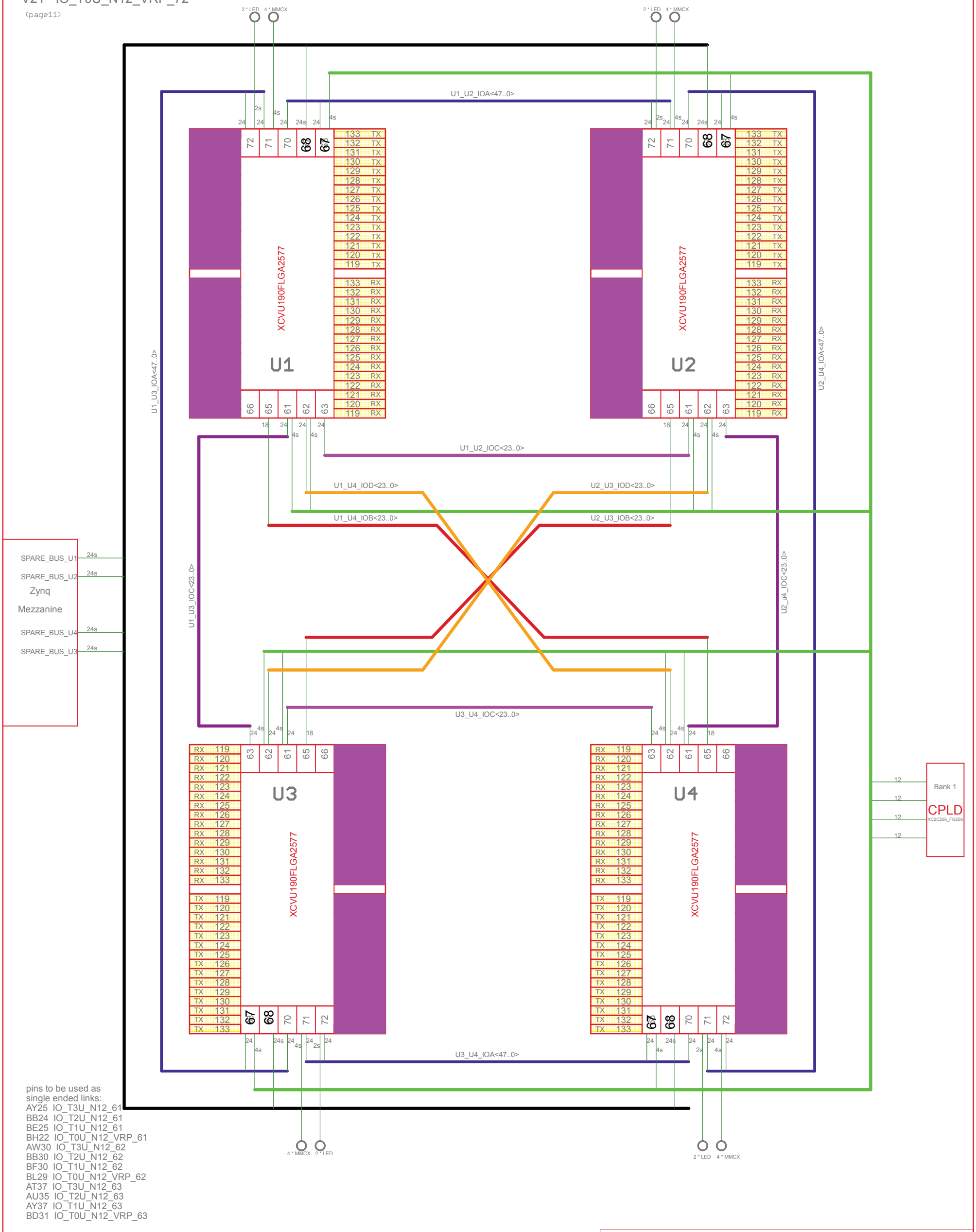
pins used for DCI referenz resistors(240R):
BD31 IO_T0U_N12_VRP_63
BD21 IO_T0U_N12_VRP_A28_65
V21 IO_T0U_N12_VRP_72



pins to be used as
single ended links:
AY25 IO_T3U_N12_61
BB24 IO_T2U_N12_61
BE25 IO_T1U_N12_61
BH22 IO_T0U_N12_VRP_61
AW30 IO_T3U_N12_62
BB30 IO_T2U_N12_62
BF30 IO_T1U_N12_62
BL29 IO_T0U_N12_VRP_62
AT37 IO_T3U_N12_63
AU35 IO_T2U_N12_63
AY37 IO_T1U_N12_63
BD31 IO_T0U_N12_VRP_63

connect complete banks
swapping of complete banks allowed
swapping within banks allowed
if possible swap identically for all FPGAs
if possible do not connect GC pins to GC pins
connection of banks within busses:
bank 67 to 71
bank 70 to 72

Bank 68 (XCVU190) single-ended pins on :
IO_L(1-12)P/N 24 single

Bank 65 (XCVU190) differential pairs on :
IO_L1P/N, IO_L(3-19)P/N 18 diff

PARALLEL I/0

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Document Number:

REV:

Date: 02.03.2016 13:11:54

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