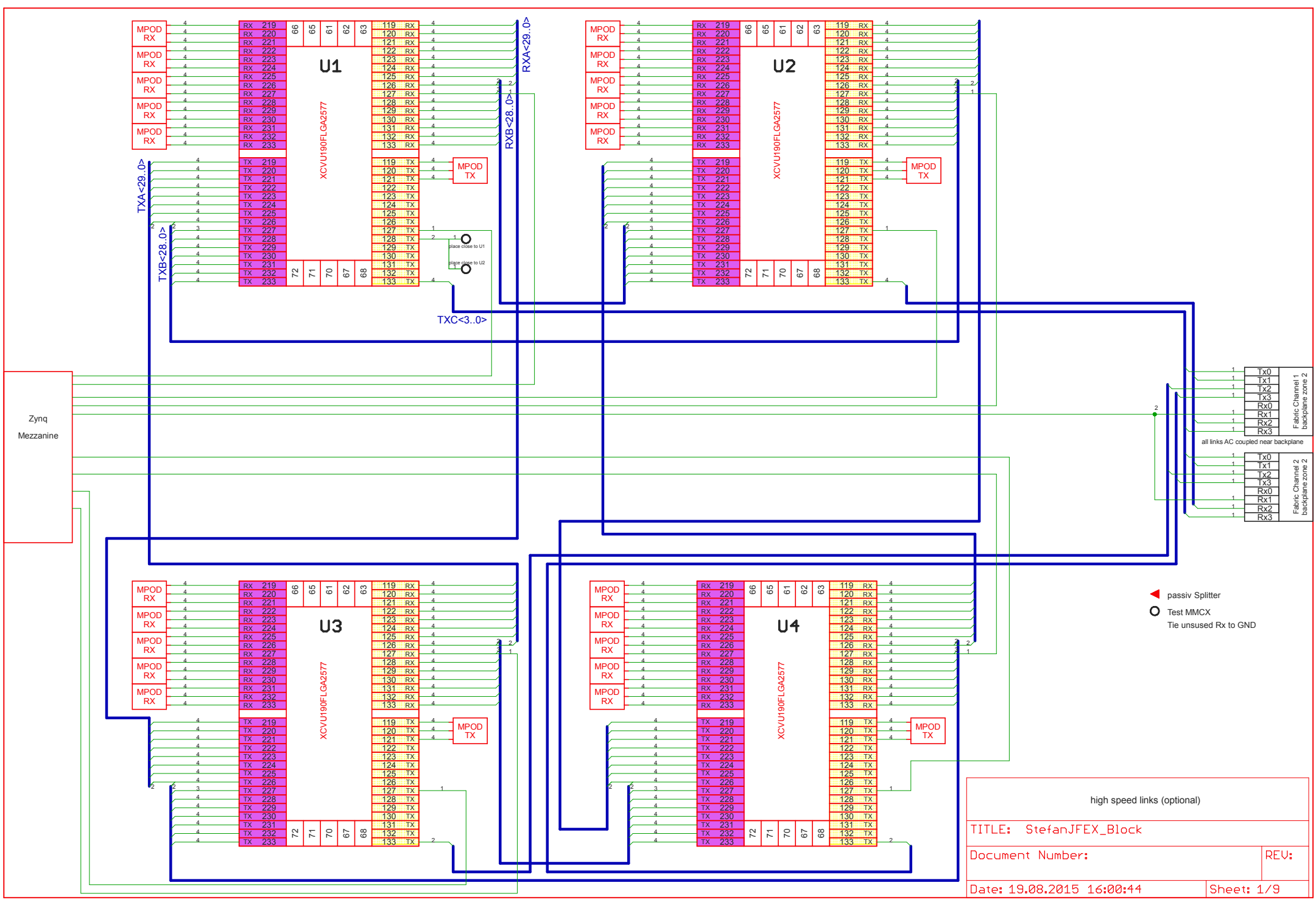
U1
U2
U3
U4
XCVU190FLGA2577
MPOD RX
MPOD TX
RXA<29..0>
RXB<28..0>
TXA<29..0>
TXB<28..0>
TXC<3..0>
place close to U1
place close to U2
Zynq
Mezzanine
Tx0
Tx1
Tx2
Tx3
Rx0
Rx1
Rx2
Rx3
Fabric Channel 1 backplane zone 2
Fabric Channel 2 backplane zone 2
all links AC coupled near backplane
passiv Splitter
Test MMCX
Tie unused Rx to GND
high speed links (optional)
TITLE: StefanJFEX_Block
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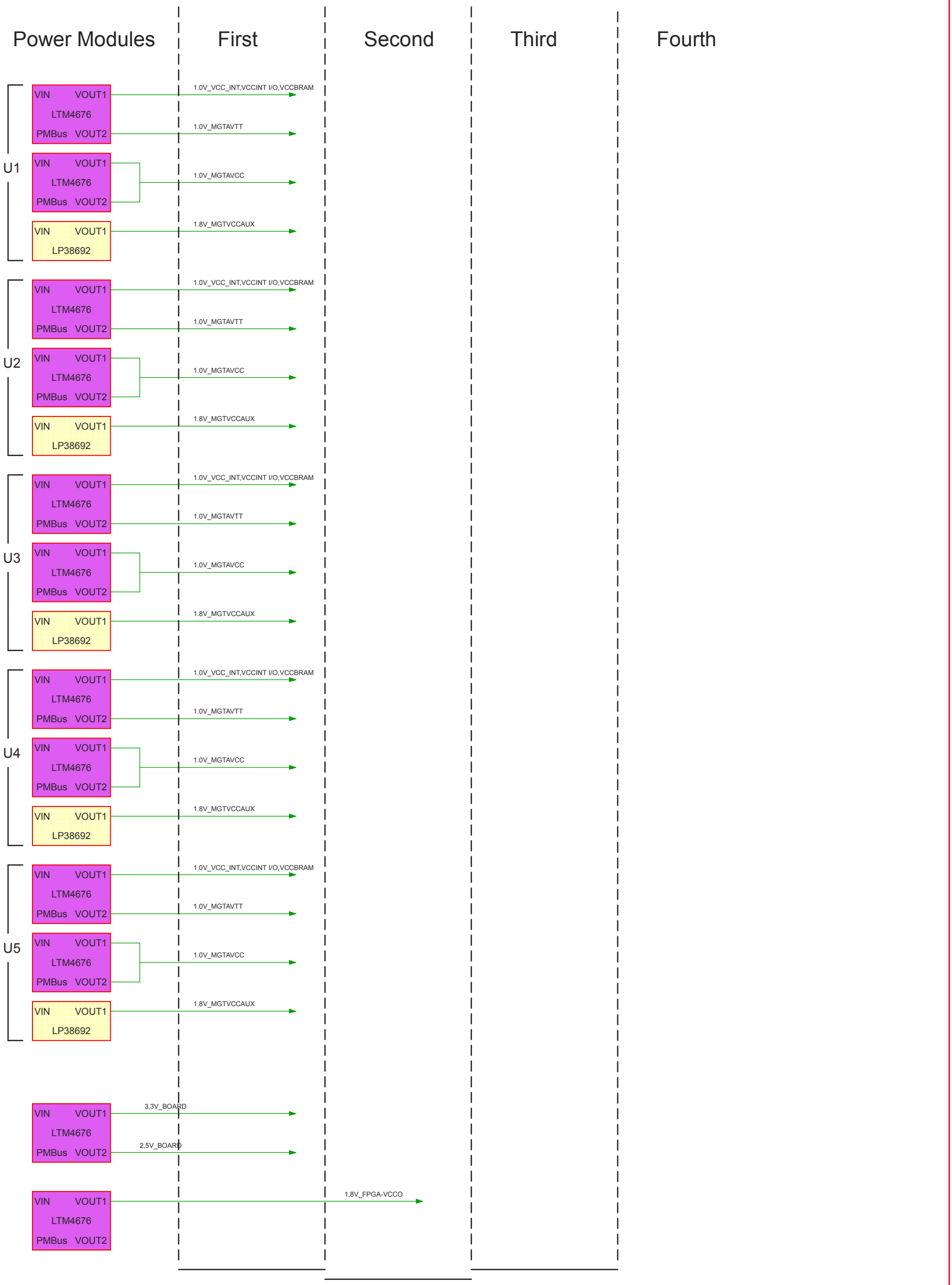

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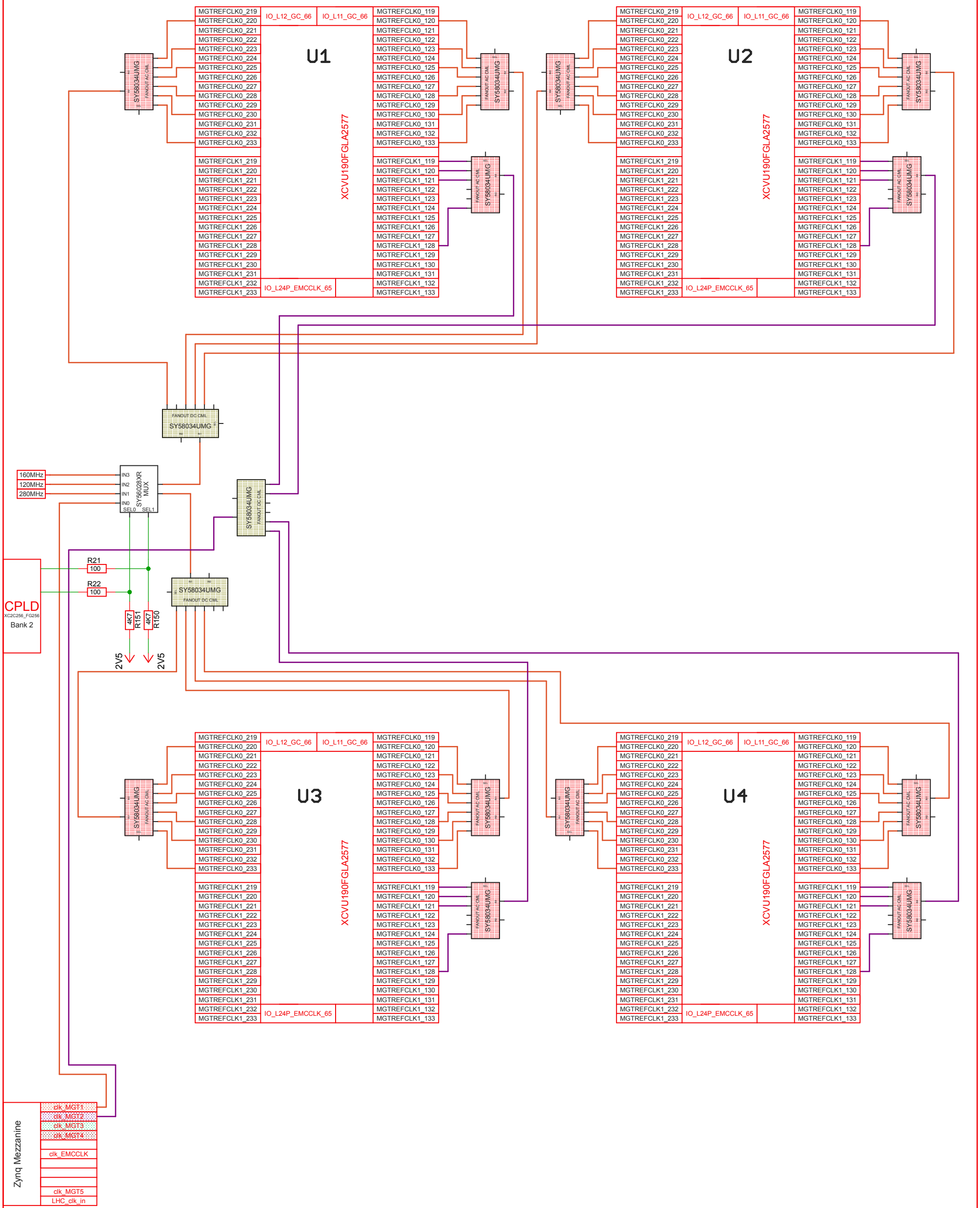
U1
U2
U3
U4
XCVU190FGLA2577
MGTREFCLK0_219
MGTREFCLK0_220
MGTREFCLK0_221
MGTREFCLK0_222
MGTREFCLK0_223
MGTREFCLK0_224
MGTREFCLK0_225
MGTREFCLK0_226
MGTREFCLK0_227
MGTREFCLK0_228
MGTREFCLK0_229
MGTREFCLK0_230
MGTREFCLK0_231
MGTREFCLK0_232
MGTREFCLK0_233
MGTREFCLK1_219
MGTREFCLK1_220
MGTREFCLK1_221
MGTREFCLK1_222
MGTREFCLK1_223
MGTREFCLK1_224
MGTREFCLK1_225
MGTREFCLK1_226
MGTREFCLK1_227
MGTREFCLK1_228
MGTREFCLK1_229
MGTREFCLK1_230
MGTREFCLK1_231
MGTREFCLK1_232
MGTREFCLK1_233
IO_L12_GC_66
IO_L11_GC_66
IO_L24P_EMCCLK_65
MGTREFCLK0_119
MGTREFCLK0_120
MGTREFCLK0_121
MGTREFCLK0_122
MGTREFCLK0_123
MGTREFCLK0_124
MGTREFCLK0_125
MGTREFCLK0_126
MGTREFCLK0_127
MGTREFCLK0_128
MGTREFCLK0_129
MGTREFCLK0_130
MGTREFCLK0_131
MGTREFCLK0_132
MGTREFCLK0_133
MGTREFCLK1_119
MGTREFCLK1_120
MGTREFCLK1_121
MGTREFCLK1_122
MGTREFCLK1_123
MGTREFCLK1_124
MGTREFCLK1_125
MGTREFCLK1_126
MGTREFCLK1_127
MGTREFCLK1_128
MGTREFCLK1_129
MGTREFCLK1_130
MGTREFCLK1_131
MGTREFCLK1_132
MGTREFCLK1_133
SY58034UMG
FANOUT AC CML
FANOUT DC CML
SY56028XR
MUX
IN3
IN2
IN1
IN0
SEL0
SEL1
160MHz
120MHz
280MHz
CPLD
XC2C256_FG256
Bank 2
R21
100
R22
100
4K7
R151
4K7
R150
2V5
2V5
Zynq Mezzanine
clk_MGT1
clk_MGT2
clk_MGT3
clk_MGT4
clk_EMCCLK
clk_MGT5
LHC_clk_in
MGT1 + MGT2 CLOCK
TITLE: StefanJFEX_Block
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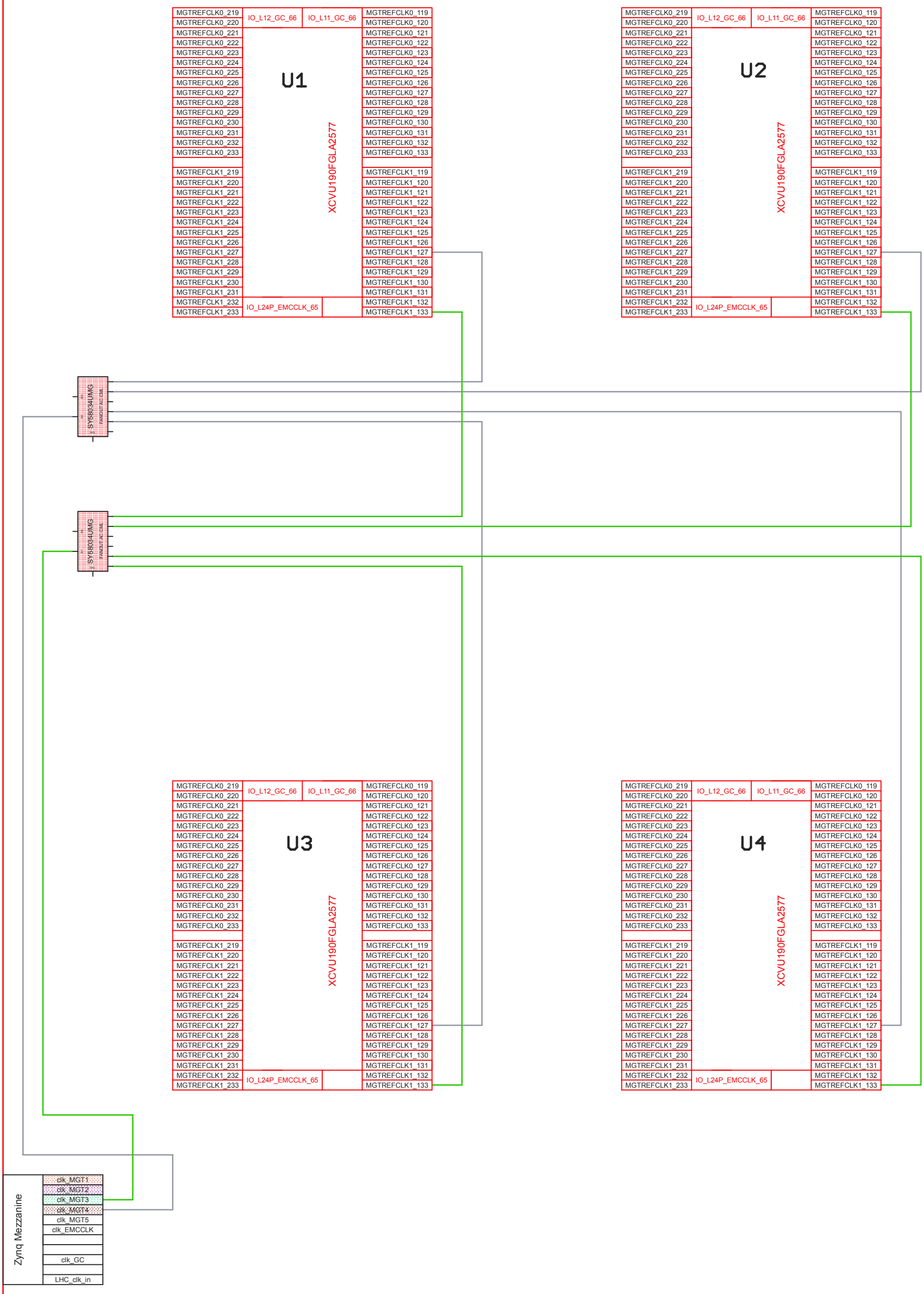
U1
XCVU190FGLA2577
MGTREFCLK0_219
MGTREFCLK0_220
MGTREFCLK0_221
MGTREFCLK0_222
MGTREFCLK0_223
MGTREFCLK0_224
MGTREFCLK0_225
MGTREFCLK0_226
MGTREFCLK0_227
MGTREFCLK0_228
MGTREFCLK0_229
MGTREFCLK0_230
MGTREFCLK0_231
MGTREFCLK0_232
MGTREFCLK0_233
MGTREFCLK1_219
MGTREFCLK1_220
MGTREFCLK1_221
MGTREFCLK1_222
MGTREFCLK1_223
MGTREFCLK1_224
MGTREFCLK1_225
MGTREFCLK1_226
MGTREFCLK1_227
MGTREFCLK1_228
MGTREFCLK1_229
MGTREFCLK1_230
MGTREFCLK1_231
MGTREFCLK1_232
MGTREFCLK1_233
IO_L12_GC_66
IO_L11_GC_66
IO_L24P_EMCCLK_65
MGTREFCLK0_119
MGTREFCLK0_120
MGTREFCLK0_121
MGTREFCLK0_122
MGTREFCLK0_123
MGTREFCLK0_124
MGTREFCLK0_125
MGTREFCLK0_126
MGTREFCLK0_127
MGTREFCLK0_128
MGTREFCLK0_129
MGTREFCLK0_130
MGTREFCLK0_131
MGTREFCLK0_132
MGTREFCLK0_133
MGTREFCLK1_119
MGTREFCLK1_120
MGTREFCLK1_121
MGTREFCLK1_122
MGTREFCLK1_123
MGTREFCLK1_124
MGTREFCLK1_125
MGTREFCLK1_126
MGTREFCLK1_127
MGTREFCLK1_128
MGTREFCLK1_129
MGTREFCLK1_130
MGTREFCLK1_131
MGTREFCLK1_132
MGTREFCLK1_133
U2
U3
U4
SY58034UMG
Zynq Mezzanine
clk_MGT1
clk_MGT2
clk_MGT3
clk_MGT4
clk_MGT5
clk_EMCCLK
clk_GC
LHC_clk_in
MGT3 + MGT4 +IPBUS CLOCK
TITLE: StefanJFEX_Block
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Front Panel mezzanine

XCVU190FGLA2577

MGTREFCLK0_219 … MGTREFCLK0_233
MGTREFCLK1_219 … MGTREFCLK1_233
IO_L12P/N_GC_66 | IO_L11P/N_GC_66 | IO_T3U_N12_70
IO_L24P_65 | IO_L12P/N_GC_68 | IO_T3U_N12_70

100 — place closely — CMOS / LVDS

out — in — CMOS / LVDS — out

Zynq Mezzanine

clk_MGT1
clk_MGT2
clk_MGT3
clk_MGT4
clk_MGT5
clk_EMCCLK (5)
clk_GC (4)
LHC_clk_in

CMOS / LVDS

CPLD
XC2C256_FG256

2V5
R154 4K7
R149 4K7
100 R24
100 R23

SY89832U

LVDS

unused output terminated with 100 Ohm across the diff pair sy89832u.pdf, page 3

MUX SY89540UMG

CML

default (1,1): IN3

unused output terminated with 100 Ohm across the diff pair sy89546u.pdf, page 4 place close to backplane

CML AC coupled

Tx0 Tx1 Tx2 Tx3 Rx0 Rx1 Rx2 Rx3

Fabric Channel 1 backplane zone 2

Fabric Channel 2 backplane zone 2

LVPECL — 40MHz

GLOBAL CLOCK

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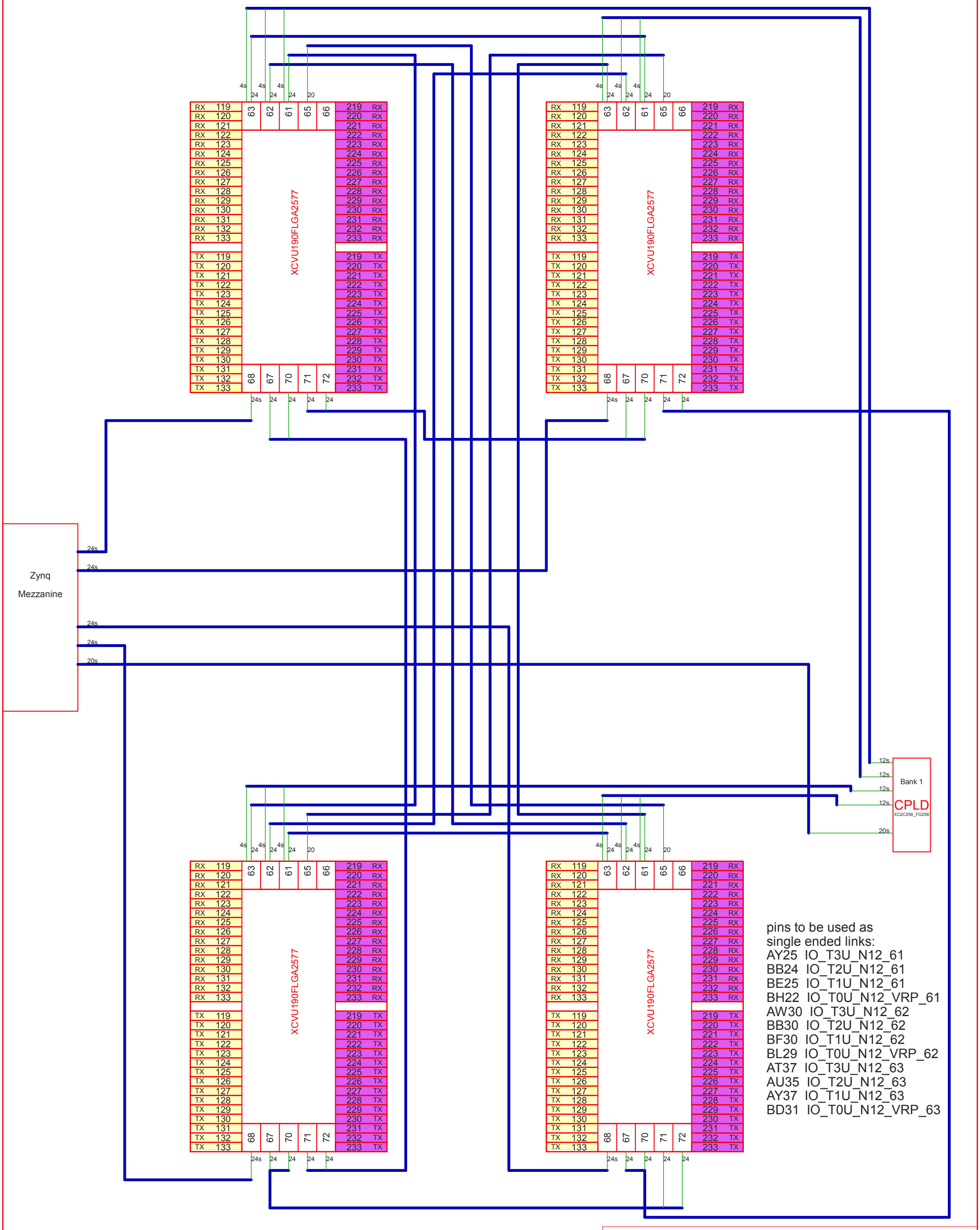

Bank 68 (XCVU190) single-ended pins on :
IO_L(1-11)P/N 22 single

Bank 65 (XCVU095) 32 single-ended pins on :
IO_L[1,3-10,14-19]P/N, IO_T1,IO_T3

Bank 65 (XCVU190) differential pairs on :
IO_L1P/N, IO_L(3-20)P/N 19 diff

PARALLEL I/0

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Front Panel mezzanine

Zynq Mezzanine

U1 U2 U3 U4 U5 — 20s

XCVU190FLGA2577

Bank 65

EMCCLK (BD16)
CSI_B (AV18)
CSO_B (BD15)
D04 (BD18)
D05 (BD17)
FCS2_B (BA22)
D06 (BB17)
D07 (BC17)

Bank 0

CFGBVS
PUDC_B (M14)
M2 (V14)
M1 (Y14)
M0 (AB14)
PROGRAM_B (AK14)
POR_OVERRIDE (AC13)
D00_MOSI (AY14)
D01_DIN (AV14)
RDWR_FCS_B (AM14)
D02 (AT14)
D03 (AP14)
CCLK (AD13)
INIT_B
DONE

VCC GND VCCIO VCCINT 3V3

R6 R1 R2 R38 R37 R48 R47 R26 R36 R35 R12 R13 R14 R50 R49 R27 R34 R33 R15 R16 R17 R32 R31 R18 R19 R20 R46 R45 R29 R44 R43 R28 — 1K, NC, 4k7, 4.7k, 330, 100

LED1 LED2 LED4 LED5 — D G S

CONFIG

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place components closly together if possible

config options:

option 1 (boundary scan, no mezzanine)
0 Ohm:
R121, R105, R146, R147, R142, R112, R118, R198, R200, R144
NA:
R145, R101, R102, R138, R148, R153, R126, R104, R119, R135, R133, R197, R114, R129, R117, R124, R123, R143, R137, R136, R134, R132, R127, R199, R106, R120, R140, R141
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128

option 2 (boundary scan, incl mezzanine)
0 Ohm:
R121, R105, R146, R147, R120, R106, R140, R141, R142, R129, R153, R126, R112, R118, R117, R132, R143, R199, R114
NA:
R145, R101, R102, R138, R148, R104, R119, R135, R133, R144, R124, R197, R198, R200 R123, R137, R136, R134, R127
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128

option 3 (config for 2 FPGAs, no mezzanine)
0 Ohm:
R145, R138, R144, R124, R123, R197
NA:
R153, R126, R104, R121, R105, R146, R199, R147, R120, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R114, R135, R133, R117, R143, R137, R136, R134, R132, R127, R198, R200
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128

option 4 (config for 2 FPGAs, incl mezzanine)
0 Ohm:
R153, R126, R145, R138, R144, R117, R124, R123, R132, R143, R197
NA:
R104, R121, R105, R146, R147, R120, R199, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R135, R133, R114, R137, R136, R134, R127, R198, R200
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128

JTAG	
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Backplane
Magnetics
Jumper
RJ45 Frontpanel
insert resistors?
Zynq mezzanine
IPMC Frontpanel
12
I2C
3
IPMC
Power On
A_OK
B_OK
Frontpanel?
3V3_up
Power Reset
ATCA_Switch
ATCA Power Supply
Header
I2C
LTC2991
DXP (AK18) DXN (AK17) U1
DXP (AK18) DXN (AK17) U2
DXP (AK18) DXN (AK17) U3
DXP (AK18) DXN (AK17) U4
LTC2991
Thermal sensor diode
Thermal sensor diode
Thermal sensor diode
Thermal sensor diode
BOARD TEMP
10
I2C_AV1
Jumper
USB Header
I2C_AV2
Jumper
USB Header
I2C_AV3
Jumper
USB Header
INTL/RES AVR1
INTL/RES AVR2
INTL/RES AVR3
INTL/RES AVR4
INTL/RES AVR5
INTL/RES AVR6
INTL/RES AVR7
INTL/RES AVR8
INTL/RES AVR9
INTL/RES AVR10
INTL/RES AVR11
INTL/RES AVR12
INTL/RES AVR13
INTL/RES AVR14
INTL/RES AVR15
INTL/RES AVR16
INTL/RES AVR17
INTL/RES AVR18
INTL/RES AVR19
INTL/RES AVR20
INTL/RES AVT1
INTL/RES AVT2
INTL/RES AVT3
INTL/RES AVT4
16
16
16
CPLD
XC2C256_FG256
Bank 2
Zynq
Mezzanine
10
PowerSupply chain 2
I2C_PS1
Jumper
USB Header
PowerSupply chain 1
I2C_PS2
Jumper
USB Header

I2C, IPMC, some more

TITLE: StefanJFEX_Block

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