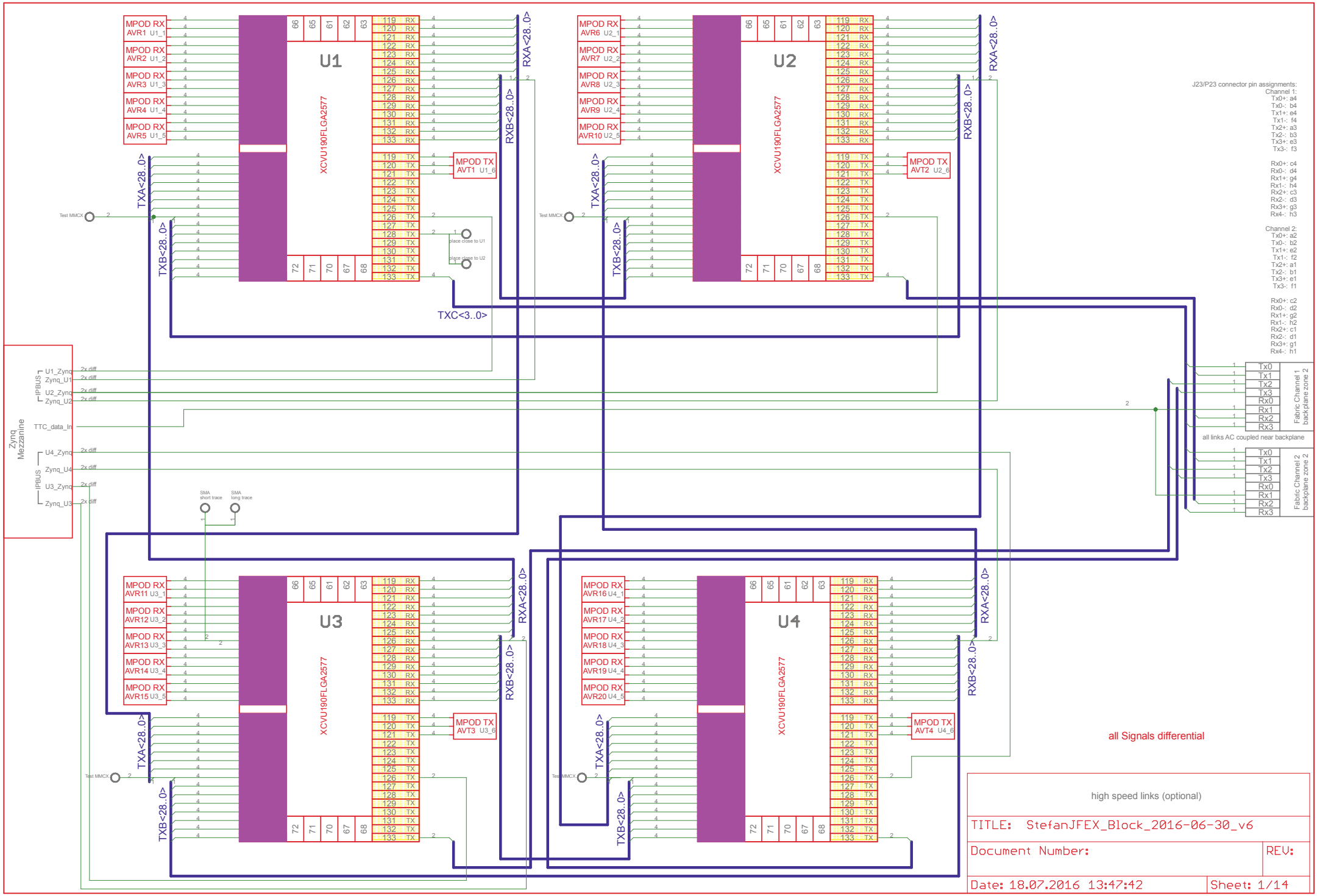
U1
XCVU190FLGA2577
MPOD RX AVR1 U1_1
MPOD RX AVR2 U1_2
MPOD RX AVR3 U1_3
MPOD RX AVR4 U1_4
MPOD RX AVR5 U1_5
MPOD TX AVT1 U1_6
U2
XCVU190FLGA2577
MPOD RX AVR6 U2_1
MPOD RX AVR7 U2_2
MPOD RX AVR8 U2_3
MPOD RX AVR9 U2_4
MPOD RX AVR10 U2_5
MPOD TX AVT2 U2_6
U3
XCVU190FLGA2577
MPOD RX AVR11 U3_1
MPOD RX AVR12 U3_2
MPOD RX AVR13 U3_3
MPOD RX AVR14 U3_4
MPOD RX AVR15 U3_5
MPOD TX AVT3 U3_6
U4
XCVU190FLGA2577
MPOD RX AVR16 U4_1
MPOD RX AVR17 U4_2
MPOD RX AVR18 U4_3
MPOD RX AVR19 U4_4
MPOD RX AVR20 U4_5
MPOD TX AVT4 U4_6
RXA<28..0>
RXB<28..0>
TXA<28..0>
TXB<28..0>
TXC<3..0>
Test MMCX
place close to U1
place close to U2
Zynq Mezzanine
IPBUS
U1_Zynq
Zynq_U1
U2_Zynq
Zynq_U2
TTC_data_In
U4_Zynq
Zynq_U4
U3_Zynq
Zynq_U3
2x diff
SMA short trace
SMA long trace
J23/P23 connector pin assignments:
Channel 1:
Tx0+: a4
Tx0-: b4
Tx1+: e4
Tx1-: f4
Tx2+: a3
Tx2-: b3
Tx3+: e3
Tx3-: f3
Rx0+: c4
Rx0-: d4
Rx1+: g4
Rx1-: h4
Rx2+: c3
Rx2-: d3
Rx3+: g3
Rx4-: h3
Channel 2:
Tx0+: a2
Tx0-: b2
Tx1+: e2
Tx1-: f2
Tx2+: a1
Tx2-: b1
Tx3+: e1
Tx3-: f1
Rx0+: c2
Rx0-: d2
Rx1+: g2
Rx1-: h2
Rx2+: c1
Rx2-: d1
Rx3+: g1
Rx4-: h1
Tx0
Tx1
Tx2
Tx3
Rx0
Rx1
Rx2
Rx3
Fabric Channel 1 backplane zone 2
Fabric Channel 2 backplane zone 2
all links AC coupled near backplane
all Signals differential
high speed links (optional)
TITLE: StefanJFEX_Block_2016-06-30_v6
Document Number:
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Date: 18.07.2016 13:47:42
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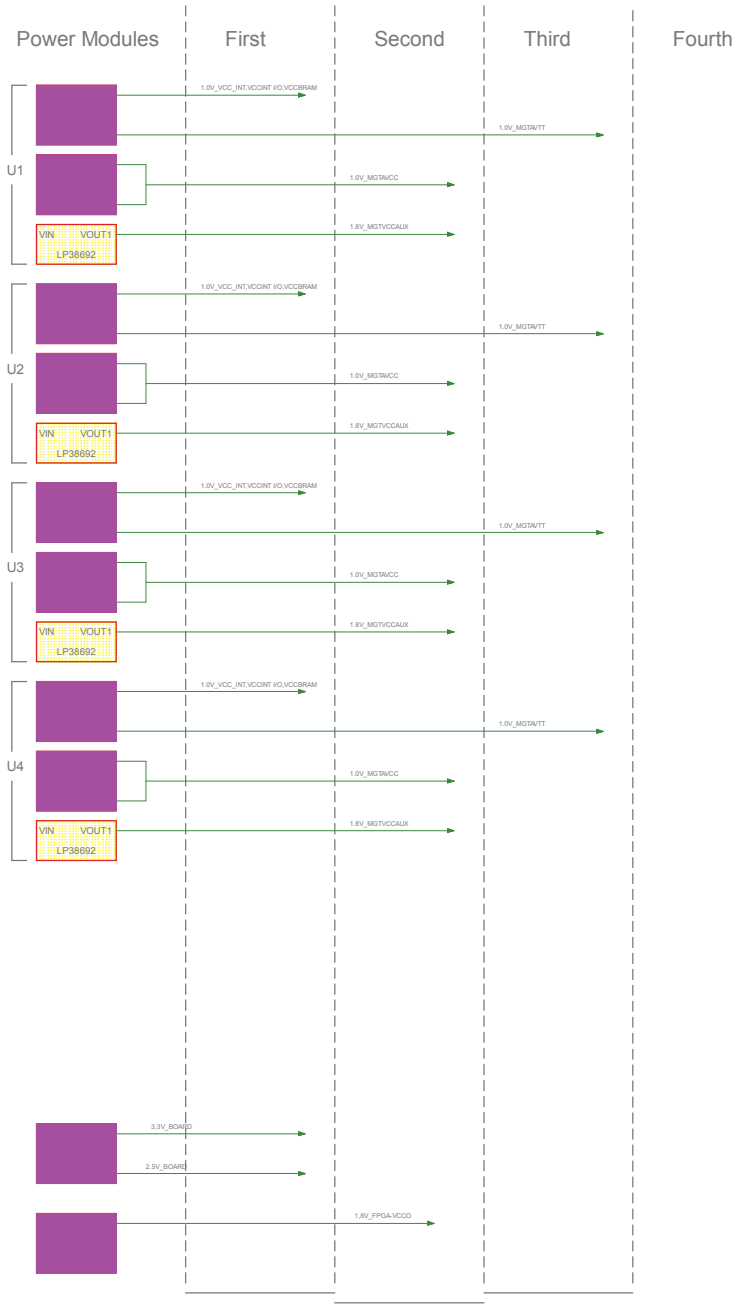
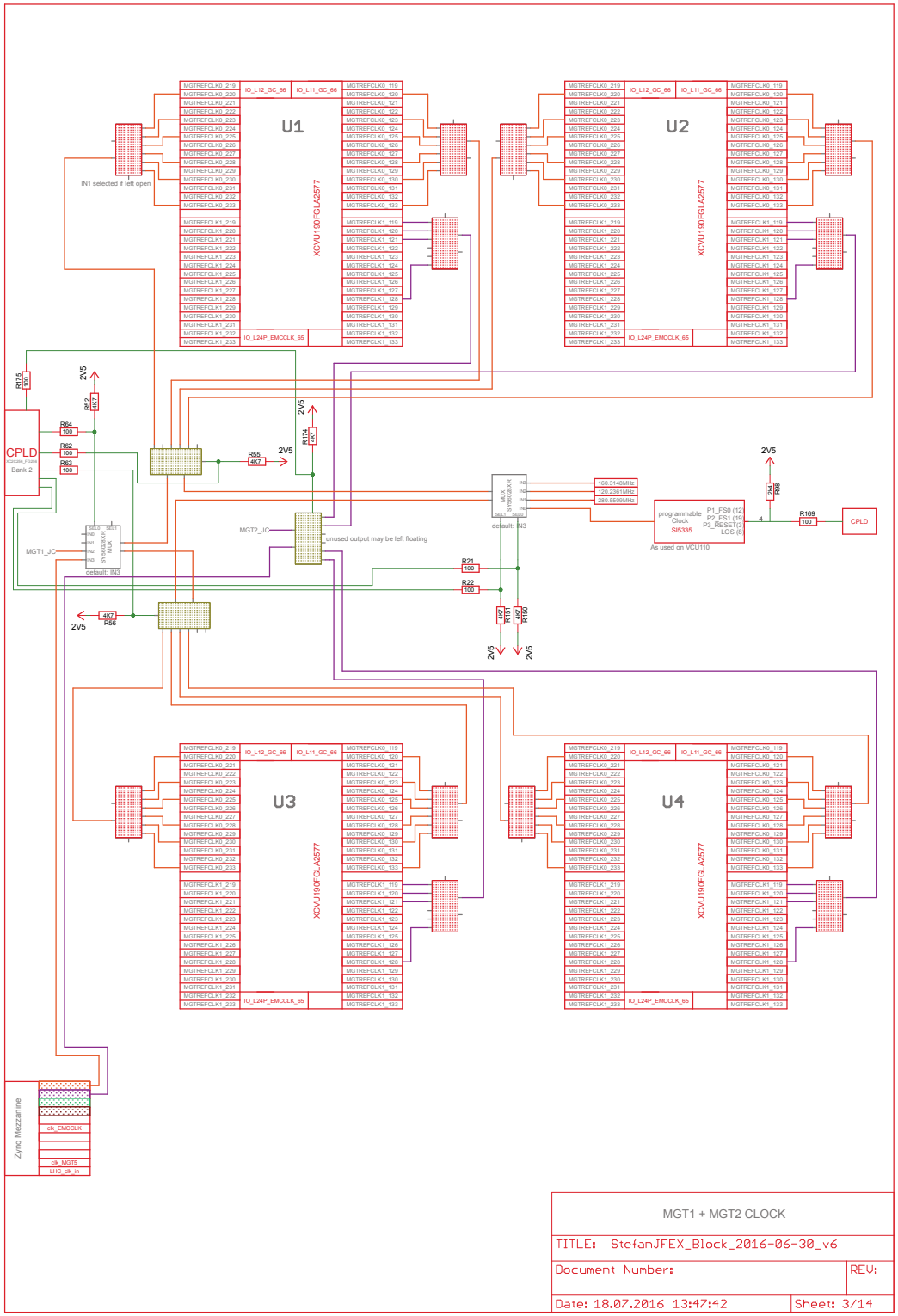
Ramping time for all power supplies: 0.2 ms < T < 40 ms



TITLE: StefanJFEX_Block_2016-06-30_v6	
Document Number:	REV:
Date: 18.07.2016 13:47:42	Sheet: 2/14


U1
U2
U3
U4
XCVU190FLGA2577
IN1 selected if left open
CPLD
Bank 2
MGT1_JC
MGT2_JC
unused output may be left floating
default: IN3
2V5
programmable Clock
SI5335
As used on VCU110
160.3148MHz
120.2381MHz
280.5509MHz
Zynq Mezzanine
clk_EMCCLK
clk_MGT5
LHC_clk_in
MGT1 + MGT2 CLOCK
TITLE: StefanJFEX_Block_2016-06-30_v6
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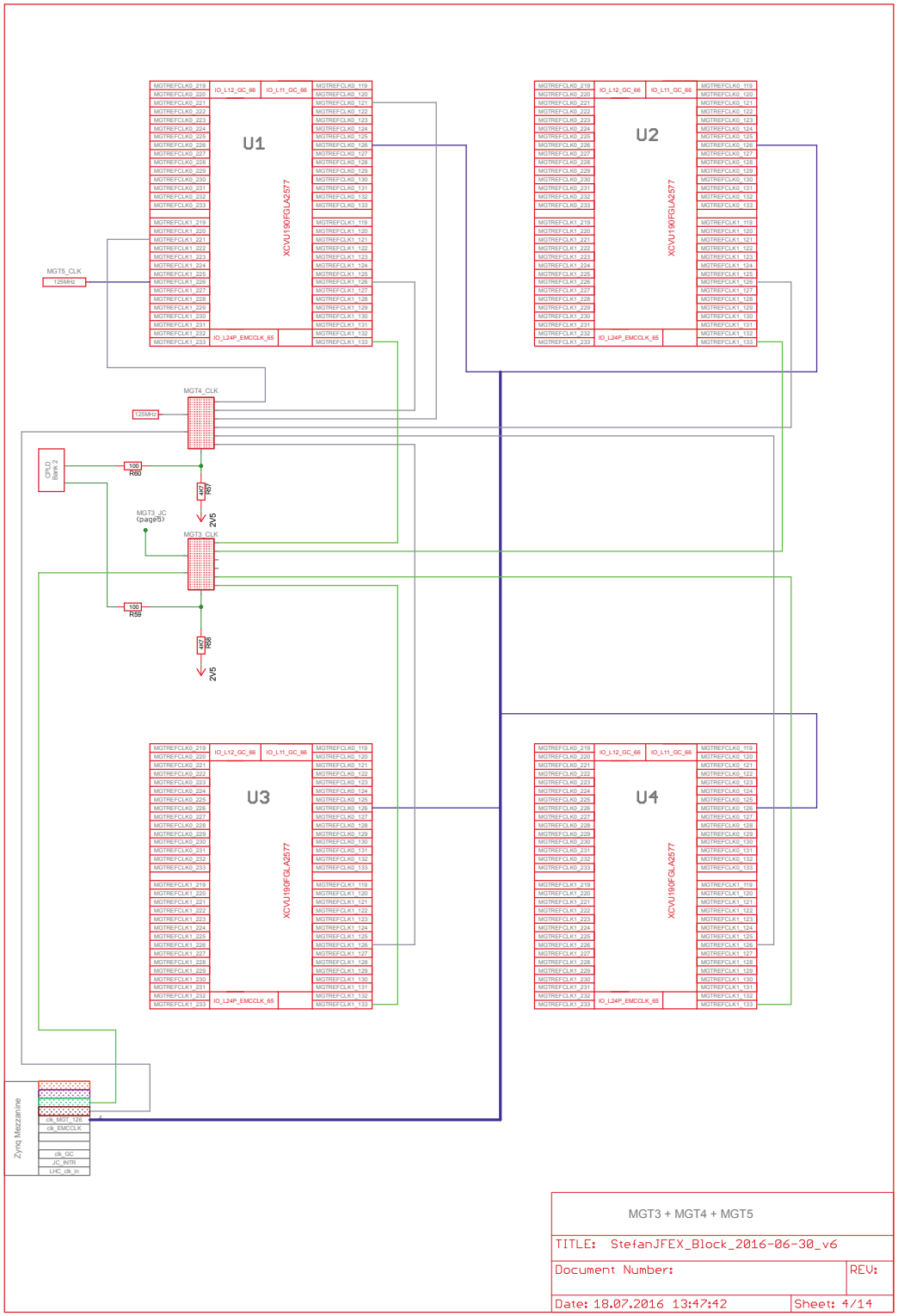
U1
U2
U3
U4
XCVU190FGLA2577
MGT5_CLK
125MHz
MGT4_CLK
MGT3_CLK
MGT3_JC
(page5)
CFG_D
Bank 2
100
R60
R59
4K7
R57
R58
2V5
Zynq Mezzanine
clk_MGT_125
clk_EMCCLK
clk_GC
JC_INTR
LHC_clk_in
MGT3 + MGT4 + MGT5
TITLE: StefanJFEX_Block_2016-06-30_v6
Document Number:
REV:
Date: 18.07.2016 13:47:42
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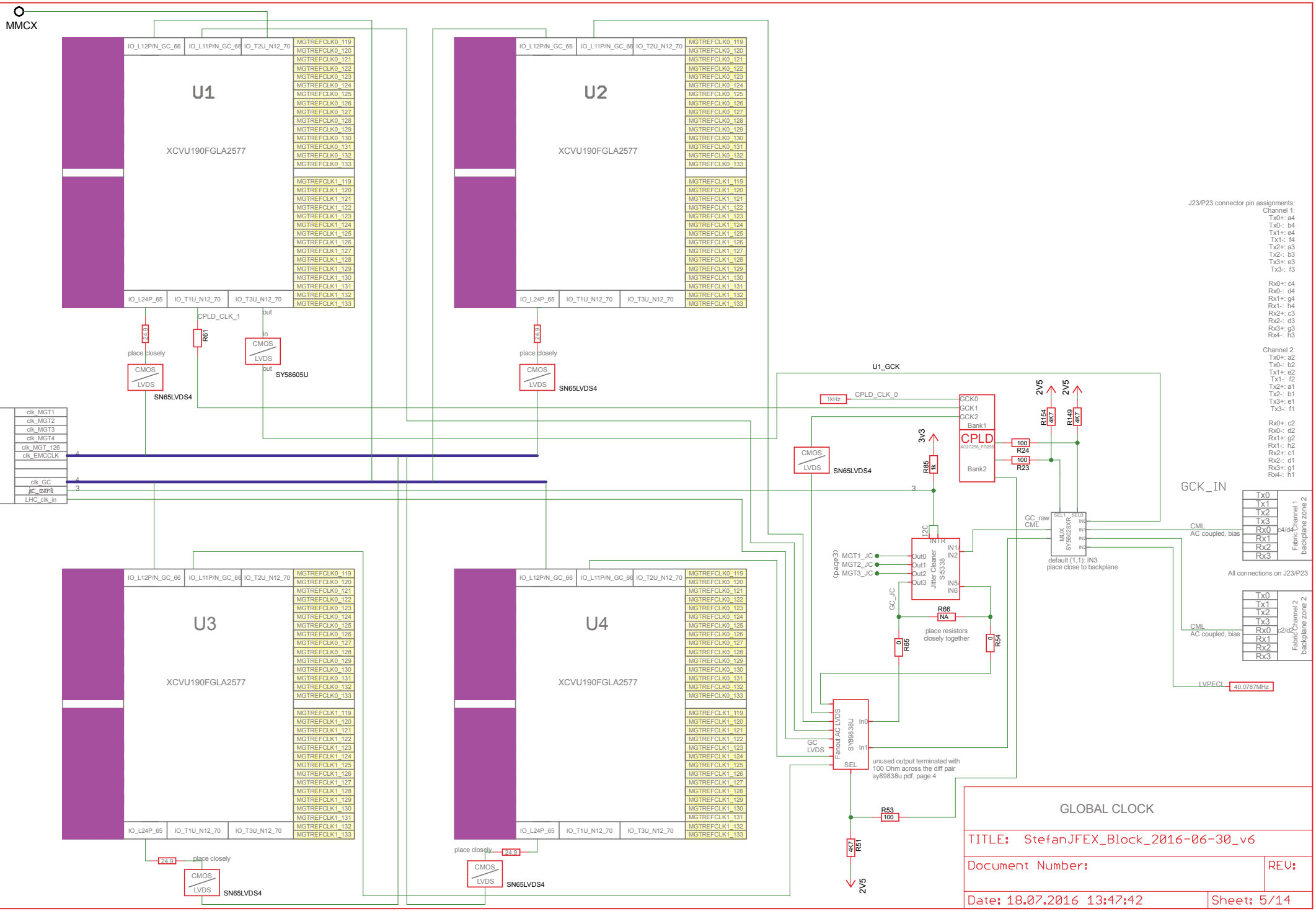
MMCX
U1
XCVU190FGLA2577
U2
XCVU190FGLA2577
U3
XCVU190FGLA2577
U4
XCVU190FGLA2577
CPLD_CLK_1
SN65LVDS4
SY58605U
U1_GCK
CPLD_CLK_0
CPLD
Bank1
Bank2
3v3
2V5
GCK_IN
Zynq Mezzanine
clk_MGT1
clk_MGT2
clk_MGT3
clk_MGT4
clk_MGT_126
clk_EMCCLK
clk_GC
LHC_clk_in
Jitter Cleaner SI5338
MGT1_JC
MGT2_JC
MGT3_JC
GC_JC
GC_raw
CML
AC coupled, bias
default (1,1): IN3
place close to backplane
All connections on J23/P23
Fabric Channel 1 backplane zone 2
Fabric Channel 2 backplane zone 2
LVPECL
40.0787MHz
Fanout AC LVDS
SY89838U
GC LVDS
unused output terminated with 100 Ohm across the diff pair
sy89838u.pdf, page 4
place resistors closely together
place closely
J23/P23 connector pin assignments:
Channel 1:
Tx0+: a4
Tx0-: b4
Tx1+: e4
Tx1-: f4
Tx2+: a3
Tx2-: b3
Tx3+: e3
Tx3-: f3
Rx0+: c4
Rx0-: d4
Rx1+: g4
Rx1-: h4
Rx2+: c3
Rx2-: d3
Rx3+: g3
Rx4-: h3
Channel 2:
Tx0+: a2
Tx0-: b2
Tx1+: e2
Tx1-: f2
Tx2+: a1
Tx2-: b1
Tx3+: e1
Tx3-: f1
Rx0+: c2
Rx0-: d2
Rx1+: g2
Rx1-: h2
Rx2+: c1
Rx2-: d1
Rx3+: g1
Rx4-: h1
GLOBAL CLOCK
TITLE: StefanJFEX_Block_2016-06-30_v6
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Date: 18.07.2016 13:47:42
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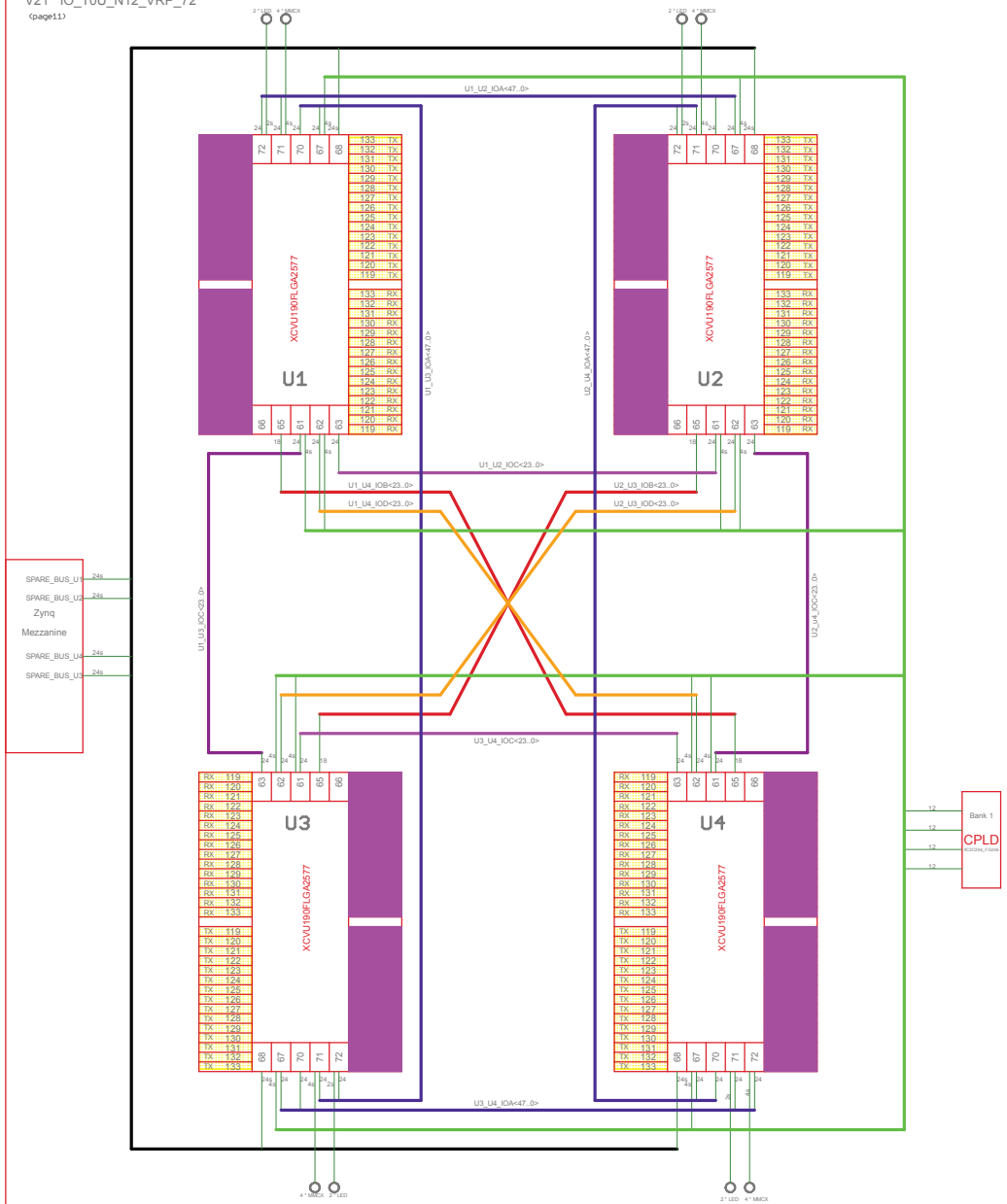
pins used for DCI referenz resistors(240R):
BD31 IO_T0U_N12_VRP_63
BD21 IO_T0U_N12_VRP_A28_65
V21 IO_T0U_N12_VRP_72

(page11)



pins to be used as
single ended links:
AY25 IO_T3U_N12_61
BB24 IO_T2U_N12_61
BE25 IO_T1U_N12_61
BH22 IO_T0U_N12_VRP_61
AW30 IO_T3U_N12_62
BB30 IO_T2U_N12_62
BF30 IO_T1U_N12_62
BL29 IO_T0U_N12_VRP_62
AT37 IO_T3U_N12_63
AU35 IO_T2U_N12_63
AY37 IO_T1U_N12_63
BD31 IO_T0U_N12_VRP_63

connect complete banks
swapping of complete banks allowed
swapping within banks allowed
if possible swap identically for all FPGAs
if possible do not connect GC pins to GC pins
connection of banks within busses:
bank 67 to 71
bank 70 to 72

Bank 68 (XCVU190) single-ended pins on :
IO_L(1-12)P/N 24 single

Bank 65 (XCVU190) differential pairs on :
IO_L1P/N, IO_L(3-19)P/N 18 diff

PARALLEL I/0

TITLE: StefanJFEX_Block_2016-06-30_v6

Document Number: REV:

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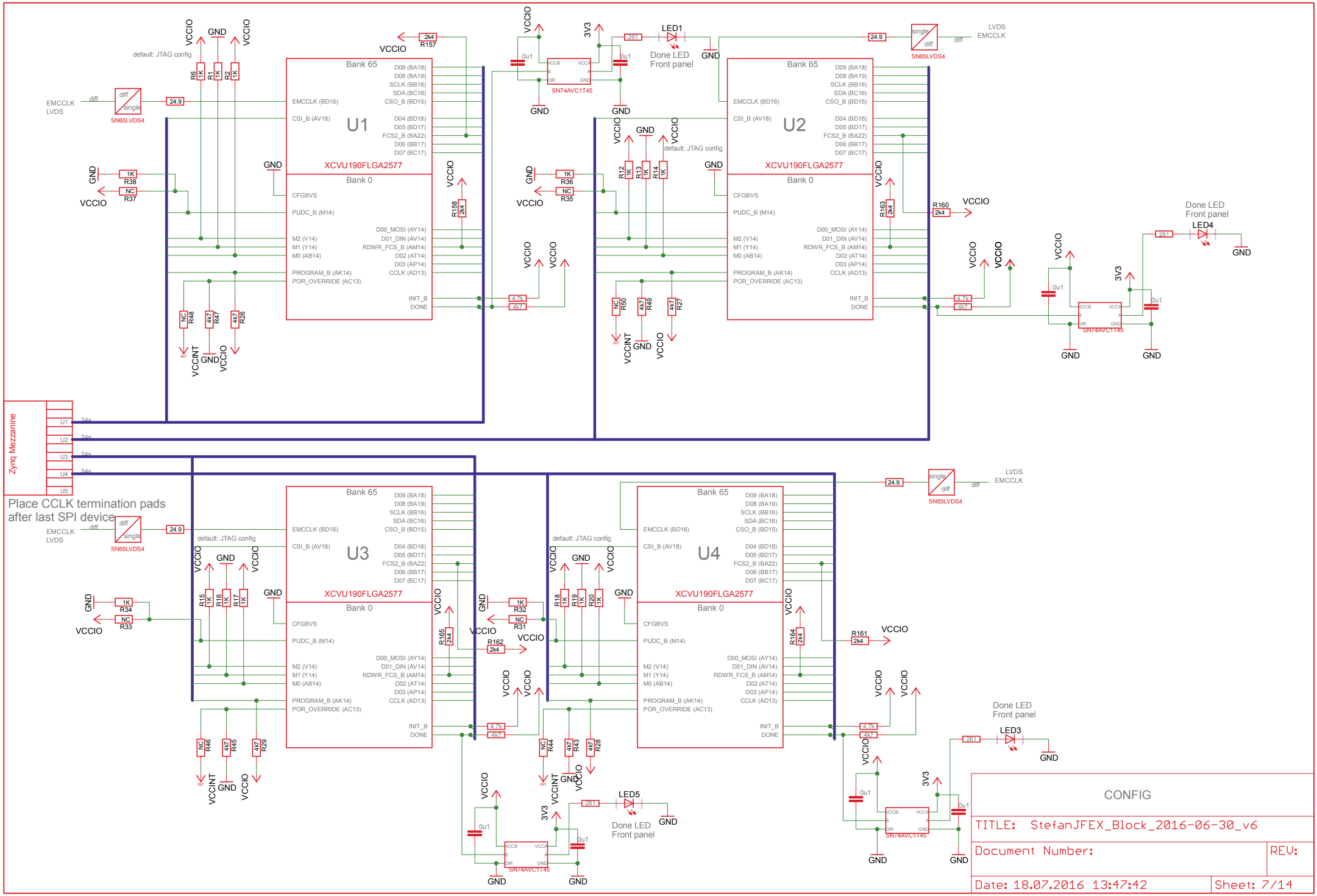
U1
U2
U3
U4
XCVU190FLGA2577
Bank 65
Bank 0
SN65LVDS4
SN74AVC1T45
Zynq Mezzanine
Place CCLK termination pads after last SPI device
default: JTAG config
Done LED Front panel
LED1
LED3
LED4
LED5
CONFIG
TITLE: StefanJFEX_Block_2016-06-30_v6
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REV:
Date: 18.07.2016 13:47:42
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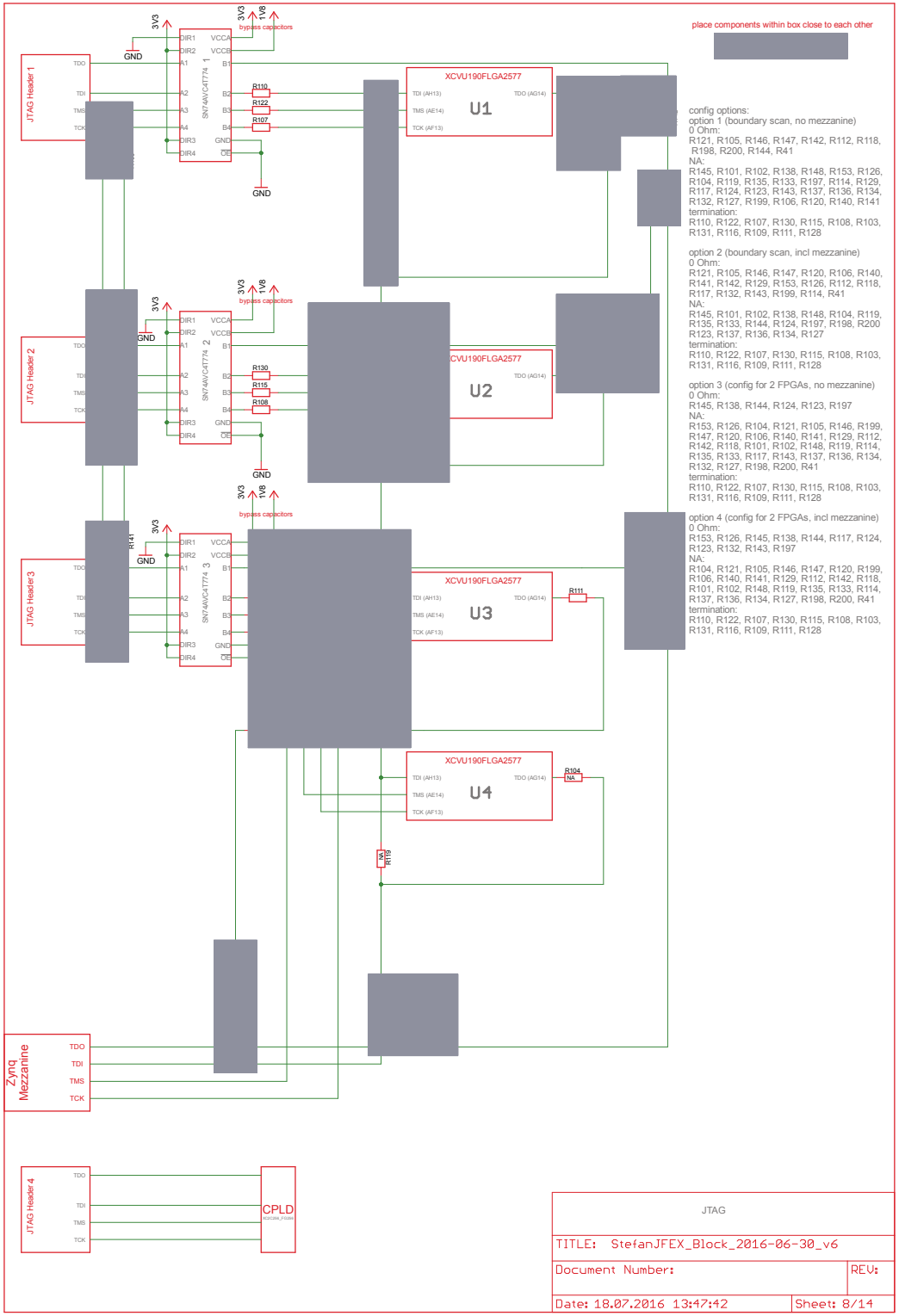
place components within box close to each other
JTAG Header 1
JTAG Header 2
JTAG Header 3
JTAG Header 4
SN74AVC4T774
XCVU190FLGA2577
U1
U2
U3
U4
CPLD
Zynq Mezzanine
bypass capacitors
3V3
1V8
GND
R110
R122
R107
R130
R115
R108
R41
R111
R104
R119
NA
config options:
option 1 (boundary scan, no mezzanine)
0 Ohm:
R121, R105, R146, R147, R142, R112, R118, R198, R200, R144, R41
NA:
R145, R101, R102, R138, R148, R153, R126, R104, R119, R135, R133, R197, R114, R129, R117, R124, R123, R143, R137, R136, R134, R132, R127, R199, R106, R120, R140, R141
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 2 (boundary scan, incl mezzanine)
0 Ohm:
R121, R105, R146, R147, R120, R106, R140, R141, R142, R129, R153, R126, R112, R118, R117, R132, R143, R199, R114, R41
NA:
R145, R101, R102, R138, R148, R104, R119, R135, R133, R144, R124, R197, R198, R200 R123, R137, R136, R134, R127
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 3 (config for 2 FPGAs, no mezzanine)
0 Ohm:
R145, R138, R144, R124, R123, R197
NA:
R153, R126, R104, R121, R105, R146, R199, R147, R120, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R114, R135, R133, R117, R143, R137, R136, R134, R132, R127, R198, R200, R41
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
option 4 (config for 2 FPGAs, incl mezzanine)
0 Ohm:
R153, R126, R145, R138, R144, R117, R124, R123, R132, R143, R197
NA:
R104, R121, R105, R146, R147, R120, R199, R106, R140, R141, R129, R112, R142, R118, R101, R102, R148, R119, R135, R133, R114, R137, R136, R134, R127, R198, R200, R41
termination:
R110, R122, R107, R130, R115, R108, R103, R131, R116, R109, R111, R128
JTAG
TITLE: StefanJFEX_Block_2016-06-30_v6
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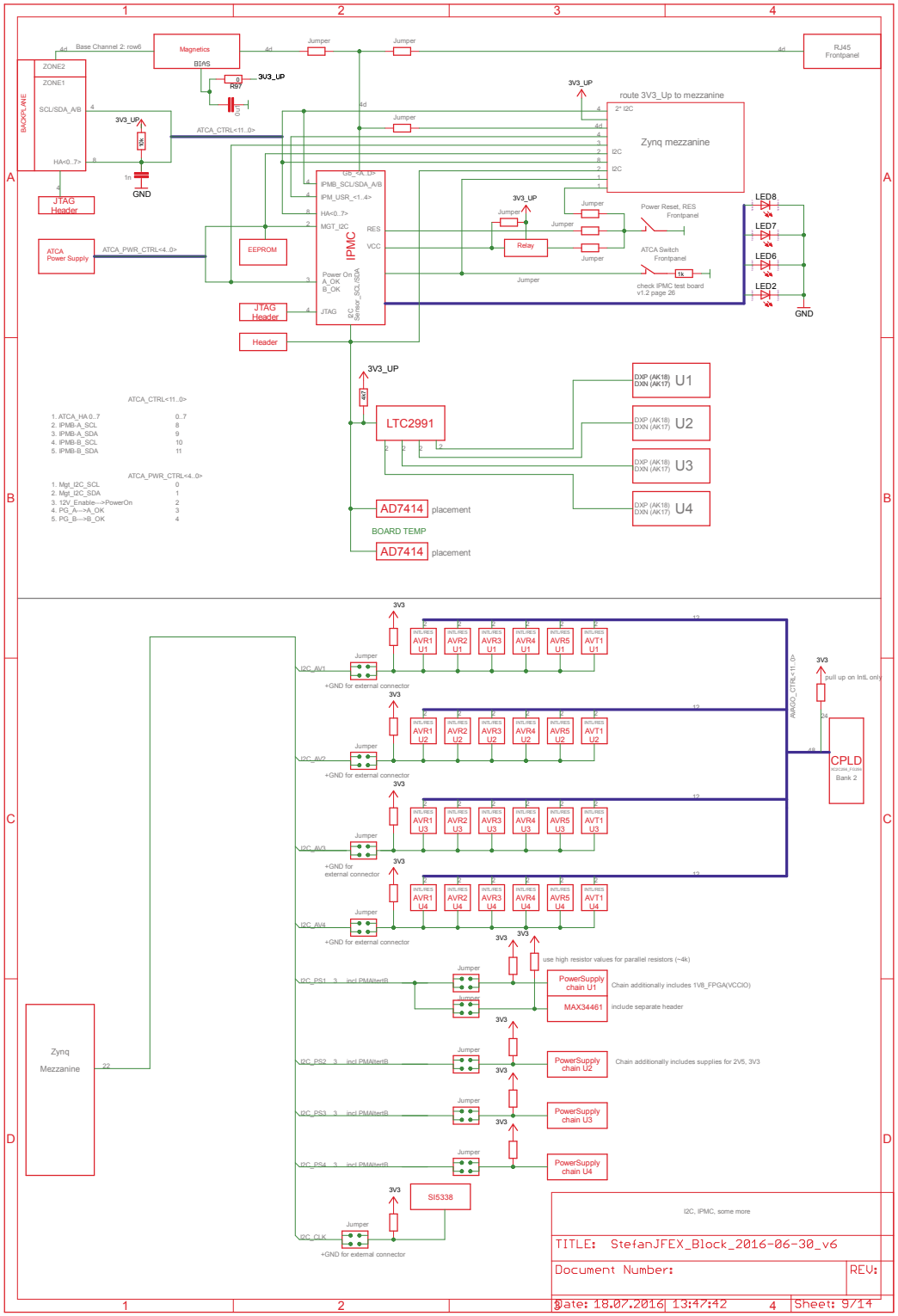
Base Channel 2: row6
Magnetics
BIAS
Jumper
RJ45 Frontpanel
ZONE2
ZONE1
SCL/SDA_A/B
HA<0..7>
BACKPLANE
3V3_UP
R97
ATCA_CTRL<11..0>
route 3V3_Up to mezzanine
2* I2C
Zynq mezzanine
I2C
JTAG Header
ATCA Power Supply
ATCA_PWR_CTRL<4..0>
EEPROM
IPMC
IPMB_SCL/SDA_A/B
IPM_USR_<1..4>
MGT_I2C
RES
VCC
Power On
A_OK
B_OK
JTAG
Relay
Power Reset, RES Frontpanel
ATCA Switch Frontpanel
check IPMC test board v1.2 page 26
LED8
LED7
LED6
LED2
GND
Header
LTC2991
AD7414
placement
BOARD TEMP
U1
U2
U3
U4
ATCA_CTRL<11..0>
1. ATCA_HA 0..7 0..7
2. IPMB-A_SCL 8
3. IPMB-A_SDA 9
4. IPMB-B_SCL 10
5. IPMB-B_SDA 11
ATCA_PWR_CTRL<4..0>
1. Mgt_I2C_SCL 0
2. Mgt_I2C_SDA 1
3. 12V_Enable--->PowerOn 2
4. PG_A--->A_OK 3
5. PG_B--->B_OK 4
AVR1 U1
AVR2 U1
AVR3 U1
AVR4 U1
AVR5 U1
AVT1 U1
AVR1 U2
AVR2 U2
AVR3 U2
AVR4 U2
AVR5 U2
AVT1 U2
AVR1 U3
AVR2 U3
AVR3 U3
AVR4 U3
AVR5 U3
AVT1 U3
AVR1 U4
AVR2 U4
AVR3 U4
AVR4 U4
AVR5 U4
AVT1 U4
I2C_AV1
I2C_AV2
I2C_AV3
I2C_AV4
+GND for external connector
AMC13_CTRL<11..0>
pull up on IntL only
CPLD
Bank 2
Zynq Mezzanine
use high resistor values for parallel resistors (~4k)
I2C_PS1_3_ incl PMAlertB
I2C_PS2_3_ incl PMAlertB
I2C_PS3_3_ incl PMAlertB
I2C_PS4_3_ incl PMAlertB
PowerSupply chain U1
MAX34461
include separate header
Chain additionally includes 1V8_FPGA(VCCIO)
PowerSupply chain U2
Chain additionally includes supplies for 2V5, 3V3
PowerSupply chain U3
PowerSupply chain U4
SI5338
I2C_CLK
I2C, IPMC, some more
TITLE: StefanJFEX_Block_2016-06-30_v6
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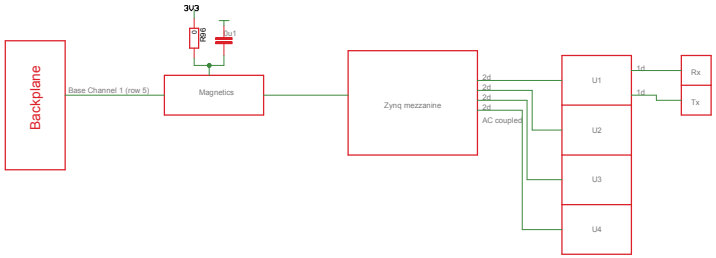
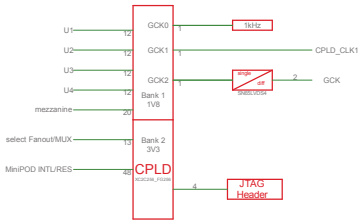
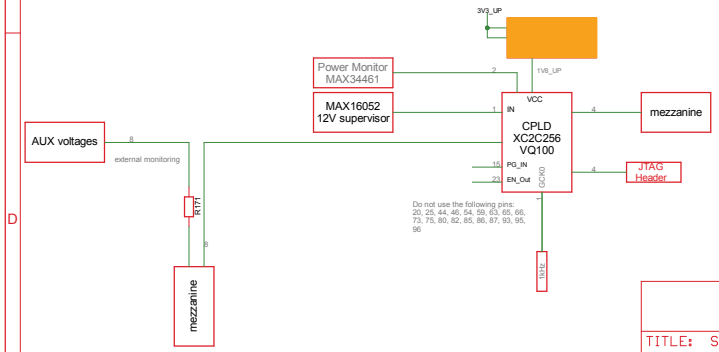
IPBUS



CPLD



sCPLD
power sequencing



IPBus (summary)

TITLE: StefanJFEX_Block_2016-06-30_v6

Document Number:

REV:

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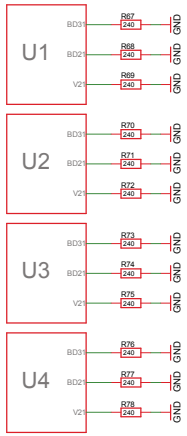
pins used for DCI refferenz resistors:
BD31 IO_T0U_N12_VRP_63
BD21 IO_T0U_N12_VRP_A28_65
V21   IO_T0U_N12_VRP_72



DCI

TITLE: StefanJFEX_Block_2016-06-30_v6

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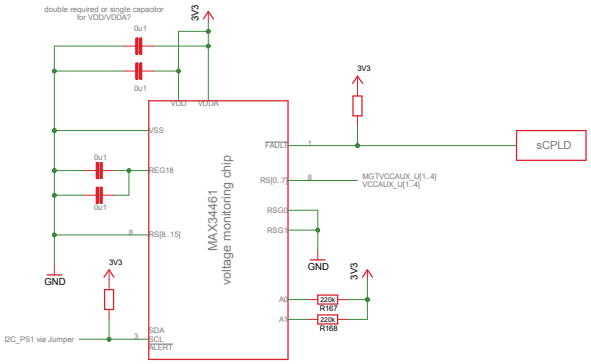

VCCAUX monitoring

TITLE: StefanJFEX_Block_2016-06-30_v6

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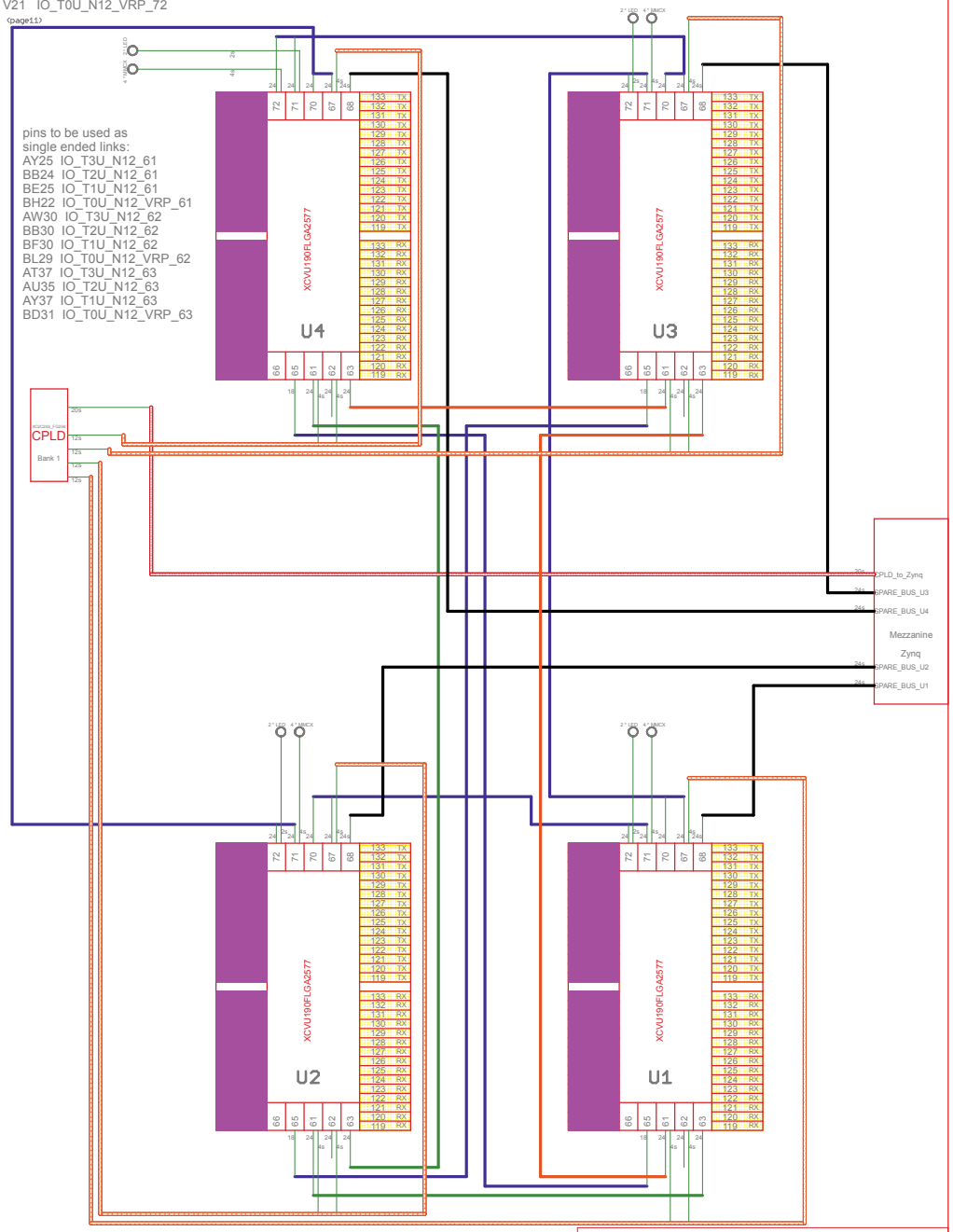
pins used for DCI referenz resistors(240R):
BD31 IO_T0U_N12_VRP_63
BD21 IO_T0U_N12_VRP_A28_65
V21 IO_T0U_N12_VRP_72



connect complete banks
swapping of complete banks allowed
swapping within banks allowed
if possible swap identically for all FPGAs
if possible do not connect GC pins to GC pins
connection of banks within busses:
bank 67 to 71
bank 70 to 72

Bank 68 (XCVU190) single-ended pins on :
IO_L(1-12)P/N 24 single

Bank 65 (XCVU190) differential pairs on :
IO_L1P/N, IO_L(3-19)P/N 18 diff

PARALLEL I/0

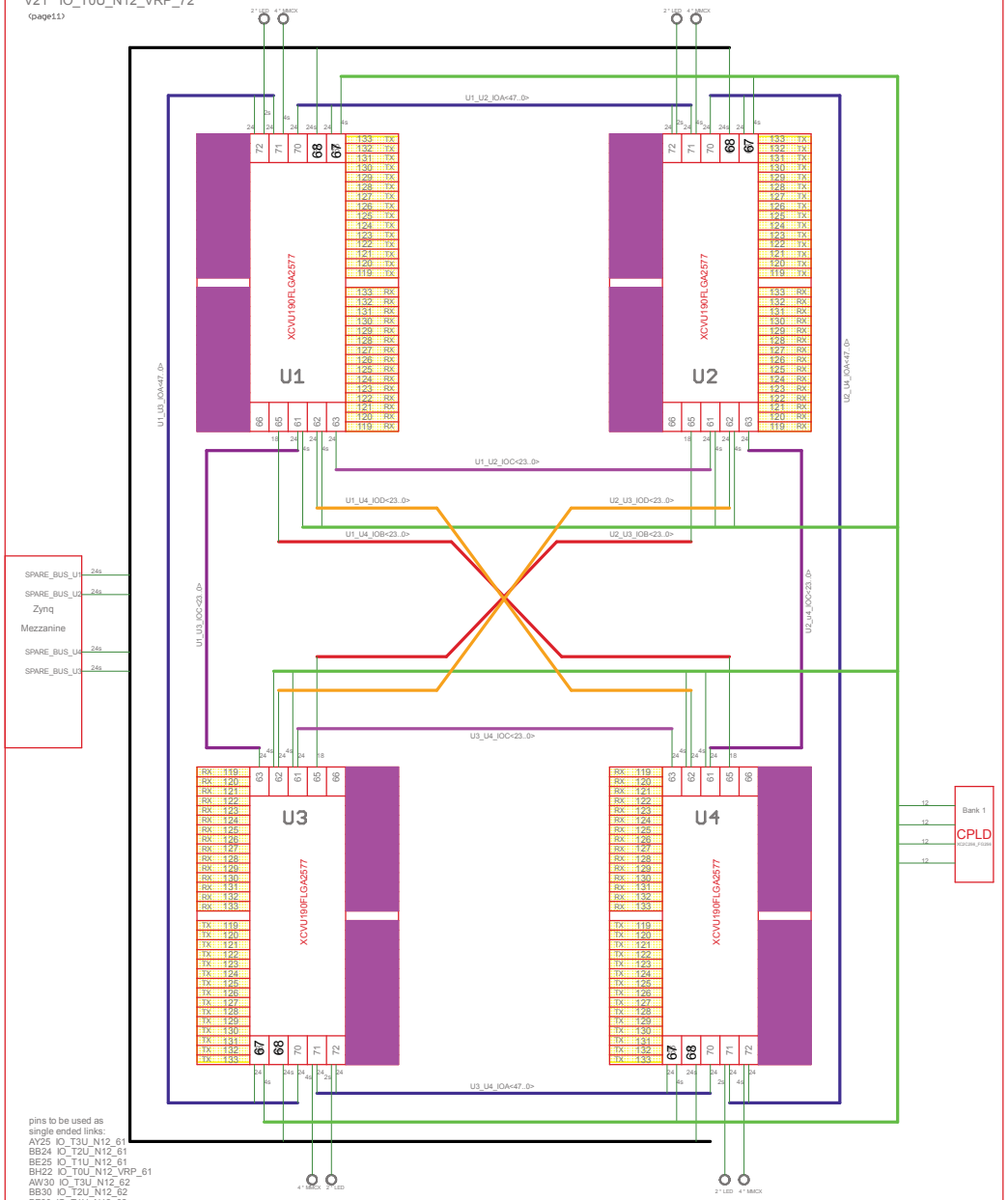
TITLE: StefanJFEX_Block_2016-06-30_v6

Document Number: REV:

Date: 18.07.2016 13:47:42 Sheet: 13/14

pins used for DCI referenz resistors(240R):
BD31 IO_T0U_N12_VRP_63
BD21 IO_T0U_N12_VRP_A28_65
V21 IO_T0U_N12_VRP_72

<page1>



pins to be used as
single ended links:
AY25 IO_T3U_N12_61
BB24 IO_T2U_N12_61
BE25 IO_T1U_N12_61
BH22 IO_T0U_N12_VRP_61
AW30 IO_T3U_N12_62
BB30 IO_T2U_N12_62
BF30 IO_T1U_N12_62
BL29 IO_T0U_N12_VRP_62
AT37 IO_T3U_N12_63
AU35 IO_T2U_N12_63
AY37 IO_T1U_N12_63
BD31 IO_T0U_N12_VRP_63

connect complete banks
swapping of complete banks allowed
swapping within banks allowed
if possible swap identically for all FPGAs
if possible do not connect GC pins to GC pins
connection of banks within busses:
bank 67 to 71
bank 70 to 72

Bank 68 (XCVU190) single-ended pins on :
IO_L(1-12)P/N 24 single

Bank 65 (XCVU190) differential pairs on :
IO_L1P/N, IO_L(3-19)P/N 18 diff

PARALLEL I/0

TITLE: StefanJFEX_Block_2016-06-30_v6

Document Number:

REV:

Date: 18.07.2016 13:47:42

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