REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

INDEX PAGE(S) FUNCTION

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE

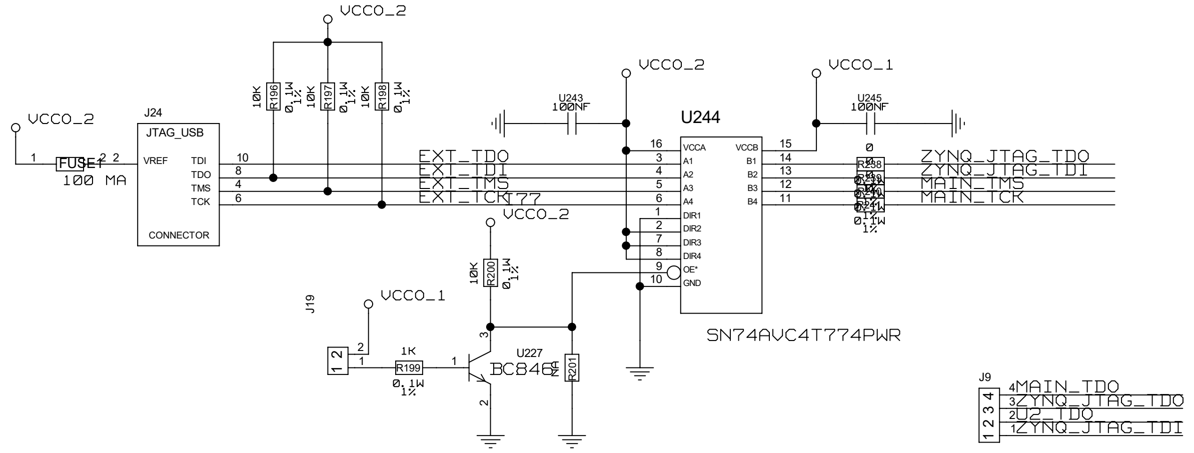
DRAWING TITLE
JFEX AND TOPO PHASE-I
CONTROL MEZZANINE

JOHANNES GUTENBERG
UNIVERSITY MAINZ

SIZE C | REV. | DRAWING NO.

SCALE 3.0 | SHEET 1 OF 13

JTAG



FOR CONNECTION
TO MAINBOARD:
CONNECT PINS 1 AND 2
CONNECT PINS 3 AND 4

VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE JTAG

DRAWING TITLE

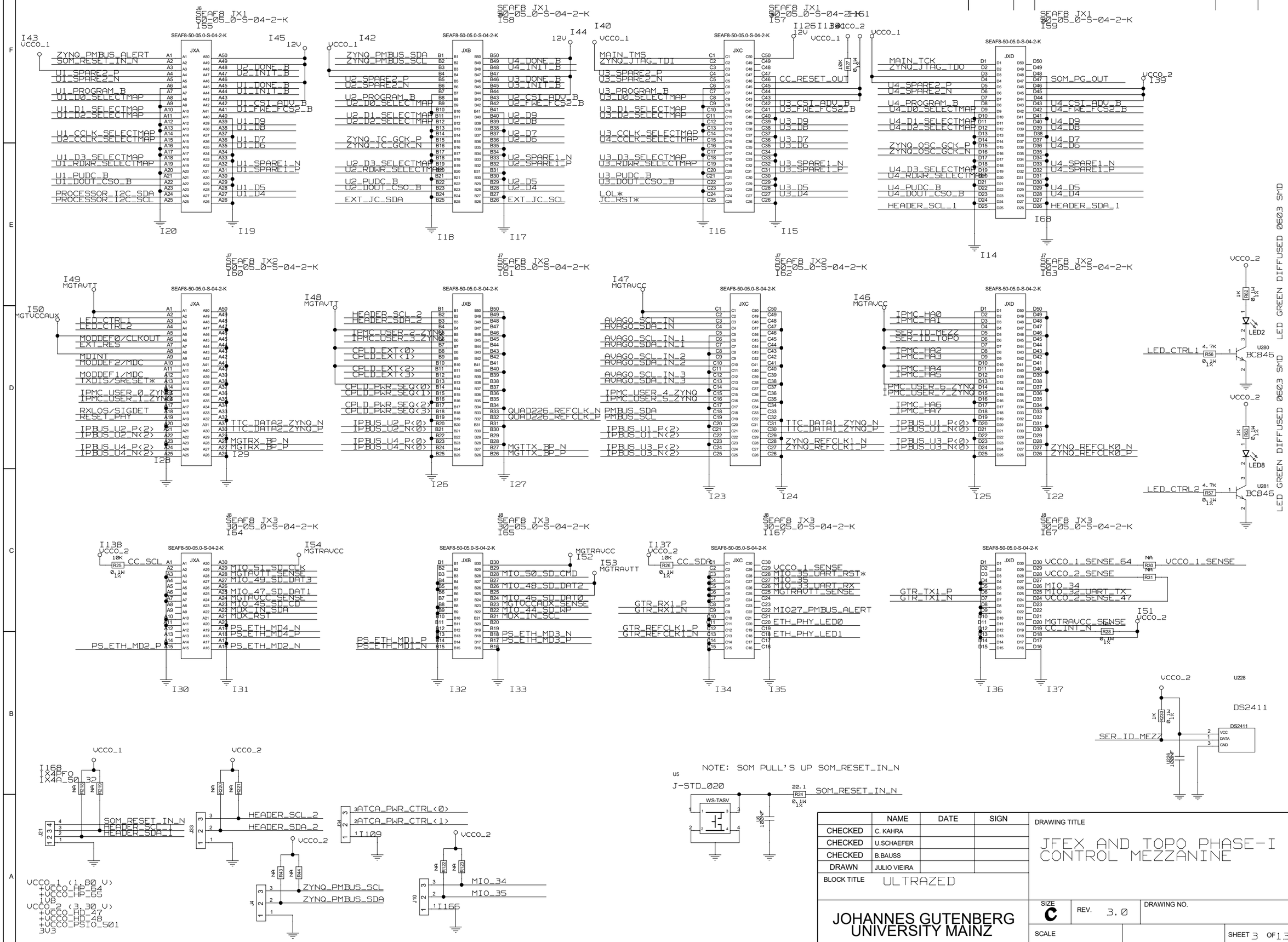
JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: ULTRAZED

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE: C | REV.: 3.0 | DRAWING NO.:

SCALE:

SHEET 3 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

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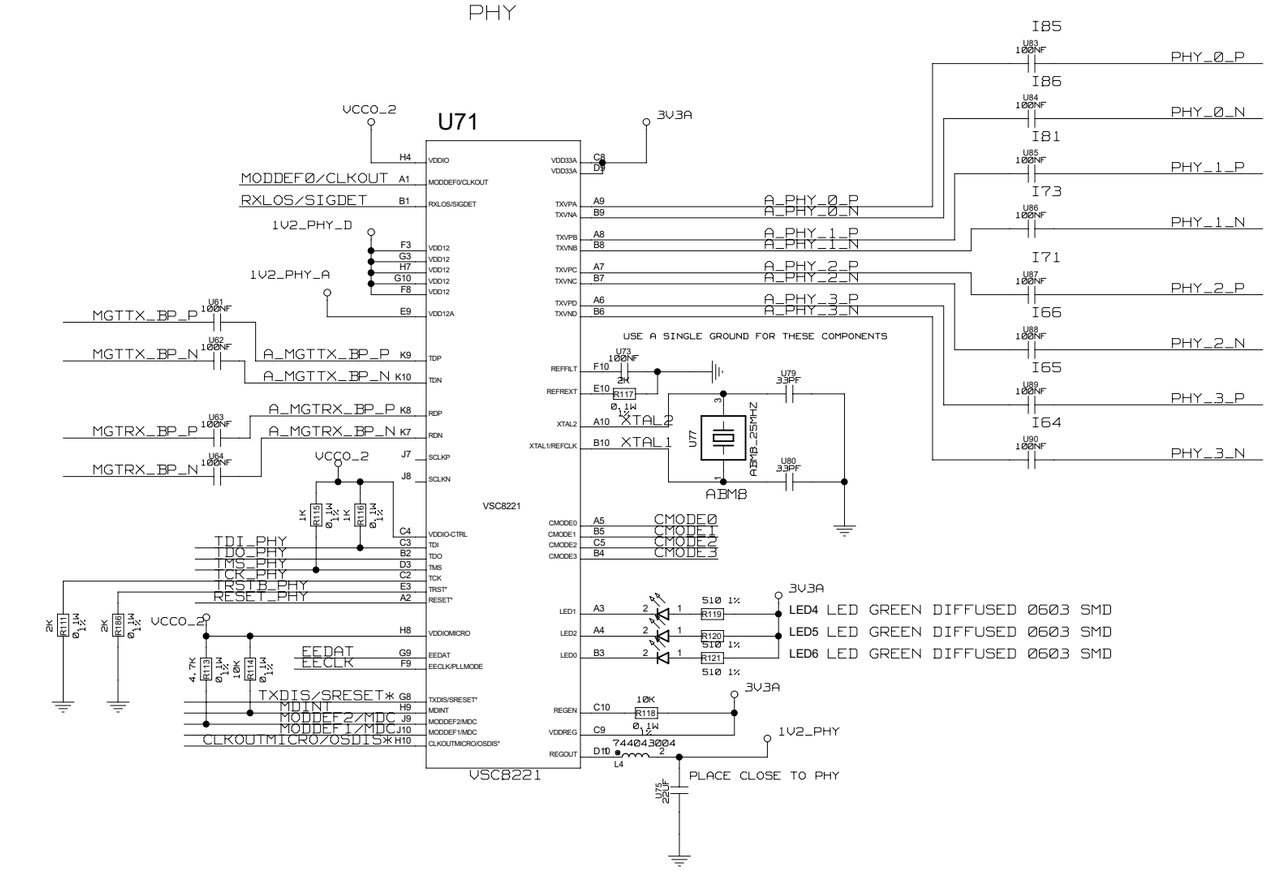

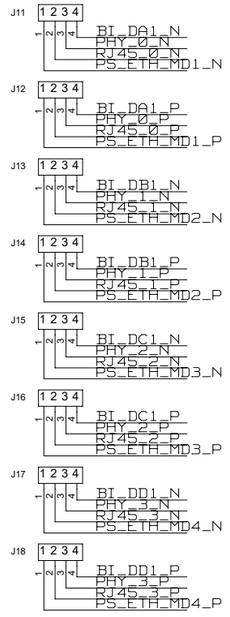

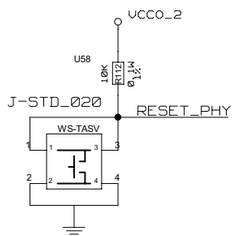

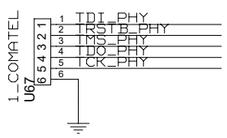

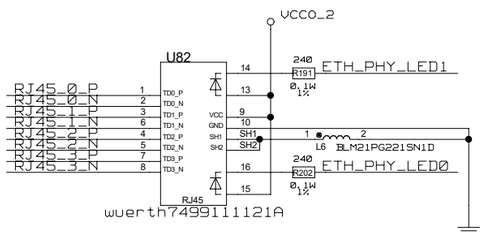

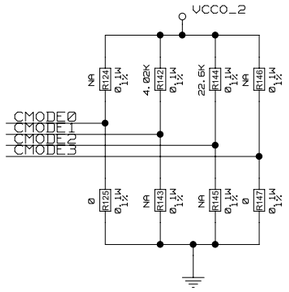

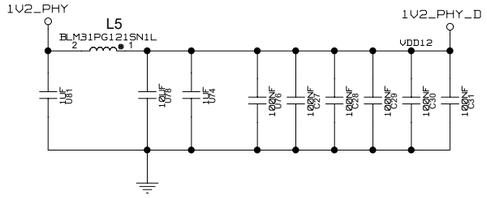

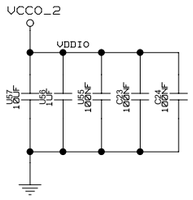

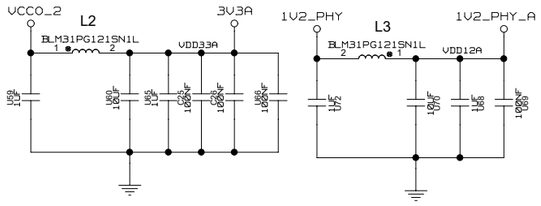

VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
+VB
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: PHY - IPBUS

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

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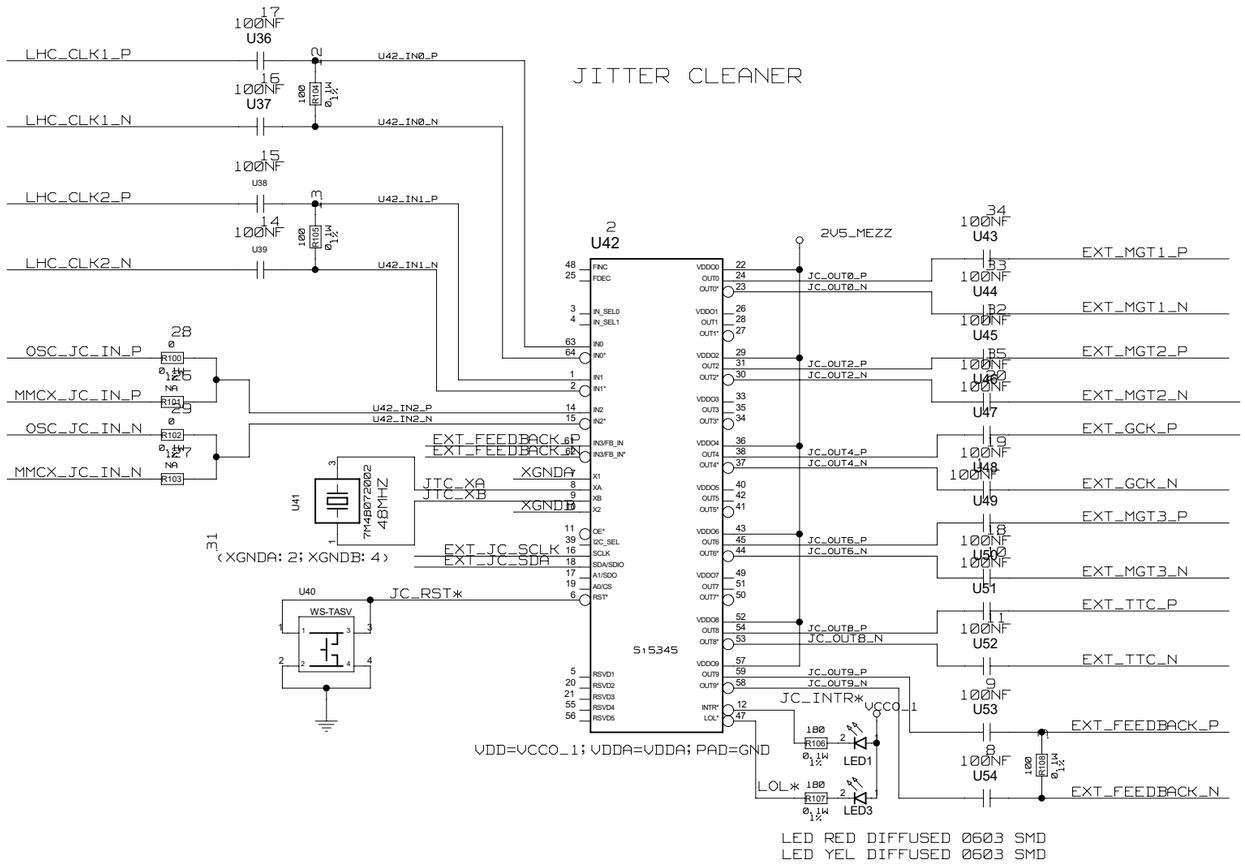
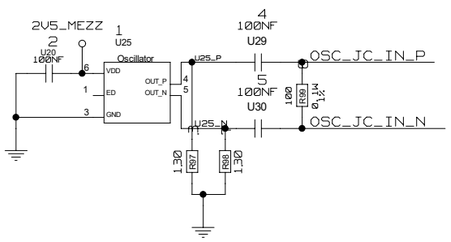
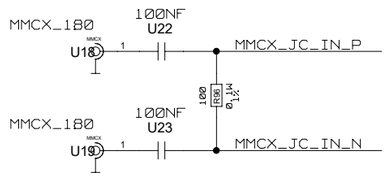
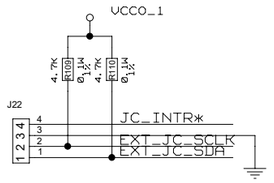
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

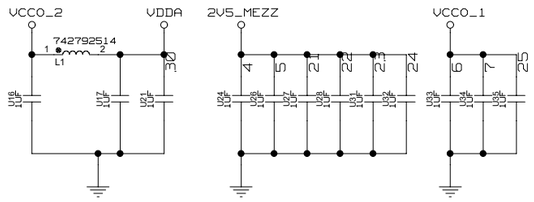
JITTER CLEANER











VCCO_1 (1.80 V)
++VCCO_HD_D01
++VCCO_HP_D51
+VCCO
VCCO_2 (3.30 V)
+VCCO_HD_A47
++VCCO_HD_AB
++VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: JITTER CLEANER

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

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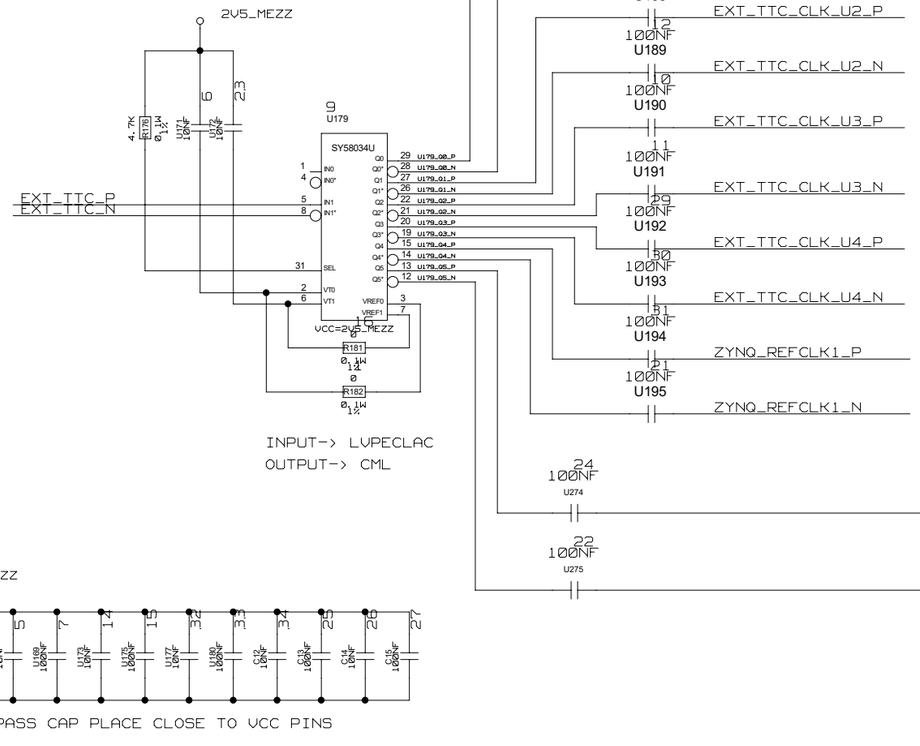
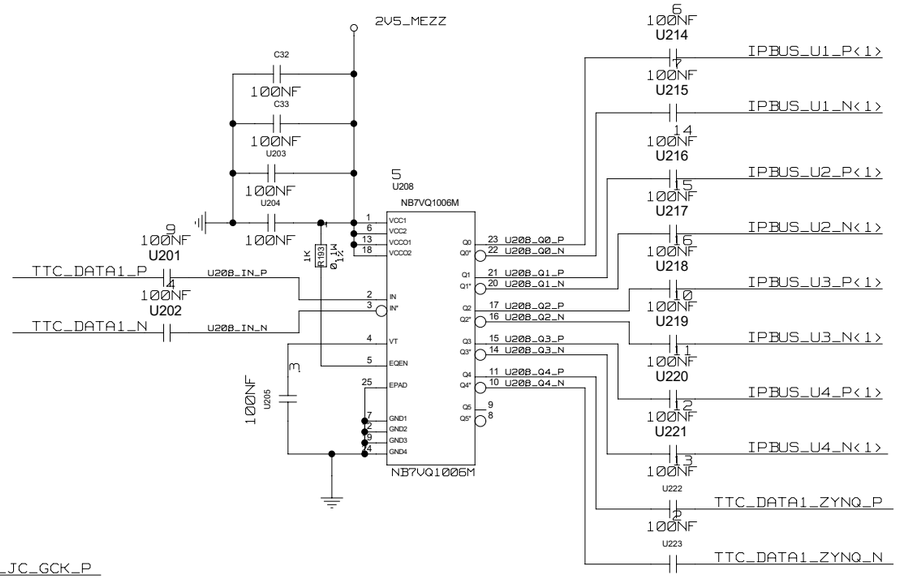
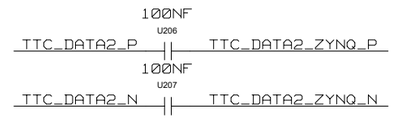
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

TTC DATA REFCLK

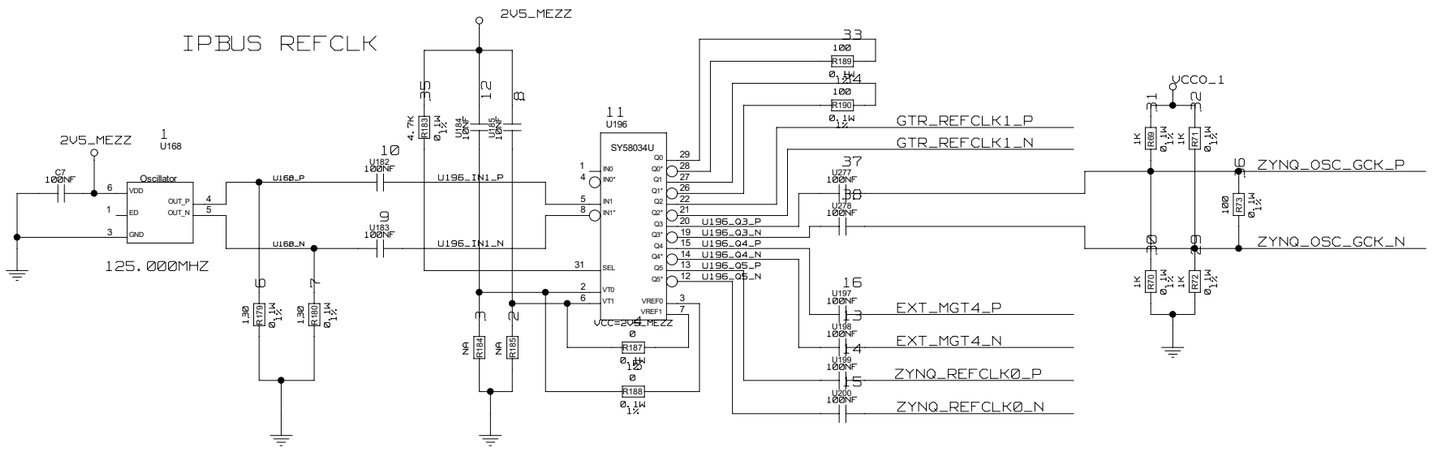


TTC DATA FANOUT

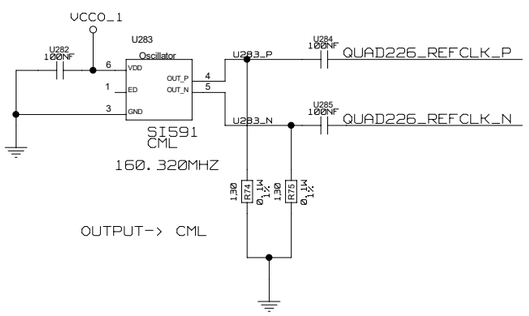


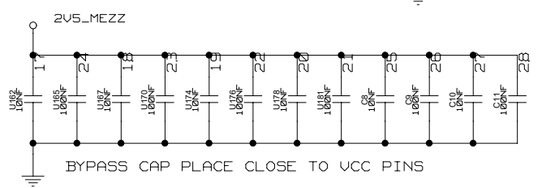


IPBUS REFCLK



SPARE MGT REFCLK





	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: CLOCK DISTRIBUTION

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

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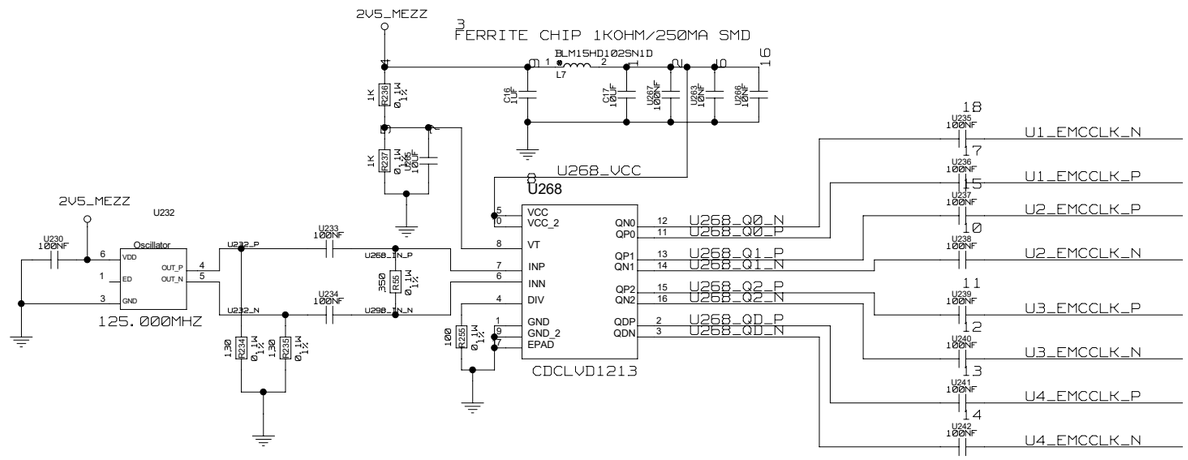
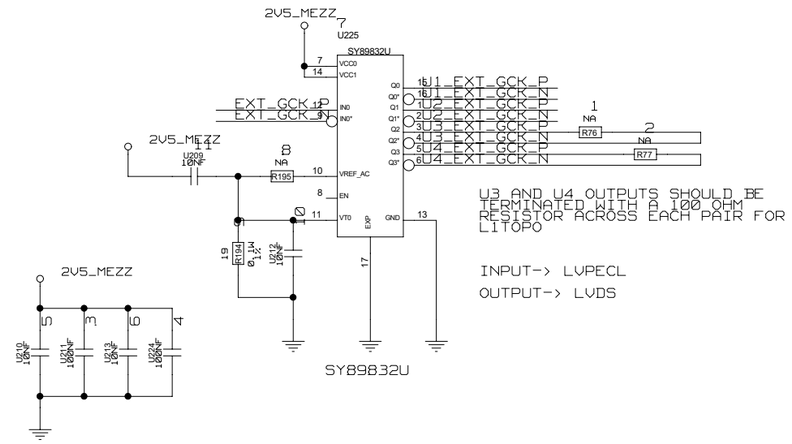
EXTERNAL MASTER CONFIGURATION CLOCK

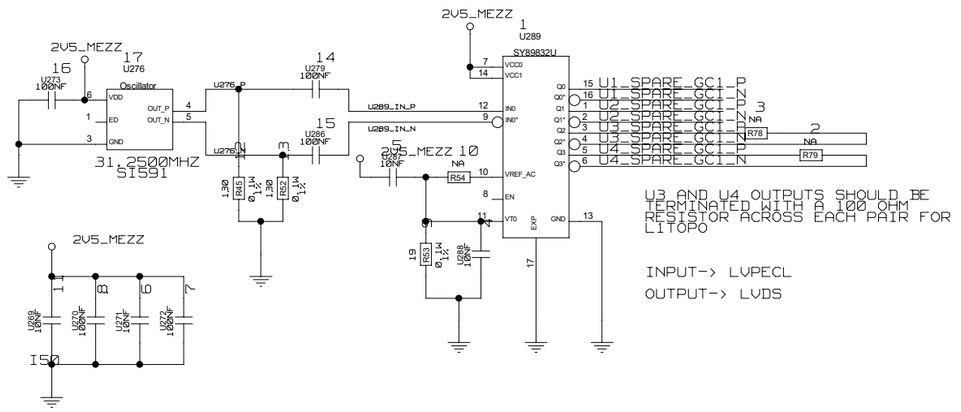


INPUT-> LVPECLAC
OUTPUT-> LVDS

CLEANED GLOBAL CLOCK



SPARE CLOCK TO PROCESSORS



VCCO_1 (1.80 V)
+VCCO_HP_54
+VCCO_HP_55
+VB
VCCO_2 (3.30 V)
+VCCO_HP_47
+VCCO_HP_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: CLOCK DISTRIBUTION

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

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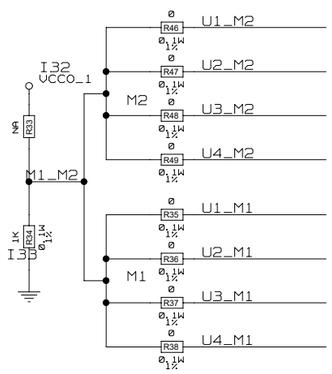
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

M1 & M2



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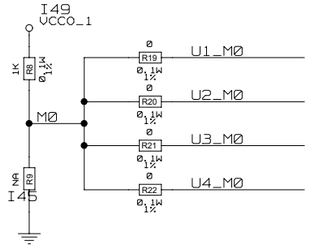
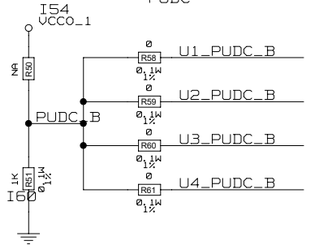
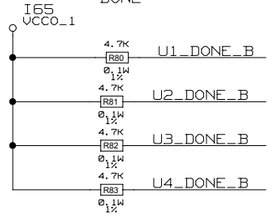


PUDC



DONE



MASTER SPI	SLAVE SELECTMAP
M0 -> 1	M0 -> 0
M1 -> 0	M1 -> 1
M2 -> 0	M2 -> 1

U1_D0_SPI / U1_D0 / U1_D0_SELECTMAP

U1_D1_SPI / U1_D1 / U1_D1_SELECTMAP

U1_D2_SPI / U1_D2 / U1_D2_SELECTMAP

U1_D3_SPI / U1_D3 / U1_D3_SELECTMAP

U2_D0_SPI / U2_D0 / U2_D0_SELECTMAP

U2_D1_SPI / U2_D1 / U2_D1_SELECTMAP

U2_D2_SPI / U2_D2 / U2_D2_SELECTMAP

U2_D3_SPI / U2_D3 / U2_D3_SELECTMAP

U3_D0_SPI / U3_D0 / U3_D0_SELECTMAP

U3_D1_SPI / U3_D1 / U3_D1_SELECTMAP

U3_D2_SPI / U3_D2 / U3_D2_SELECTMAP

U3_D3_SPI / U3_D3 / U3_D3_SELECTMAP

U4_D0_SPI / U4_D0 / U4_D0_SELECTMAP

U4_D1_SPI / U4_D1 / U4_D1_SELECTMAP

U4_D2_SPI / U4_D2 / U4_D2_SELECTMAP

U4_D3_SPI / U4_D3 / U4_D3_SELECTMAP

U1_CCLK_SPI / U1_CCLK / U1_CCLK_SELECTMAP

U1_FCS_SPI / U1_RDWR_FCS_B / U1_RDWR_SELECTMAP

U2_CCLK_SPI / U2_CCLK / U2_CCLK_SELECTMAP

U2_FCS_SPI / U2_RDWR_FCS_B / U2_RDWR_SELECTMAP

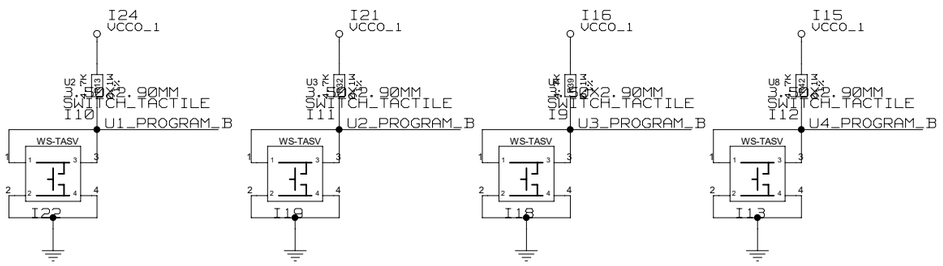
U3_CCLK_SPI / U3_CCLK / U3_CCLK_SELECTMAP

U3_FCS_SPI / U3_RDWR_FCS_B / U3_RDWR_SELECTMAP

U4_CCLK_SPI / U4_CCLK / U4_CCLK_SELECTMAP

U4_FCS_SPI / U4_RDWR_FCS_B / U4_RDWR_SELECTMAP

PROGRAM_B



NET V3.0	NET JFEX
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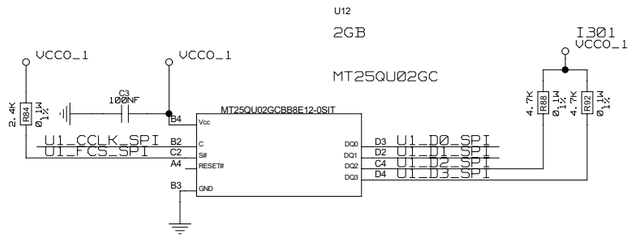
DONE	UN_CONF<12>
PROGRAM_B	UN_CONF<13>
M0	UN_CONF<14>
M1	UN_CONF<15>
M2	UN_CONF<16>
CCLK	UN_CONF<17>
D0	UN_CONF<18>
D1	UN_CONF<19>
D2	UN_CONF<20>
D3	UN_CONF<21>
RDWR_FCS_B	UN_CONF<22>
PUDC_B	UN_CONF<23>

SPI MEMORIES



VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: FPGA CONF

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE: C | REV. 3.0 | DRAWING NO.

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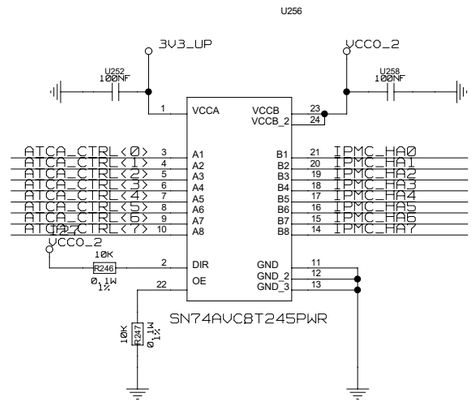
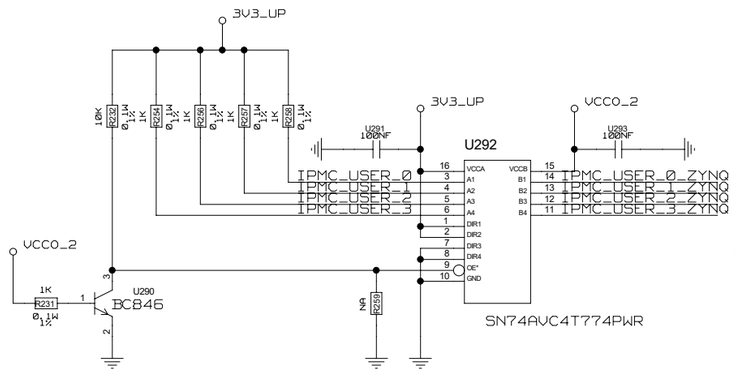
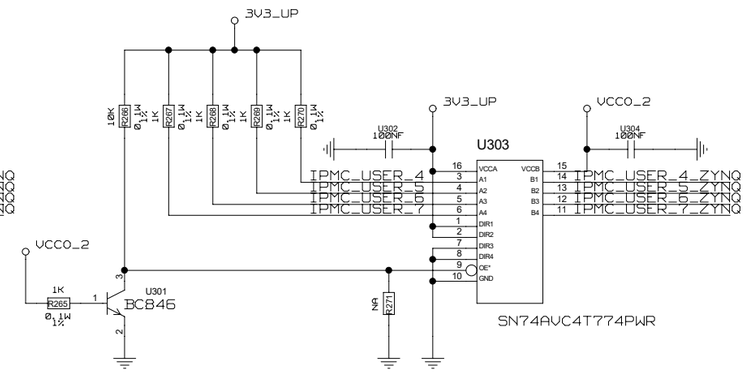
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

IPMC - LEVEL TRANSLATOR







	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	IPMC LEVEL TRANS		

DRAWING TITLE

JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

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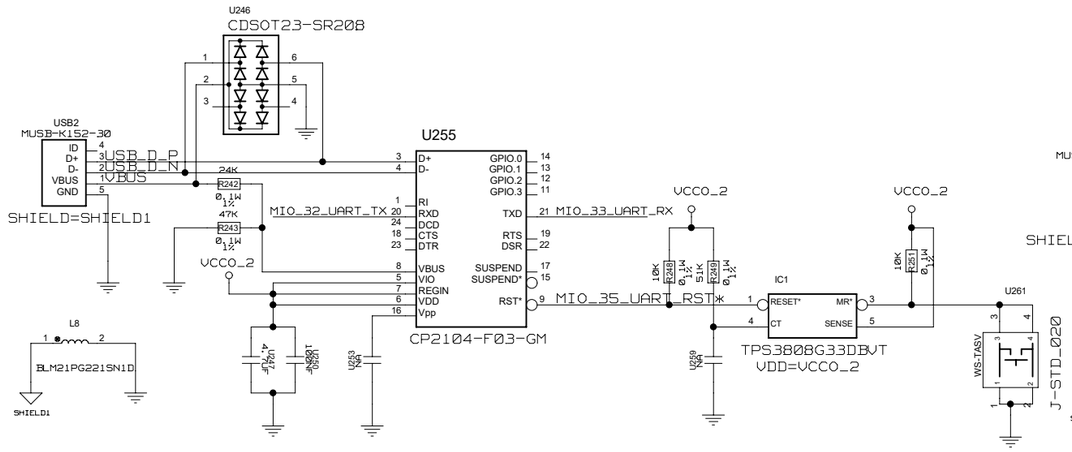
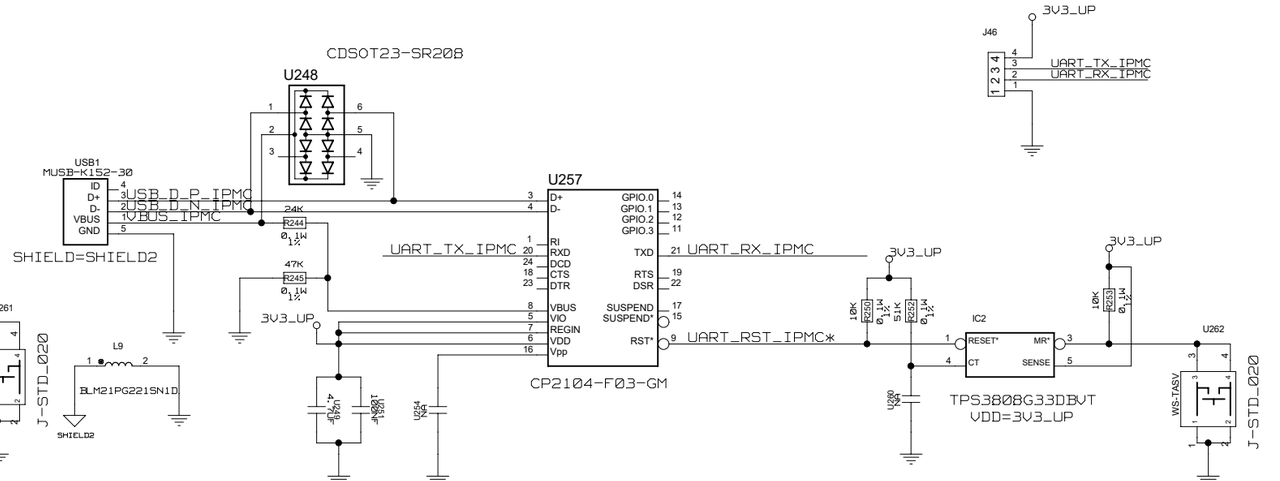
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

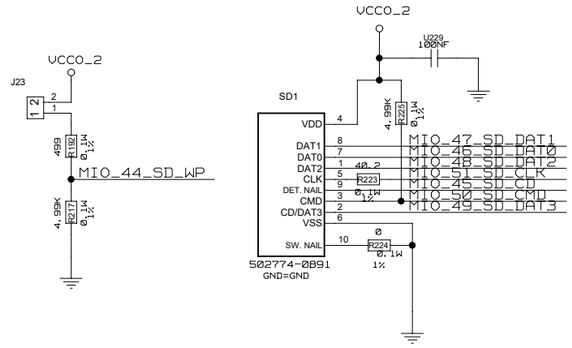
USB UART



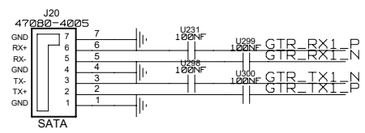
IPMC UART



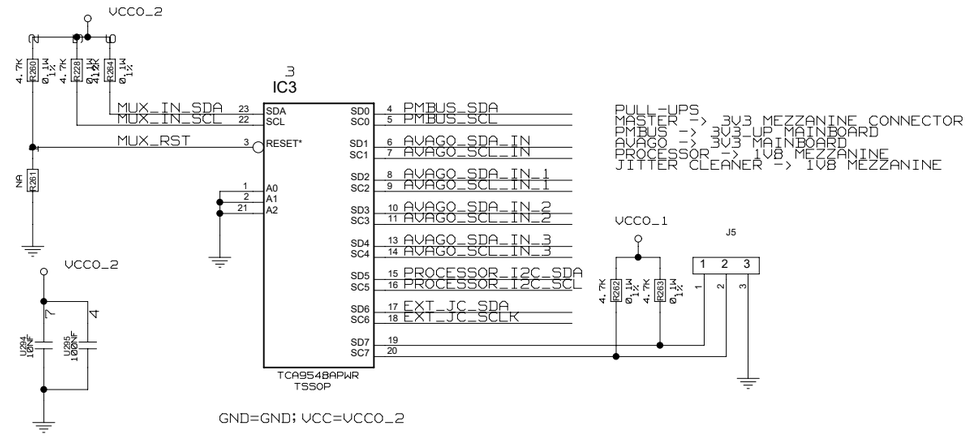
MICRO SD CARD



SATA INTERFACE



I2C - MUX



VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
IVB
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: UART, I2C MUX MICRO SD CARD

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

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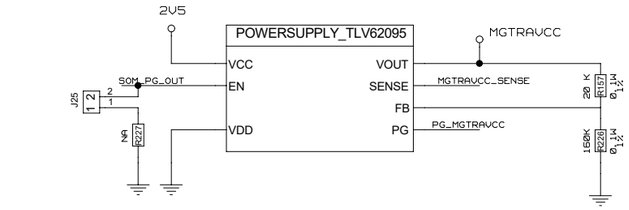
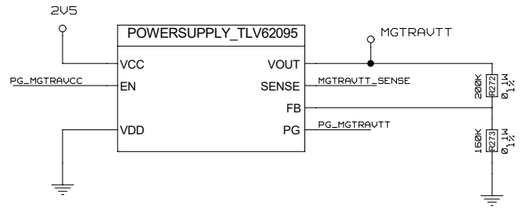
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

MGTRAVCC – 0.85V



NOTE:RES TO BE PLACED IF USING WITHOUT ULTRZED

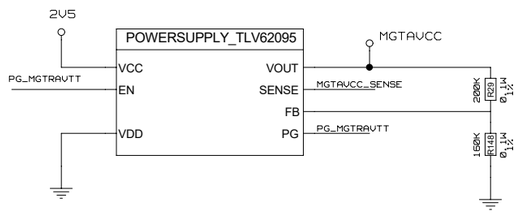
MGTRAVTT – 1.8V



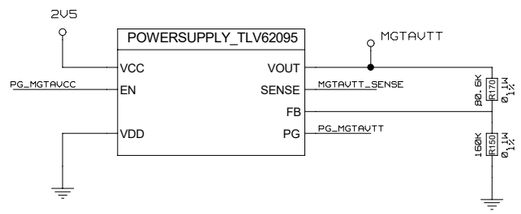
POWER SEQUENCING:
1- SOM_PG_OUT
2- PS_MGTRAVCC (0.85 V)
3- PS_MGTRAVTT (1.80 V)
4- PL_MGTRAVCC (0.90 V)
5- PL_MGTAVTT (1.200 V)
6- PL_MGTVCCAUX (1.80 V)
7- VCCO_1 (1.80 V)
8- VCCO_2 (3.30 V)
9- 2V5 (2.5 V)

VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

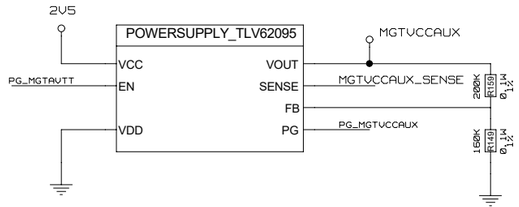
MGTAVCC – 0.9V



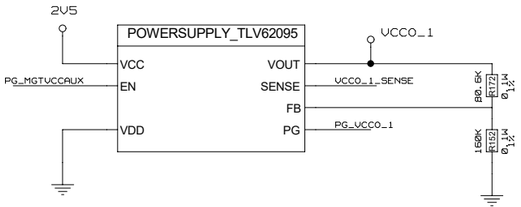
MGTAVTT – 1.2V



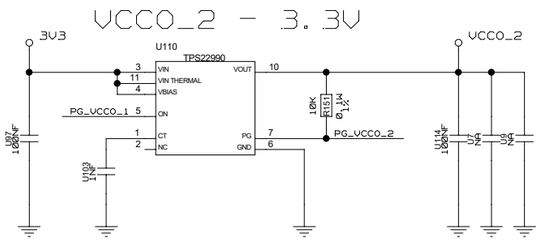
MGTVCCAUX – 1.8V



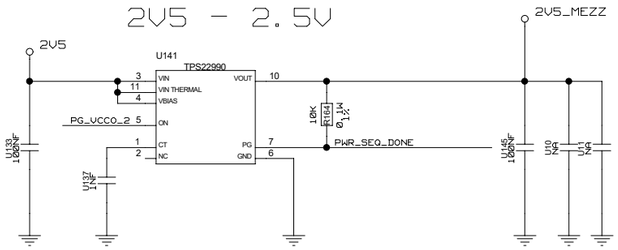
VCCO_1 – 1.8V

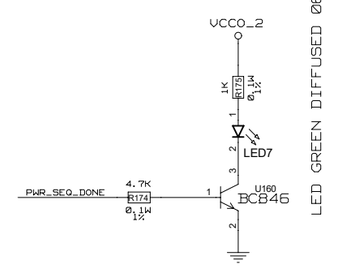


VCCO_2 – 3.3V



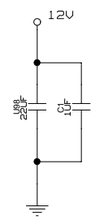
2V5 – 2.5V



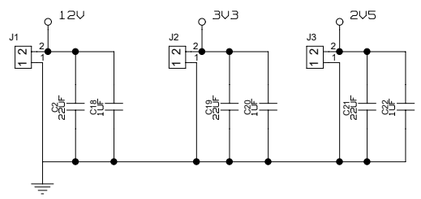


LED GREEN DIFFUSED 0603 SMD

SOM VIN – 12V



EXTERNAL POWER (WITHOUT JFEX/TOPO)
MANUAL POWER UP (WITHOUT JFEX/TOPO)



	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	POWER		

DRAWING TITLE

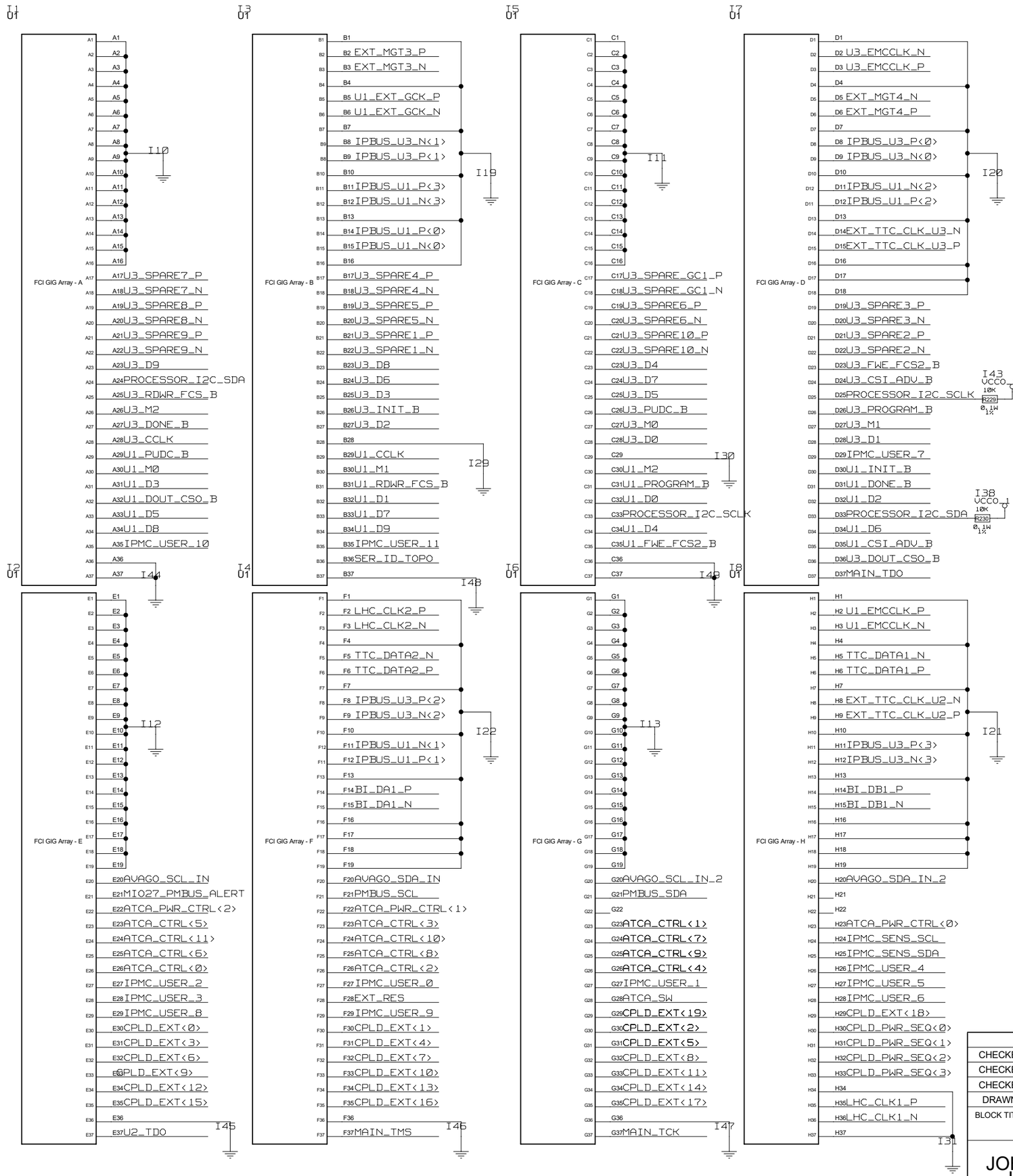
JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 11 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	JFEX/TOPO		

DRAWING TITLE

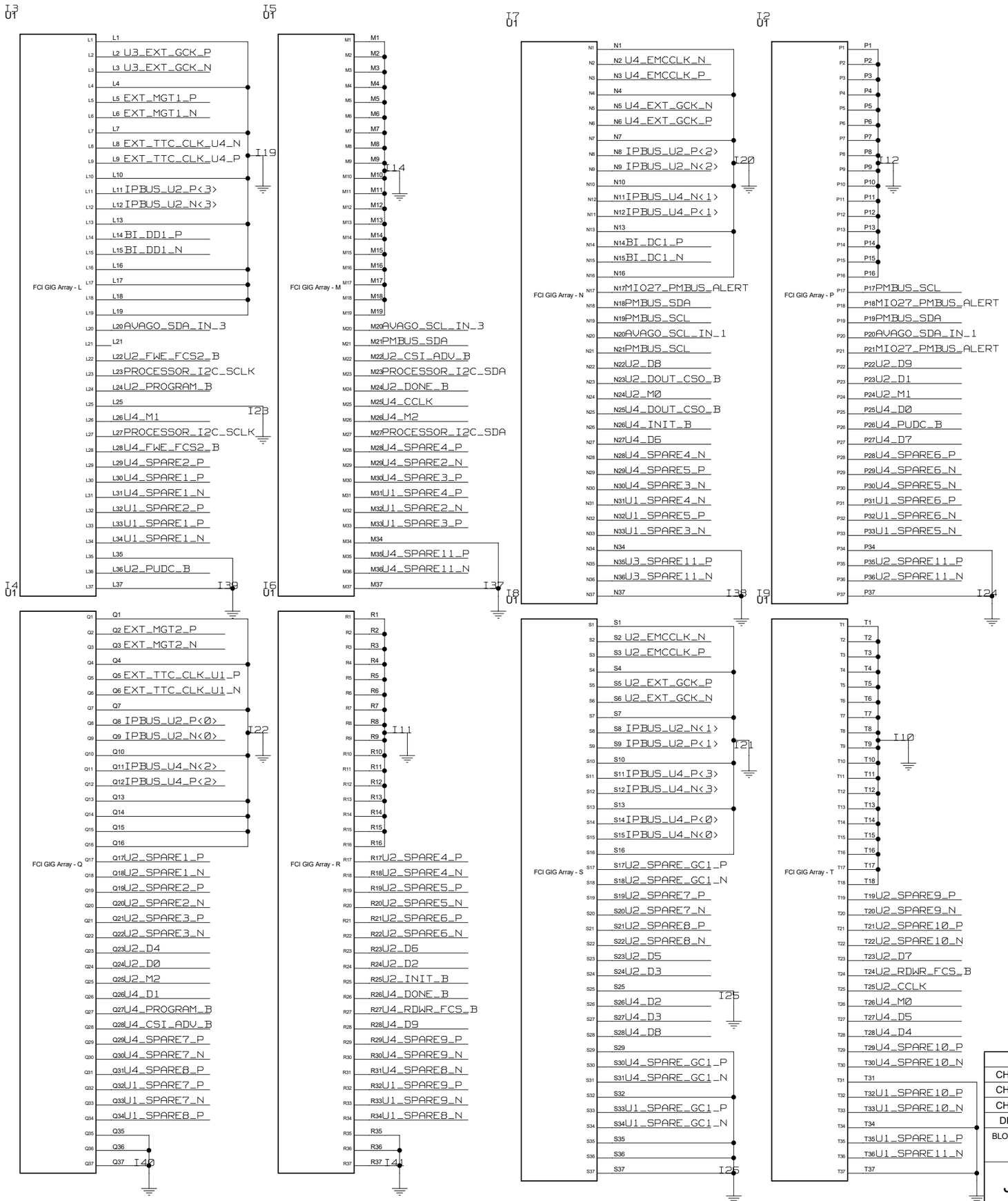
JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 12 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE JFEX/TOPO

DRAWING TITLE

JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE

SHEET 13 OF 13