REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

INDEX PAGE(S) FUNCTION

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE

DRAWING TITLE
JFEX AND TOPO PHASE-I
CONTROL MEZZANINE

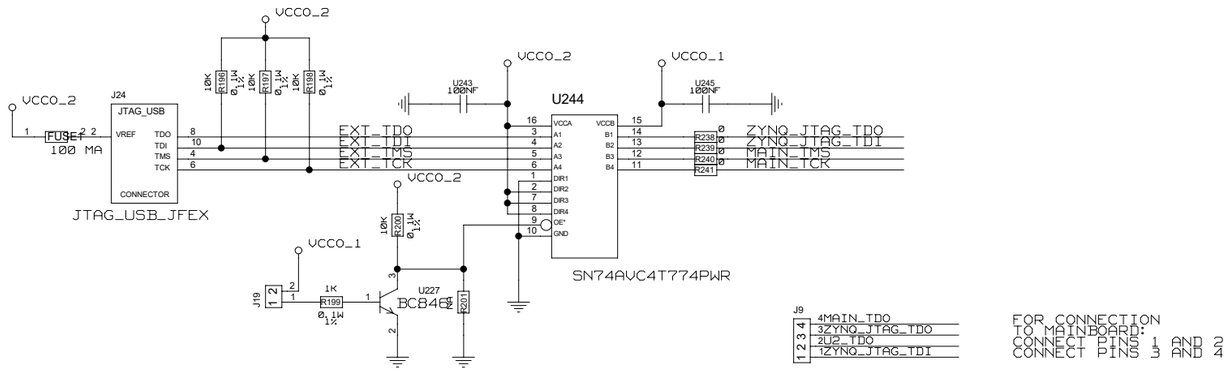
JOHANNES GUTENBERG
UNIVERSITY MAINZ

SIZE C | REV. | DRAWING NO.

SCALE 3.0 | SHEET 1 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

JTAG



VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HP_47
+VCCO_HP_48
+VCCO_PS10_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: JTAG

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE: C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 2 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

J6 SEAF8_JX1 50-05_0-S-04-2-K I55

I43 VCCO_1
- ZYNQ_PMBUS_ALERT — A1
- SOM_RESET_IN_N — A2
- U1_SPARE2_P — A3
- U1_SPARE2_N — A4
- U1_PROGRAM_B — A5
- U1_D0_SELECTMAP — A6
- U1_D1_SELECTMAP — A7
- U1_D2_SELECTMAP — A8
- U1_CCLK_SELECTMAP — A9
- U2_CCLK_SELECTMAP — A10
- U1_D3_SELECTMAP — A11
- U1_RDWR_SELECTMAP — A12
- U1_PUDC_B — A13
- U1_DOUT_CSO_B — A14
- PROCESSOR_I2C_SDA — A15
- PROCESSOR_I2C_SCL — A16

SEAF8-50-05.0-S-04-2-K JXA

I45 12V
- A50
- A49
- U2_DONE_B — A48
- U2_INIT_B — A47
- A46
- U1_DONE_B — A45
- U1_INIT_B — A44
- A43
- U1_CSI_ADV_B — A42
- U1_FWE_FCS2_B — A41
- A40
- U1_D9 — A39
- U1_D8 — A38
- A37
- U1_D7 — A36
- U1_D6 — A35
- A34
- A33
- U1_SPARE1_N — A32
- U1_SPARE1_P — A31
- A30
- A29
- U1_D5 — A28
- U1_D4 — A27
- A26

I20 I19

J6 SEAF8_JX1 50-05_0-S-04-2-K I58

I42 VCCO_1
- ZYNQ_PMBUS_SDA — B1
- ZYNQ_PMBUS_SCL — B2
- B3
- B4
- U2_SPARE2_P — B5
- U2_SPARE2_N — B6
- U2_PROGRAM_B — B7
- U2_D0_SELECTMAP — B8
- U2_D1_SELECTMAP — B9
- U2_D2_SELECTMAP — B10
- ZYNQ_JC_GCK_P — B11
- ZYNQ_JC_GCK_N — B12
- U2_D3_SELECTMAP — B13
- U2_RDWR_SELECTMAP — B14
- U2_PUDC_B — B15
- U2_DOUT_CSO_B — B16
- EXT_JC_SDA — B17

SEAF8-50-05.0-S-04-2-K JXB

I44 12V
- B50
- B49
- U4_DONE_B — B48
- U4_INIT_B — B47
- B46
- U3_DONE_B — B45
- U3_INIT_B — B44
- B43
- U2_CSI_ADV_B — B42
- U2_FWE_FCS2_B — B41
- B40
- U2_D9 — B39
- U2_D8 — B38
- B37
- U2_D7 — B36
- U2_D6 — B35
- B34
- U2_SPARE1_N — B33
- U2_SPARE1_P — B32
- B31
- B30
- U2_D5 — B29
- U2_D4 — B28
- B27
- EXT_JC_SCL — B26

I18 I17

J6 SEAF8_JX1 50-05_0-S-04-2-K I57

I40 VCCO_1
- MAIN_TMS — C1
- ZYNQ_JTAG_TDI — C2
- U3_SPARE2_P — C3
- U3_SPARE2_N — C4
- U3_PROGRAM_B — C5
- U3_D0_SELECTMAP — C6
- U3_D1_SELECTMAP — C7
- U3_D2_SELECTMAP — C8
- U3_CCLK_SELECTMAP — C9
- U4_CCLK_SELECTMAP — C10
- U3_D3_SELECTMAP — C11
- U3_RDWR_SELECTMAP — C12
- U3_PUDC_B — C13
- U3_DOUT_CSO_B — C14
- LOL* — C15
- JC_RST* — C16

SEAF8-50-05.0-S-04-2-K JXC

I126 I141 12V VCCO_2
- C50
- C49
- CC_RESET_OUT — C48
- C47
- C46
- C45
- C44
- C43
- U3_CSI_ADV_B — C42
- U3_FWE_FCS2_B — C41
- C40
- U3_D9 — C39
- U3_D8 — C38
- C37
- U3_D7 — C36
- U3_D6 — C35
- C34
- C33
- U3_SPARE1_N — C32
- U3_SPARE1_P — C31
- C30
- C29
- U3_D5 — C28
- U3_D4 — C27
- C26

10K R27 0.1W 1%

I16 I15

J6 SEAF8_JX1 50-05_0-S-04-2-K I59

VCCO_1

SEAF8-50-05.0-S-04-2-K JXD
- D1 MAIN_TCK
- D2 ZYNQ_JTAG_TDO
- D3
- D4
- D5 U4_SPARE2_P
- D6 U4_SPARE2_N
- D7
- D8 U4_PROGRAM_B
- D9 U4_D0_SELECTMAP
- D10
- D11 U4_D1_SELECTMAP
- D12 U4_D2_SELECTMAP
- D13
- D14 ZYNQ_OSC_GCK_P
- D15 ZYNQ_OSC_GCK_N
- D16
- D17
- D18
- D19 U4_D3_SELECTMAP
- D20 U4_RDWR_SELECTMAP
- D21
- D22 U4_PUDC_B
- D23 U4_DOUT_CSO_B
- D24
- D25 HEADER_SCL_1
- D26 HEADER_SDA_1
- D27
- D28
- D29 U4_D5
- D30 U4_D4
- D31
- D32 U4_SPARE1_N
- D33 U4_SPARE1_P
- D34
- D35 U4_D6
- D36 U4_D7
- D37
- D38 U4_D8
- D39 U4_D9
- D40
- D41 U4_FWE_FCS2_B
- D42 U4_CSI_ADV_B
- D43
- D44
- D45
- D46
- D47 SOM_PG_OUT
- D48
- D49
- D50

VCCO_2 I39

I14 I68

J7 SEAF8_JX2 50-05_0-S-04-2-K I60

I49 MGTAVTT

I50 MGTVCCAUX

SEAF8-50-05.0-S-04-2-K JXA
- A1
- A2 LED_CTRL1
- A3 LED_CTRL2
- A4
- A5 MODDEF0/CLKOUT
- A6 EXT_RES
- A7
- A8 MDINT
- A9 MODDEF2/MDC
- A10
- A11 MODDEF1/MDC
- A12 TXDIS/SRESET*
- A13
- A14 IPMC_USER_0_ZYNQ
- A15 IPMC_USER_1_ZYNQ
- A16
- A17 RXLOS/SIGDET
- A18 RESET_PHY
- A19
- A20
- A21 IPBUS_U2_P<2>
- A22 IPBUS_U2_N<2>
- A23
- A24 IPBUS_U4_P<2>
- A25 IPBUS_U4_N<2>
- A26

I28
- A50
- A49
- A48
- A47
- A46
- A45
- A44
- A43
- A42
- A41
- A40
- A39
- A38
- A37
- A36
- A35
- A34
- A33
- A32 TTC_DATA2_ZYNQ_N
- A31 TTC_DATA2_ZYNQ_P
- A30
- A29 MGTRX_BP_N
- A28 MGTRX_BP_P
- A27
- A26

I29

J7 SEAF8_JX2 50-05_0-S-04-2-K I61

I48 MGTAVTT

SEAF8-50-05.0-S-04-2-K JXB
- B1 HEADER_SCL_2
- B2 HEADER_SDA_2
- B3
- B4 IPMC_USER_2_ZYNQ
- B5 IPMC_USER_3_ZYNQ
- B6
- B7 CPLD_EXT<0>
- B8 CPLD_EXT<1>
- B9
- B10 CPLD_EXT<2>
- B11 CPLD_EXT<3>
- B12
- B13 CPLD_PWR_SEQ<0>
- B14 CPLD_PWR_SEQ<1>
- B15
- B16 CPLD_PWR_SEQ<2>
- B17 CPLD_PWR_SEQ<3>
- B18
- B19 IPBUS_U2_P<0>
- B20 IPBUS_U2_N<0>
- B21
- B22 IPBUS_U4_P<0>
- B23 IPBUS_U4_N<0>
- B24
- B25

I26
- B50
- B49
- B48
- B47
- B46
- B45
- B44
- B43
- B42
- B41
- B40
- B39
- B38
- B37
- B36
- B35
- B34
- B33 QUAD226_REFCLK_N
- B32 QUAD226_REFCLK_P
- B31
- B30
- B29
- B28
- B27 MGTTX_BP_N
- B26 MGTTX_BP_P

I27

J7 SEAF8_JX2 50-05_0-S-04-2-K I62

I47 MGTAVCC

SEAF8-50-05.0-S-04-2-K JXC
- C1
- C2 AVAGO_SCL_IN
- C3 AVAGO_SDA_IN
- C4
- C5
- C6 AVAGO_SCL_IN_1
- C7 AVAGO_SDA_IN_1
- C8
- C9 AVAGO_SCL_IN_2
- C10 AVAGO_SDA_IN_2
- C11
- C12 AVAGO_SCL_IN_3
- C13 AVAGO_SDA_IN_3
- C14
- C15 IPMC_USER_4_ZYNQ
- C16 IPMC_USER_5_ZYNQ
- C17
- C18 PMBUS_SDA
- C19 PMBUS_SCL
- C20
- C21 IPBUS_U1_P<2>
- C22 IPBUS_U1_N<2>
- C23
- C24 IPBUS_U3_P<2>
- C25 IPBUS_U3_N<2>
- C26

I23
- C50
- C49
- C48
- C47
- C46
- C45
- C44
- C43
- C42
- C41
- C40
- C39
- C38
- C37
- C36
- C35
- C34
- C33
- C32 TTC_DATA1_ZYNQ_N
- C31 TTC_DATA1_ZYNQ_P
- C30
- C29 ZYNQ_REFCLK1_N
- C28 ZYNQ_REFCLK1_P
- C27
- C26

I24

J7 SEAF8_JX2 50-05_0-S-04-2-K I63

I46 MGTAVCC

SEAF8-50-05.0-S-04-2-K JXD
- D1 IPMC_HA0
- D2 IPMC_HA1
- D3
- D4 SER_ID_MEZZ
- D5 SER_ID_TOPO
- D6
- D7 IPMC_HA2
- D8 IPMC_HA3
- D9
- D10 IPMC_HA4
- D11 IPMC_HA5
- D12
- D13 IPMC_USER_6_ZYNQ
- D14 IPMC_USER_7_ZYNQ
- D15
- D16 IPMC_HA6
- D17 IPMC_HA7
- D18
- D19 IPBUS_U1_P<0>
- D20 IPBUS_U1_N<0>
- D21
- D22 IPBUS_U3_P<0>
- D23 IPBUS_U3_N<0>
- D24
- D25
- D26 ZYNQ_REFCLK0_N
- D27 ZYNQ_REFCLK0_P
- D28
- D29
- D30
- D31
- D32
- D33
- D34
- D35
- D36
- D37
- D38
- D39
- D40
- D41
- D42
- D43
- D44
- D45
- D46
- D47
- D48
- D49
- D50

I25 I22

VCCO_2
- 1K R62 0.1W 1% — LED_CTRL1 4.7K R56 0.1W 1% — U280 BC846 — LED2 — LED2 GRN 0402 SMD
- 1K R63 0.1W 1% — LED_CTRL2 4.7K R57 0.1W 1% — U281 BC846 — LED8 — LED2 GRN 0402 SMD

J8 SEAF8_JX3 30-05_0-S-04-2-K I64

I138 VCCO_2
- 10K R25 0.1W 1% — CC_SCL — A1
- A2
- A3
- A4
- A5
- A6
- A7
- A8
- A9
- A10
- A11
- A12
- A13
- A14
- PS_ETH_MD2_P — A15

SEAF8-50-05.0-S-04-2-K JXA

I54 MGTRAVCC
- A30
- A29 MIO_51_SD_CLK
- A28 MGTAVTT_SENSE
- A27 MIO_49_SD_DAT3
- A26
- A25 MIO_47_SD_DAT1
- A24 MGTAVCC_SENSE
- A23 MIO_45_SD_CD
- A22 MUX_IN_SDA
- A21 MUX_RST
- A20
- A19 PS_ETH_MD4_N
- A18 PS_ETH_MD4_P
- A17
- A16 PS_ETH_MD2_N

I30 I31

J8 SEAF8_JX3 30-05_0-S-04-2-K I65

SEAF8-50-05.0-S-04-2-K JXB
- B1
- B2
- B3
- B4
- B5
- B6
- B7
- B8
- B9
- B10
- B11
- B12
- B13
- B14
- PS_ETH_MD1_P — B15

I52 MGTRAVCC

I53 MGTRAVTT
- B30
- B29
- B28 MIO_50_SD_CMD
- B27
- B26 MIO_48_SD_DAT2
- B25
- B24 MIO_46_SD_DAT0
- B23 MGTVCCAUX_SENSE
- B22 MIO_44_SD_WP
- B21 MUX_IN_SCL
- B20
- B19
- B18 PS_ETH_MD3_N
- B17 PS_ETH_MD3_P
- B16
- B15 PS_ETH_MD1_N

I32 I33

J8 SEAF8_JX3 30-05_0-S-04-2-K I167

I137 VCCO_2
- 10K R26 0.1W 1% — CC_SDA — C1
- C2
- C3
- C4
- C5
- C6
- C7
- C8 GTR_RX1_P
- C9 GTR_RX1_N
- C10
- C11
- C12 GTR_REFCLK1_P
- C13 GTR_REFCLK1_N
- C14
- C15

SEAF8-50-05.0-S-04-2-K JXC

I51
- C30
- C29 VCCO_1_SENSE
- C28 MIO_37_UART_RST*
- C27 MIO_35
- C26 MIO_33_UART_RX
- C25 MGTRAVTT_SENSE
- C24
- C23
- C22 MIO27_PMBUS_ALERT
- C21
- C20 ETH_PHY_LED0
- C19
- C18 ETH_PHY_LED1
- C17
- C16

I34 I35

J8 SEAF8_JX3 30-05_0-S-04-2-K I67

SEAF8-50-05.0-S-04-2-K JXD
- D1 GTR_TX1_P
- D2 GTR_TX1_N
- D3
- D4
- D5
- D6
- D7
- D8
- D9
- D10
- D11
- D12
- D13
- D14
- D15

I36
- D30 VCCO_1_SENSE_64
- D29
- D28 VCCO_2_SENSE
- D27
- D26 MIO_34
- D25 MIO_32_UART_TX
- D24 VCCO_2_SENSE_47
- D23
- D22
- D21
- D20 MGTRAVCC_SENSE
- D19 CC_INT_N
- D18
- D17
- D16

I37

NA R30 NA — VCCO_1_SENSE

NA R31

I51 VCCO_2

10K R28 0.1W 1%

VCCO_2

U228 DS2411

1K R233 0.1W 1% — SER_ID_MEZZ — DS2411 (VCC, DATA, GND)

1000pF C226

VCCO_1
- I168 IX4PFO IX4A_50_32
- NA R218
- NA R219
- J21: SOM_RESET_IN_N, HEADER_SCL_1, HEADER_SDA_1

VCCO_2
- NA R220
- NA R221
- J33: HEADER_SCL_2, HEADER_SDA_2

J34: ATCA_PWR_CTRL<0>, ATCA_PWR_CTRL<1>, I109

VCCO_2
- NA R43
- NA R44
- J4: ZYNQ_PMBUS_SCL, ZYNQ_PMBUS_SDA

VCCO_2
- NA R122
- NA R123
- J10: MIO_34, MIO_35, I166

VCCO_1 (1.80 V)
- +VCCO_HP_64
- +VCCO_HP_65
- 1V8

VCCO_2 (3.30 V)
- +VCCO_HD_47
- +VCCO_HD_48
- +VCCO_PSIO_501
- 3V3

NOTE: SOM PULL'S UP SOM_RESET_IN_N

U5 J-STD_020 — WS-TASV — 22.1 R24 0.1W 1% — SOM_RESET_IN_N — 1000pF C6

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: ULTRAZED

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 3 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

PHY

U71 VSC8221

VCCO_2 3V3A

MODDEF0/CLKOUT RXLOS/SIGDET 1V2_PHY_D 1V2_PHY_A

MGTTX_BP_P MGTTX_BP_N MGTRX_BP_P MGTRX_BP_N

A_MGTTX_BP_P A_MGTTX_BP_N A_MGTRX_BP_P A_MGTRX_BP_N

TDI_PHY TDO_PHY TMS_PHY TCK_PHY TRSTB_PHY RESET_PHY

EEDAT EECLK TXDIS/SRESET* MDINT MODDEF2/MDC MODDEF1/MDC CLKOUTMICRO/OSDIS*

A_PHY_0_P A_PHY_0_N A_PHY_1_P A_PHY_1_N A_PHY_2_P A_PHY_2_N A_PHY_3_P A_PHY_3_N

I85 PHY_0_P I86 PHY_0_N I81 PHY_1_P I73 PHY_1_N I71 PHY_2_P I66 PHY_2_N I65 PHY_3_P I64 PHY_3_N

USE A SINGLE GROUND FOR THESE COMPONENTS

XTAL_2 XTAL_1 ABM8 ABM8_25MHZ

CMODE0 CMODE1 CMODE2 CMODE3

LED4 LED5 LED6 LED2 GRN 0402 SMD

PLACE CLOSE TO PHY

IC4 TS3L501ERUAR

IC5 TS3L501ERUAR

QFN VDD=VCCO_2

J11 CPLD_EXT<4>

ETH_PHY_LED0 ETH_PHY_LED1 RJ45_LED0 RJ45_LED1

U58 J-STD_020 WS-TASV RESET_PHY

1_COMATEL U67

U82 RJ45 wuerth7499111121A RJ45_LED1 RJ45_LED0

L5 BLM31PG121SN1L L2 BLM31PG121SN1L L3 BLM31PG121SN1L L6 BLM21PG221SN1D

VCCO_1 (1.80 V)
+VCCO_HP_04
+VCCO_HP_05
VCCO_2 (3.30 V)
+VCCO_HP_47
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE PHY - IPBUS

DRAWING TITLE

JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

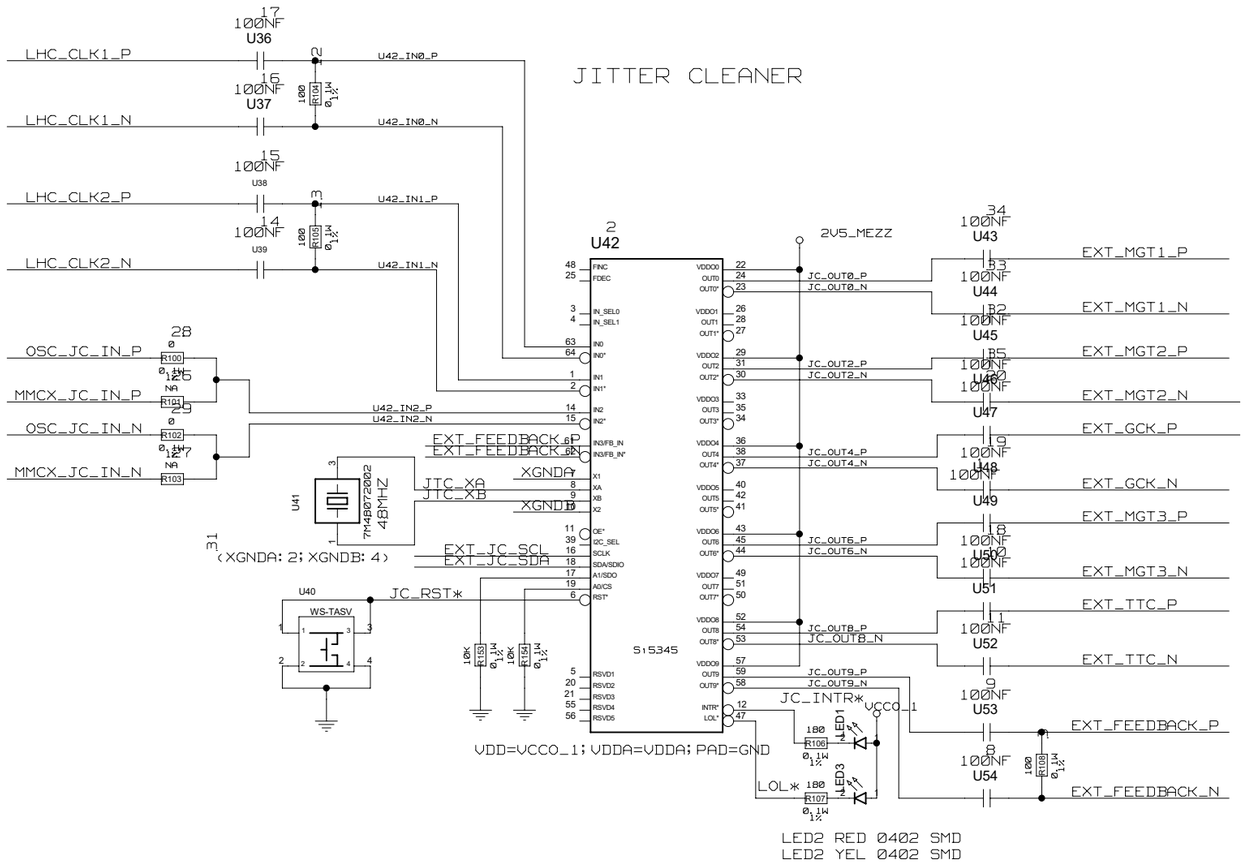
SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 4 OF 13

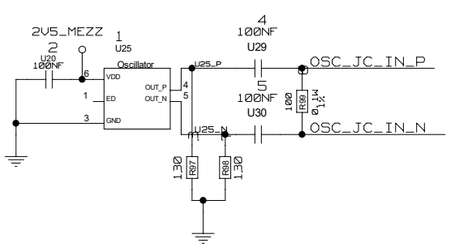
23

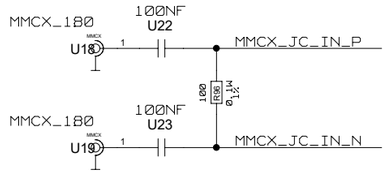
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

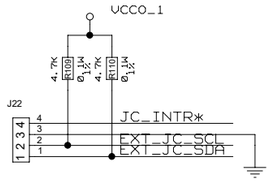
JITTER CLEANER

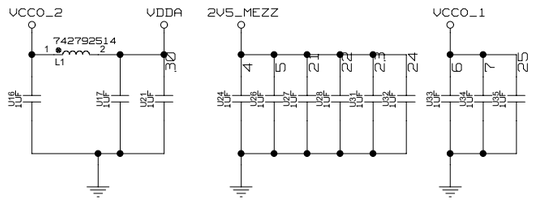


LED2 RED 0402 SMD
LED2 YEL 0402 SMD









VCCO_1 (1.80 V)
++VCCO_HP_D01
++VCCO_HP_D54
VCCO_2 (3.30 V)
++VCCO_HPD_47
++VCCO_HPD_48
++VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: JITTER CLEANER

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

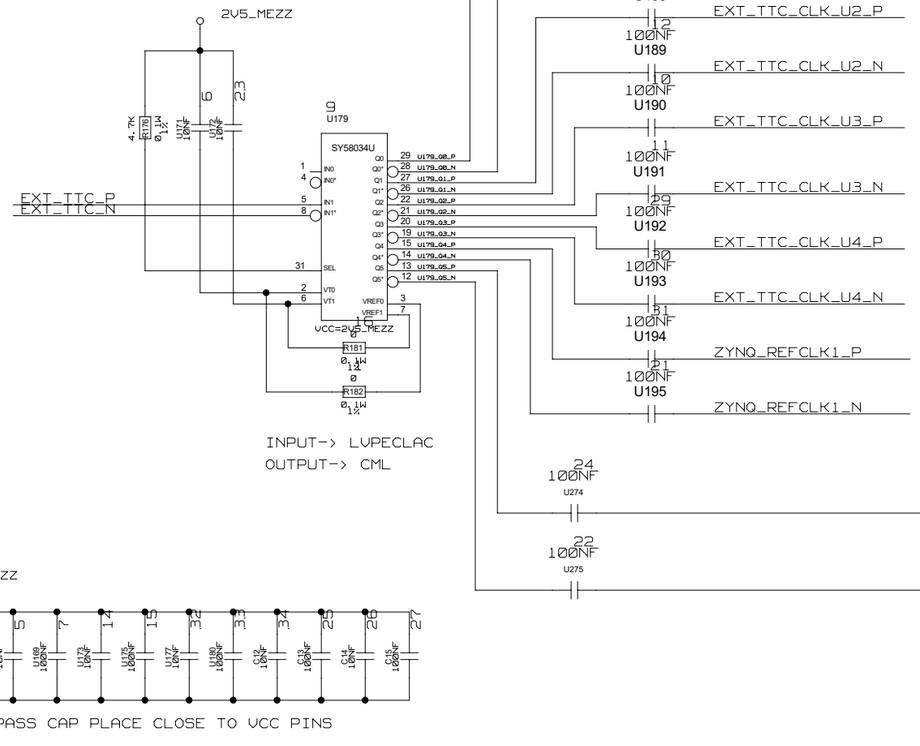
JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE: C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 5 OF 13

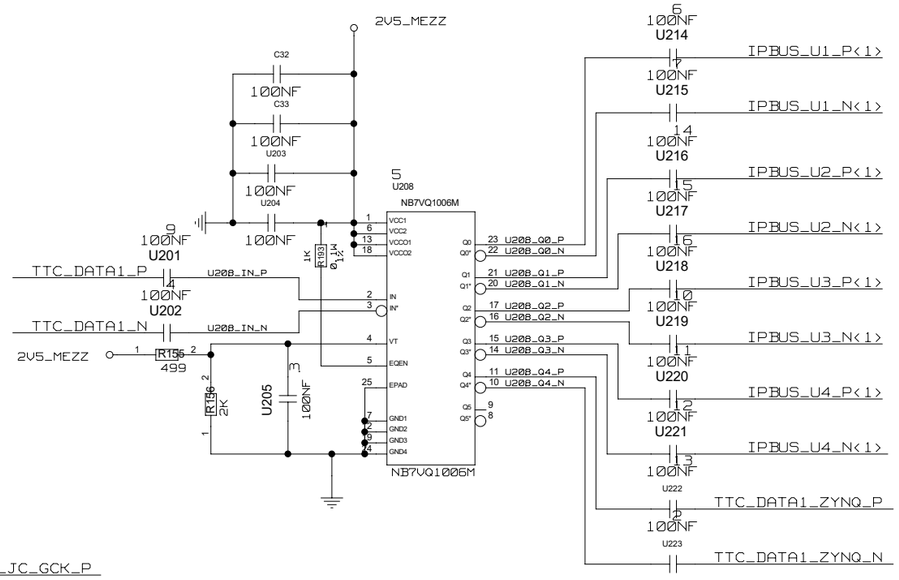
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

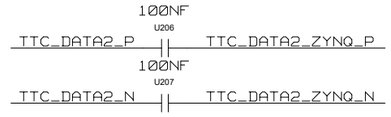
TTC DATA REFCLK



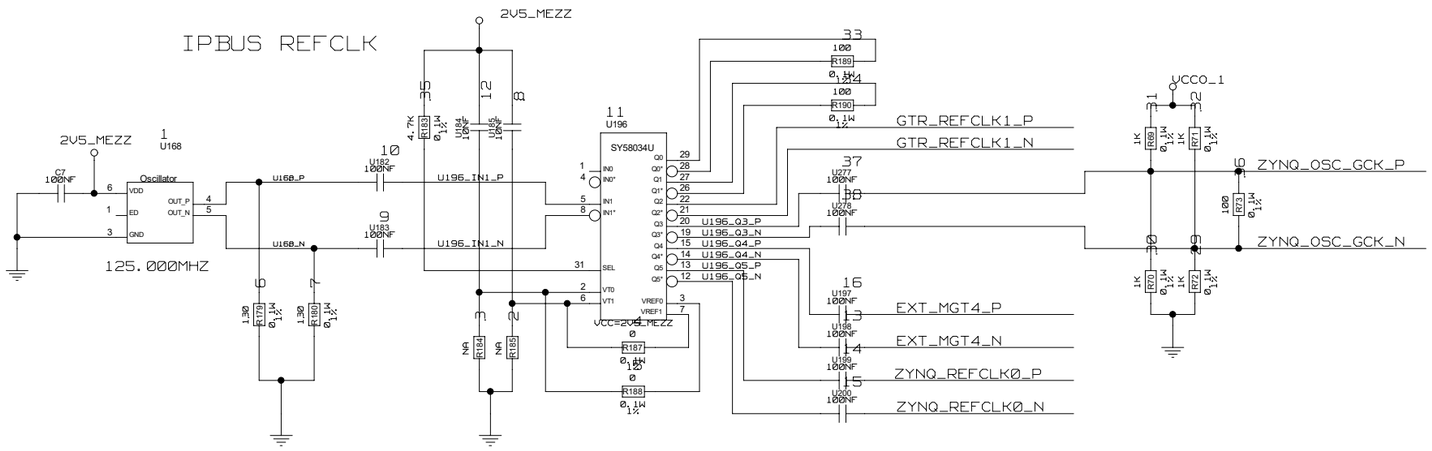
INPUT-> LVPECLAC
OUTPUT-> CML

TTC DATA FANOUT

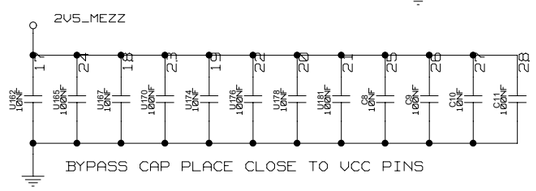




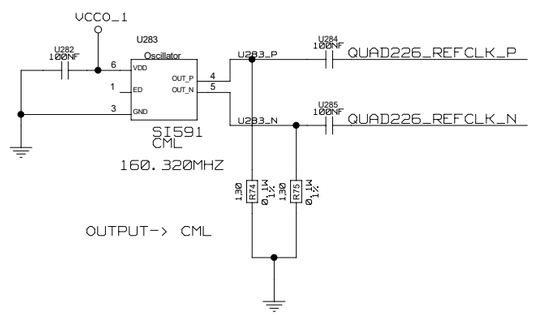
IPBUS REFCLK



INPUT-> LVPECLAC
OUTPUT-> CML



SPARE MGT REFCLK



OUTPUT-> CML

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: CLOCK DISTRIBUTION

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

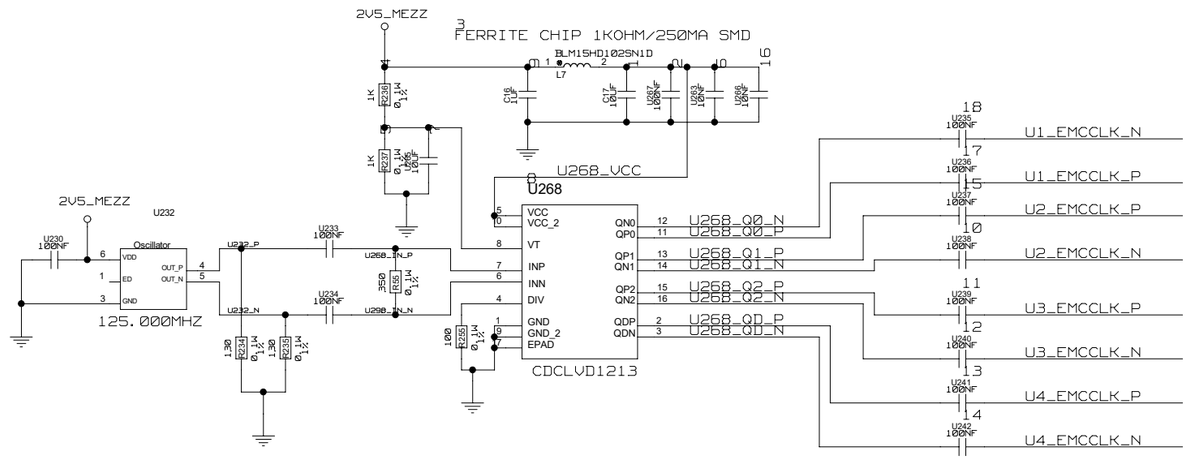
JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE: C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 6 OF 13

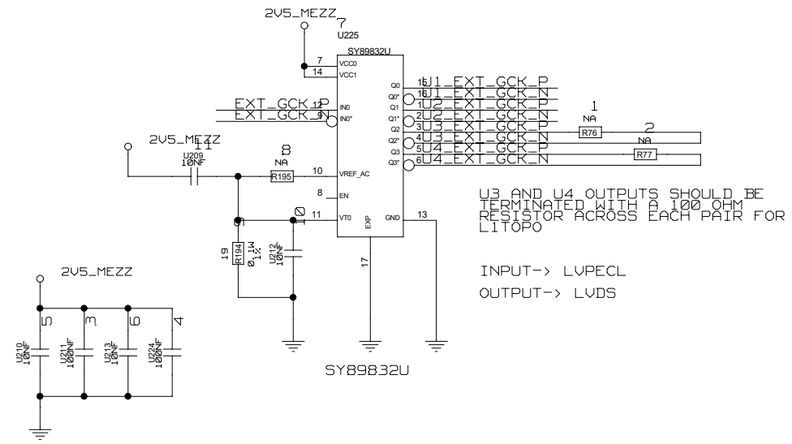
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

EXTERNAL MASTER CONFIGURATION CLOCK

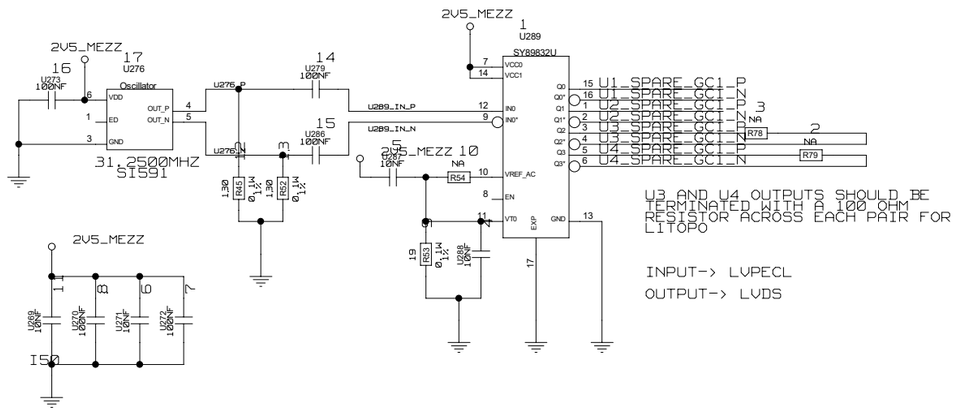


INPUT-> LVPECLAC
OUTPUT-> LVDS

CLEANED GLOBAL CLOCK



SPARE CLOCK TO PROCESSORS



VCCO_1 (1.80 V)
+VCCO_HP_54
+VCCO_HP_55
+VB
VCCO_2 (3.30 V)
+VCCO_HP_47
+VCCO_HP_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: CLOCK DISTRIBUTION

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

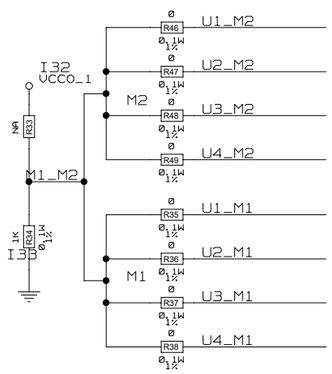
JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

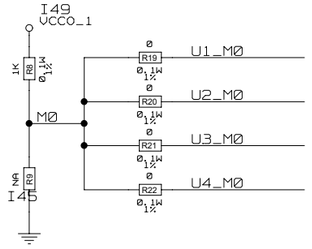
SCALE | SHEET 7 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

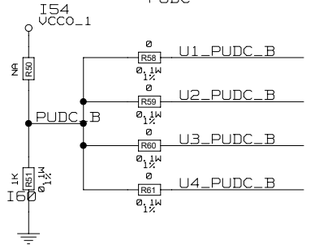
M1 & M2



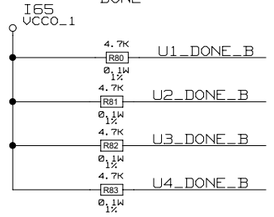
M0



PUDC



DONE



MASTER SPI	SLAVE SELECTMAP
M0 -> 1	M0 -> 0
M1 -> 0	M1 -> 1
M2 -> 0	M2 -> 1

U1_D0_SPI / U1_D0 / U1_D0_SELECTMAP

U1_D1_SPI / U1_D1 / U1_D1_SELECTMAP

U1_D2_SPI / U1_D2 / U1_D2_SELECTMAP

U1_D3_SPI / U1_D3 / U1_D3_SELECTMAP

U2_D0_SPI / U2_D0 / U2_D0_SELECTMAP

U2_D1_SPI / U2_D1 / U2_D1_SELECTMAP

U2_D2_SPI / U2_D2 / U2_D2_SELECTMAP

U2_D3_SPI / U2_D3 / U2_D3_SELECTMAP

U3_D0_SPI / U3_D0 / U3_D0_SELECTMAP

U3_D1_SPI / U3_D1 / U3_D1_SELECTMAP

U3_D2_SPI / U3_D2 / U3_D2_SELECTMAP

U3_D3_SPI / U3_D3 / U3_D3_SELECTMAP

U4_D0_SPI / U4_D0 / U4_D0_SELECTMAP

U4_D1_SPI / U4_D1 / U4_D1_SELECTMAP

U4_D2_SPI / U4_D2 / U4_D2_SELECTMAP

U4_D3_SPI / U4_D3 / U4_D3_SELECTMAP

U1_CCLK_SPI / U1_CCLK / U1_CCLK_SELECTMAP

U1_FCS_SPI / U1_RDWR_FCS_B / U1_RDWR_SELECTMAP

U2_CCLK_SPI / U2_CCLK / U2_CCLK_SELECTMAP

U2_FCS_SPI / U2_RDWR_FCS_B / U2_RDWR_SELECTMAP

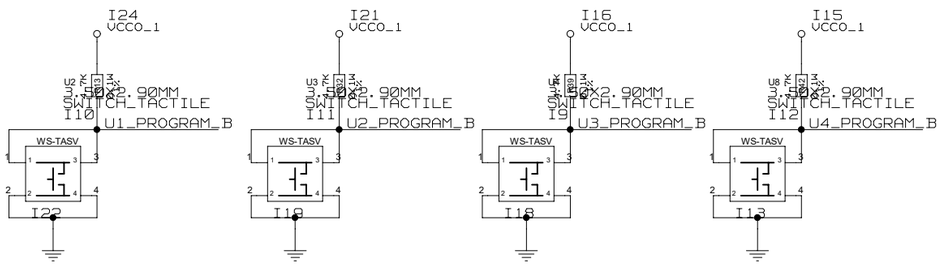
U3_CCLK_SPI / U3_CCLK / U3_CCLK_SELECTMAP

U3_FCS_SPI / U3_RDWR_FCS_B / U3_RDWR_SELECTMAP

U4_CCLK_SPI / U4_CCLK / U4_CCLK_SELECTMAP

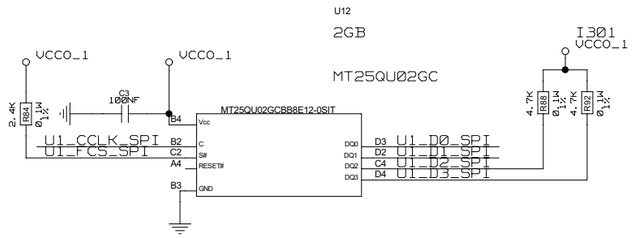
U4_FCS_SPI / U4_RDWR_FCS_B / U4_RDWR_SELECTMAP

PROGRAM_B



NET V3.0	NET JFEX
INIT_B	UN_CONF<11>
DONE	UN_CONF<12>
PROGRAM_B	UN_CONF<13>
M0	UN_CONF<14>
M1	UN_CONF<15>
M2	UN_CONF<16>
CCLK	UN_CONF<17>
D0	UN_CONF<18>
D1	UN_CONF<19>
D2	UN_CONF<20>
D3	UN_CONF<21>
RDWR_FCS_B	UN_CONF<22>
PUDC_B	UN_CONF<23>

SPI MEMORIES



VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: FPGA CONF

DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

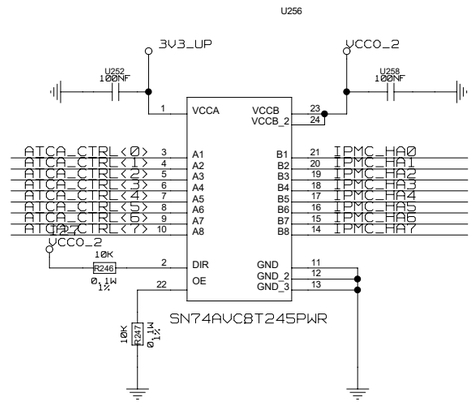
JOHANNES GUTENBERG UNIVERSITY MAINZ

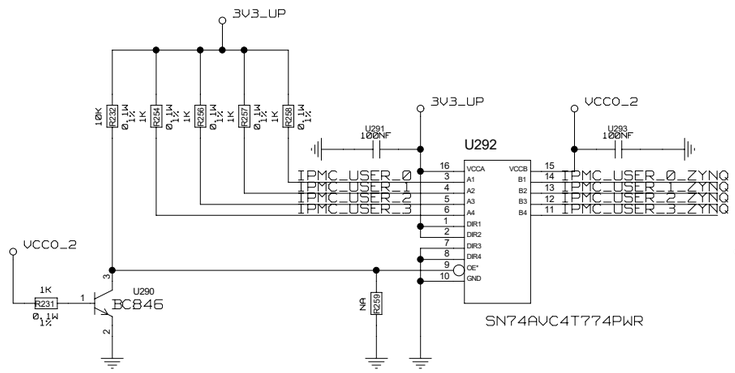
SIZE: C | REV. 3.0 | DRAWING NO.

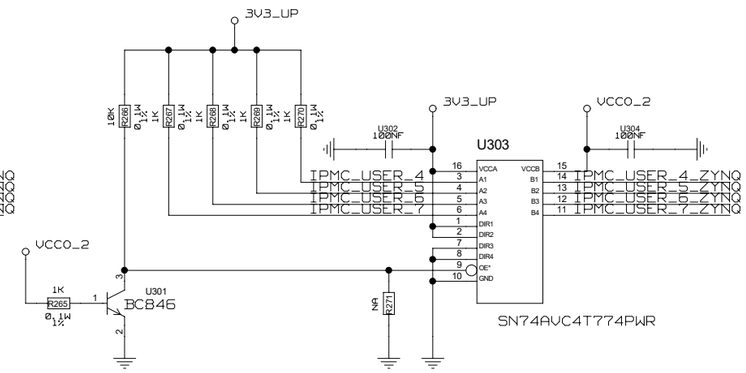
SCALE | SHEET 8 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

IPMC - LEVEL TRANSLATOR







	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	IPMC LEVEL TRANS		

DRAWING TITLE

JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

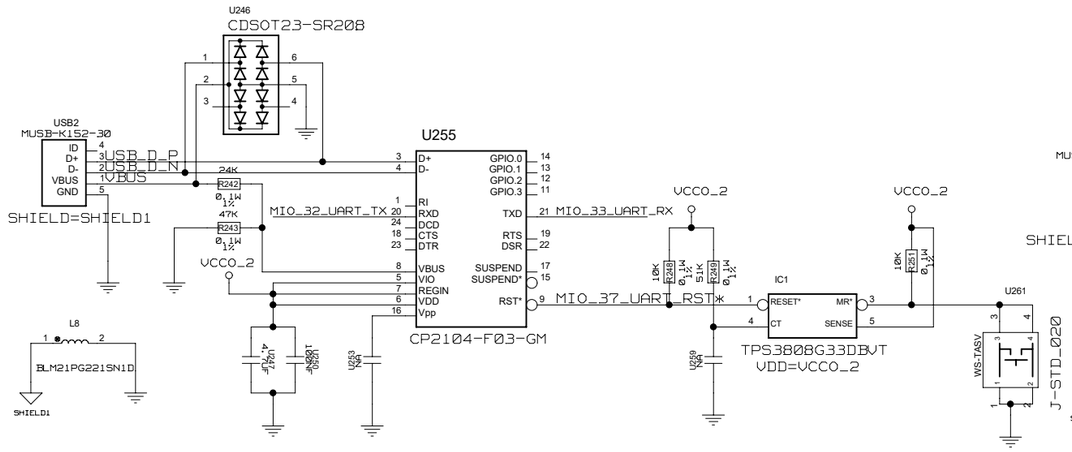
SIZE C | REV. 3.0 | DRAWING NO.

SCALE

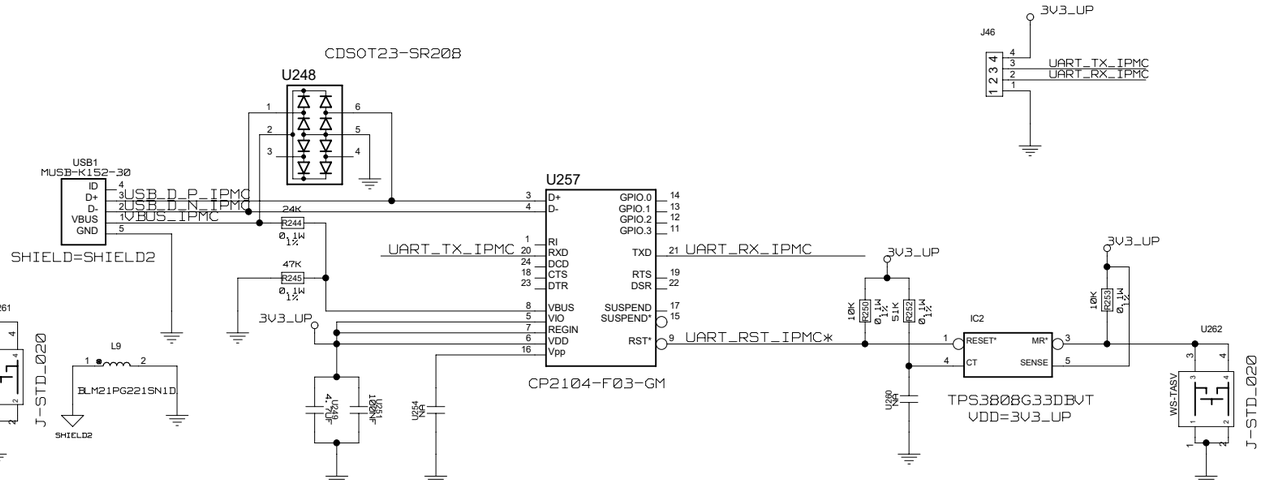
SHEET 9 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

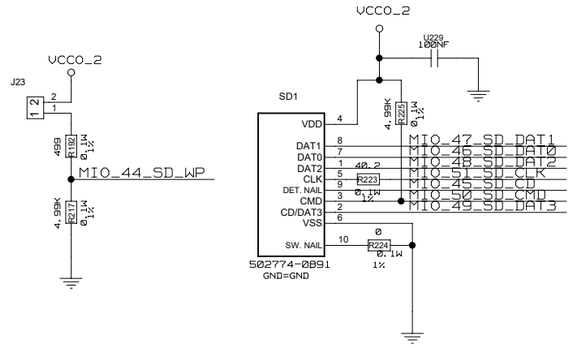
USB UART



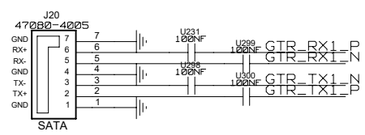
IPMC UART



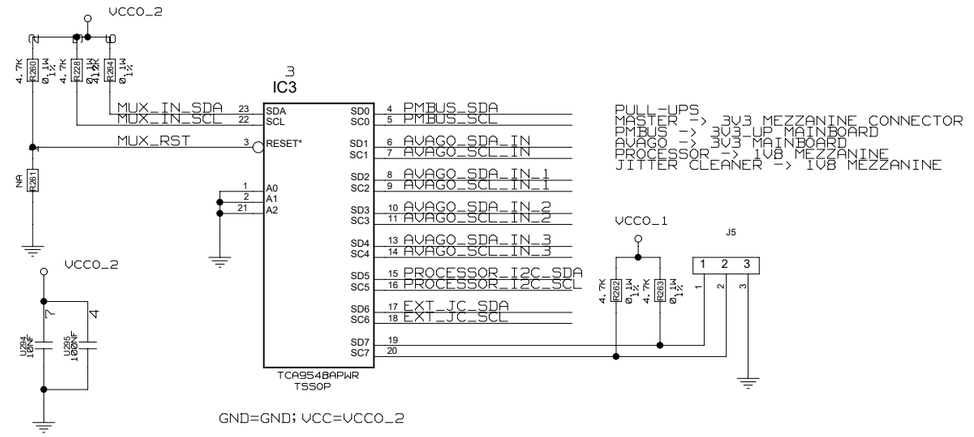
MICRO SD CARD



SATA INTERFACE



I2C - MUX



GND=GND; VCC=VCCO_2

VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE: UART, I2C MUX MICRO SD CARD

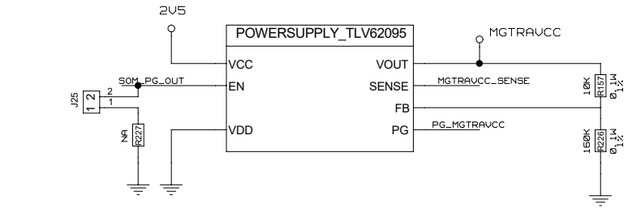
DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO. | SCALE | SHEET 10 OF 13

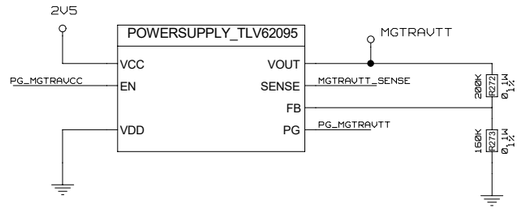
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

MGTRAVCC – 0.85V



NOTE:RES TO BE PLACED IF USING WITHOUT ULTRZED

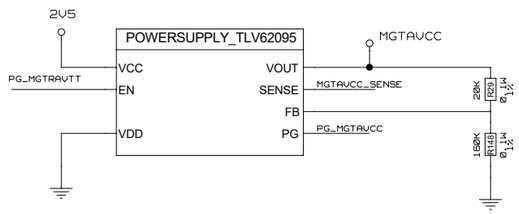
MGTRAVTT – 1.8V



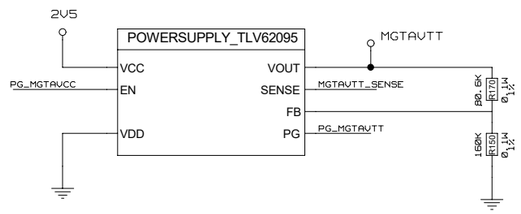
POWER SEQUENCING:
1- SOM_PG_OUT
2- PS_MGTRAVCC (0.85 V)
3- PS_MGTRAVTT (1.800 V)
4- PL_MGTAVCC (0.900 V)
5- PL_MGTAVTT (1.200 V)
6- PL_MGTVCCAUX (1.80 V)
7- VCCO_1 (1.80 V)
8- VCCO_2 (3.3 V)
9- 2V5 (2.5 V)

VCCO_1 (1.80 V)
+VCCO_HP_64
+VCCO_HP_65
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

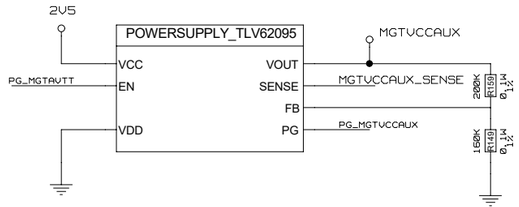
MGTAVCC – 0.9V



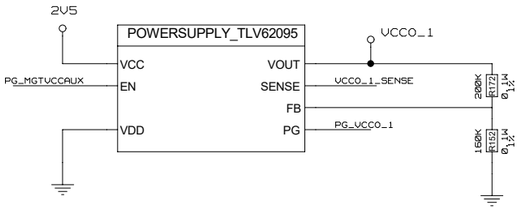
MGTAVTT – 1.2V



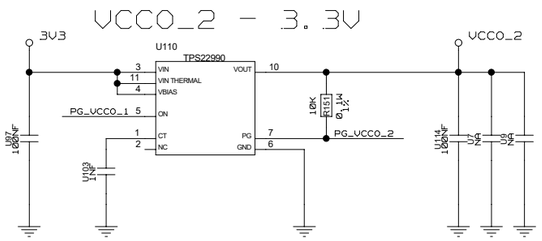
MGTVCCAUX – 1.8V



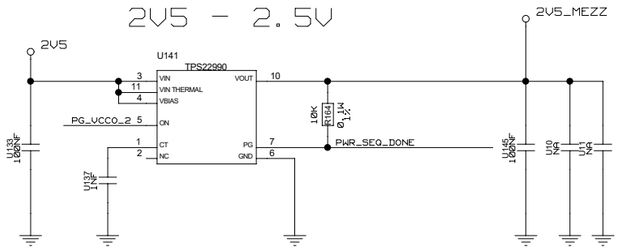
VCCO_1 – 1.8V

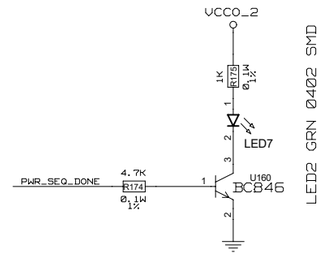


VCCO_2 – 3.3V

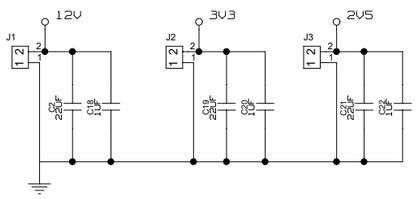


2V5 – 2.5V





EXTERNAL POWER (WITHOUT JFEX/TOPO)
MANUAL POWER UP (WITHOUT JFEX/TOPO)



	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	POWER		

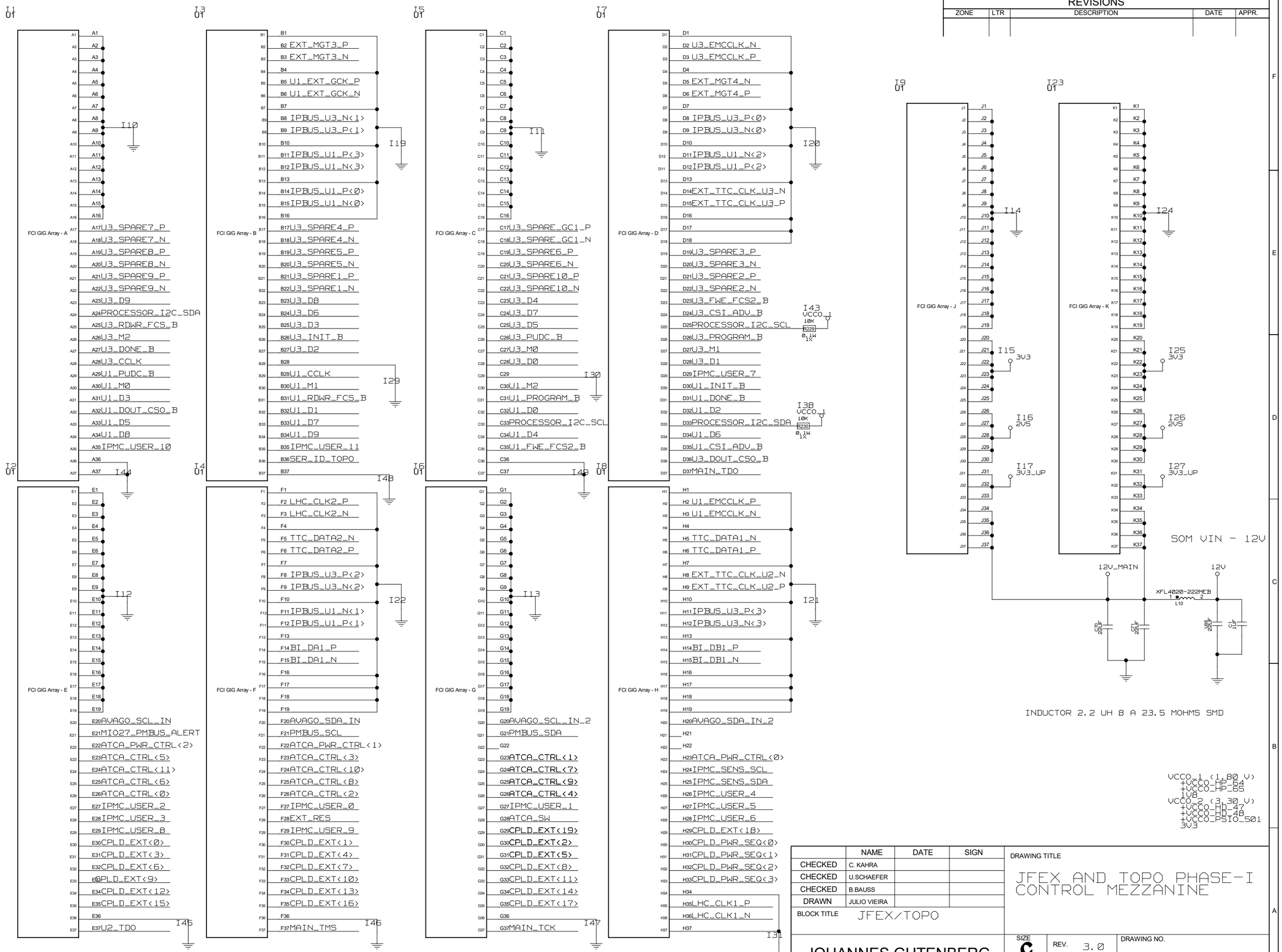
DRAWING TITLE: JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 11 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		
BLOCK TITLE	JFEX/TOPO		

DRAWING TITLE

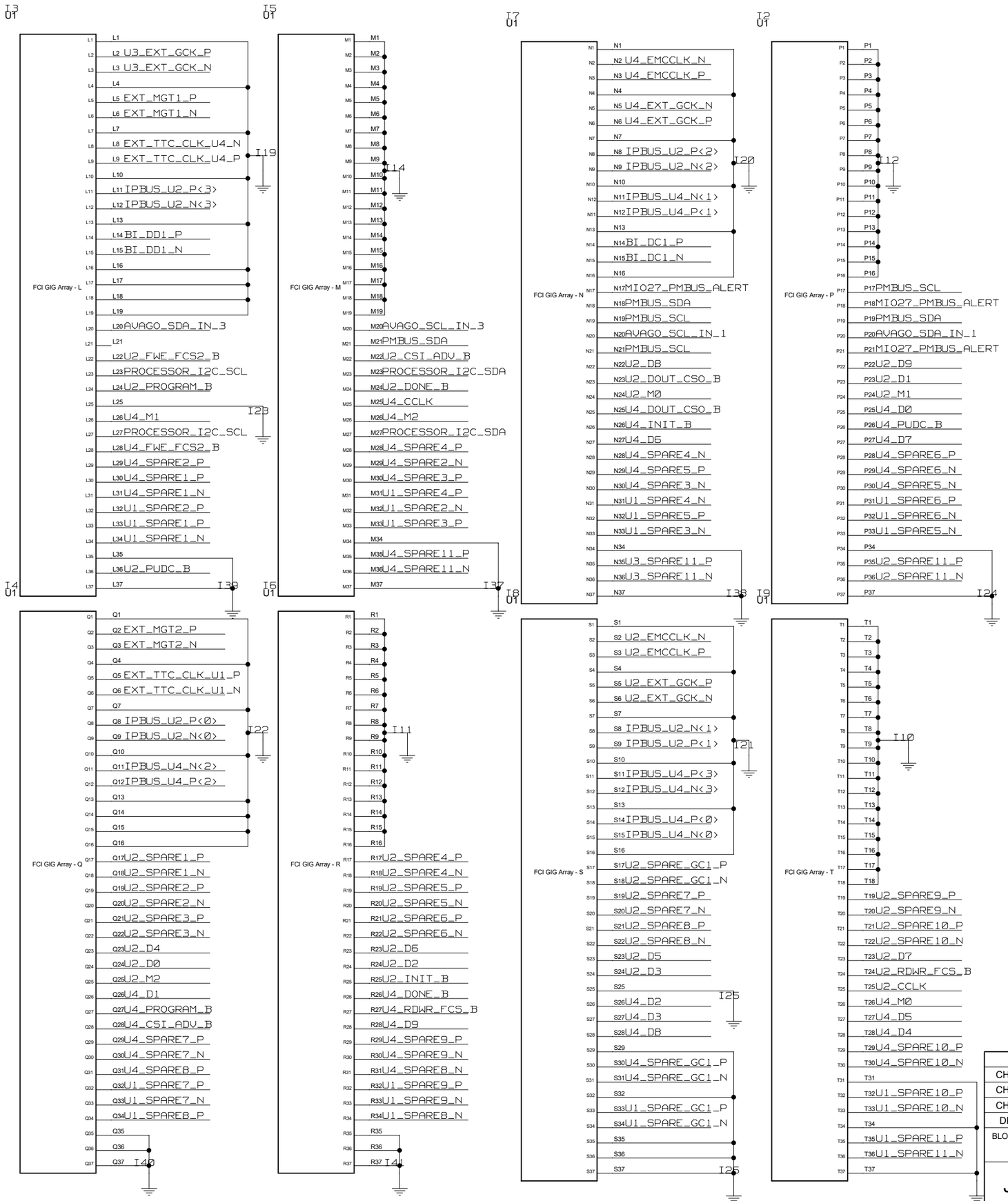
JFEX AND TOPO PHASE-I CONTROL MEZZANINE

JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE | SHEET 12 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



VCCO_1 (1.80 V)
+VCCO_HP_54
+VCCO_HP_55
1V8
VCCO_2 (3.30 V)
+VCCO_HD_47
+VCCO_HD_48
+VCCO_PSIO_501
3V3

	NAME	DATE	SIGN
CHECKED	C. KAHRA		
CHECKED	U.SCHAEFER		
CHECKED	B.BAUSS		
DRAWN	JULIO VIEIRA		

BLOCK TITLE JFEX/TOPO

DRAWING TITLE

JFEX AND TOPO PHASE-I CONTROL MEZZANINE

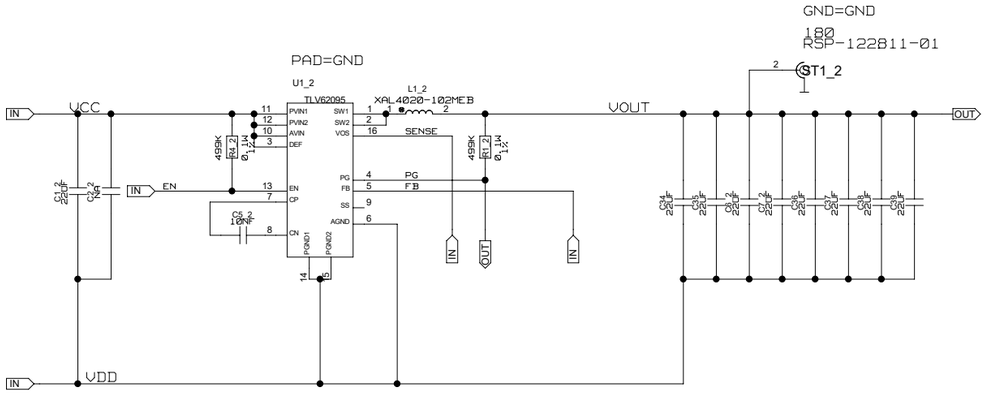
JOHANNES GUTENBERG UNIVERSITY MAINZ

SIZE C | REV. 3.0 | DRAWING NO.

SCALE

SHEET 13 OF 13

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS,INC.

CADENCE

DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF