CERN-IPMC: Hardware guide

The AdvancedTCA standard has been selected as one of the hardware platforms for the upgrades of the back-end electronics of the CMS and ATLAS experiments of the Large Hadron Collider. In this context, the CERN EP-ESE group has designed and produced an IPMC mezzanine card for the management of AdvancedTCA blades. This document describes in detail how to implement the CERN-IPMC module on a custom ATCA board.

Hardware document
v.1.0

Sources:

CERN-IPMC sharepoint - https://espace.cern.ch/ph-dep-ESE-BE-ATCAEvaluationProject/PP_IPMC
Support e-mail – julian.mendez@cern.ch

1. Introduction

The commercial IPMC solution from Pigeon Point System was adapted to answer the needs defined by the CERN-IPMC specification. To be compliant with already designed AdvancedTCA blades, the DIMM-DDR3 VLP form factor and connector pinout[1] previously defined by the solution developed at LAPP were used.

The mezzanine card was designed to support the functions defined by the AdvancedTCA rev. 3.0 standard (hotswap, sensor monitoring, etc.), up to 8 AMCs and 1 intelligent-RTM, an Ethernet interface with RMCP/RCMP+, TCP/IP subset and UDP protocols, a serial interface for debug or Serial Over LAN (SOL), up to 51 user I/Os and a JTAG master that can be accessed via a Xilinx Virtual Cable server. Figure 1 shows a typical use of the CERN-IPMC where all of the interfaces are implemented.

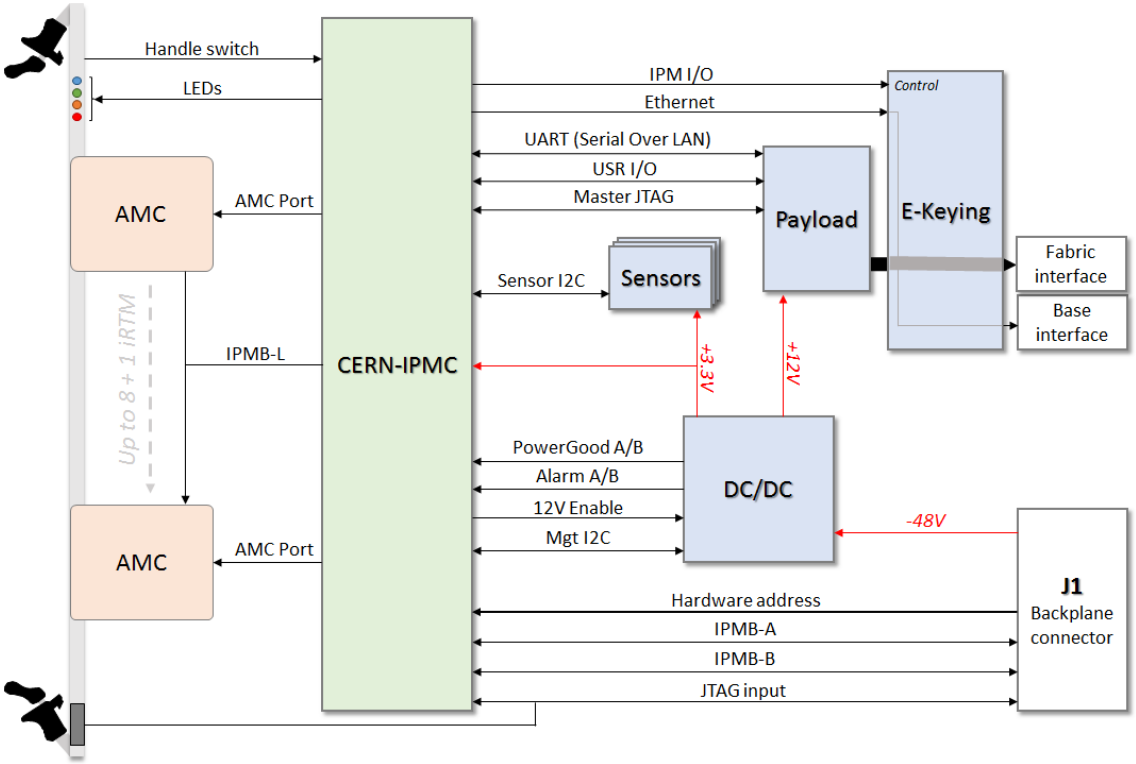

Figure 1: Typical use of the CERN-IPMC

[1] DIMM-DDR3 VLP connector pinout and signals mapping in firmware: https://espace.cern.ch/ph-dep-ESE-BE-ATCAEvaluationProject/PP_IPMC/Public%20documents/CERN-IPMC%20-%20Pinout%20and%20mapping.pdf

2. Hardware

The CERN-IPMC architecture is mainly defined by the use of a SmartFusion FPGA. This Microsemi device provides all of the interfaces required and runs the firmware application on its embedded ARM Cortex M3 processor. Figure 2 shows the complete architecture of the CERN-IPMC mezzanine card.

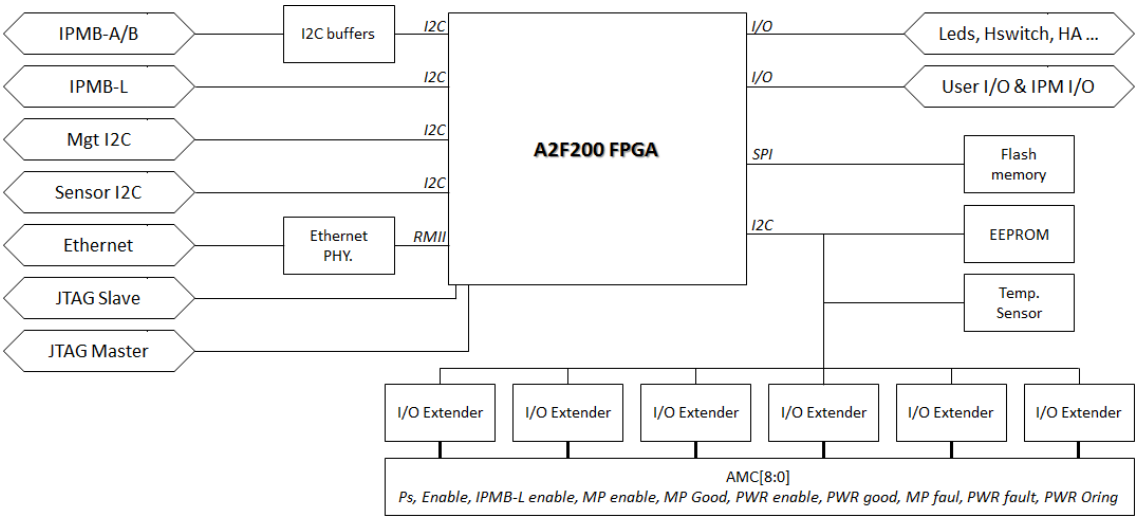

Figure 2: Hardware architecture

2.1 Backplane connector (Zone 1)

The backplane connector (Zone 1) provides the interfaces required for the communication between the on-board controller and the shelf manager (shown in Figure 3).

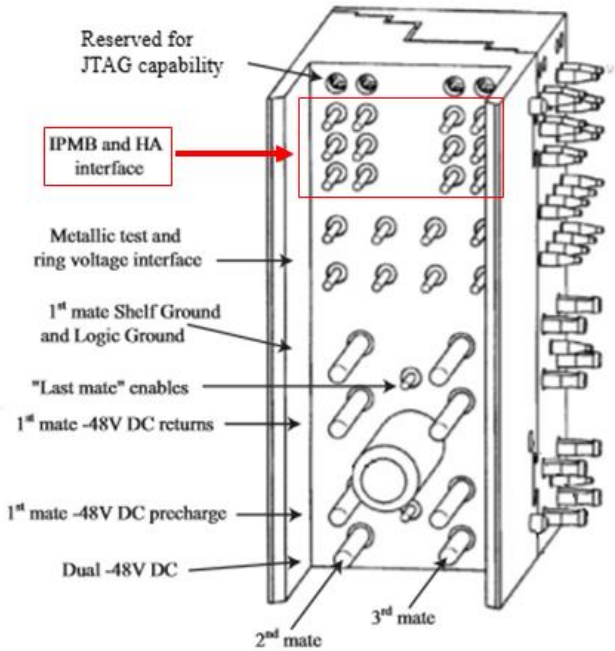

Figure 3: Backplane (Zone 1) connector

The required capacitors and resistors for the Hardware address signals defined by REQ 2.298 and REQ 2.299 of the AdvancedTCA R3.0 standard and the I2C buffers for IPMB buses used to ensure safe insertion/extraction processes are already implemented on the mezzanine card. Therefore, the signals can be directly routed from the IPMC DIMM-DDR3 VLP connector to the backplane as shown in Figure 4.

IPMC	Backplane	Designation	Description	Explanation
115	5	HA0	HA0 Hardware Address Bit 0	Hardware Address Bits read by the IPMC
237	6	HA1	HA1 Hardware Address Bit 1	
116	7	HA2	HA2 Hardware Address Bit 2	
238	8	HA3	HA3 Hardware Address Bit 3	
117	9	HA4	HA4 Hardware Address Bit 4	
239	10	HA5	HA5 Hardware Address Bit 5	
118	11	HA6	HA6 Hardware Address Bit 6	
240	12	HA7/P	HA7/P Hardware Address Bit 7 (Odd Parity Bit)	
120	13	SCL_A	IPMB Clock, Port A	IPMB Connection Port A
121	14	SDA_A	IPMB Data, Port A	
242	15	SCL_B	IPMB Clock, Port B	IPMB Connection Port B
243	16	SDA_B	IPMB Data, Port B	

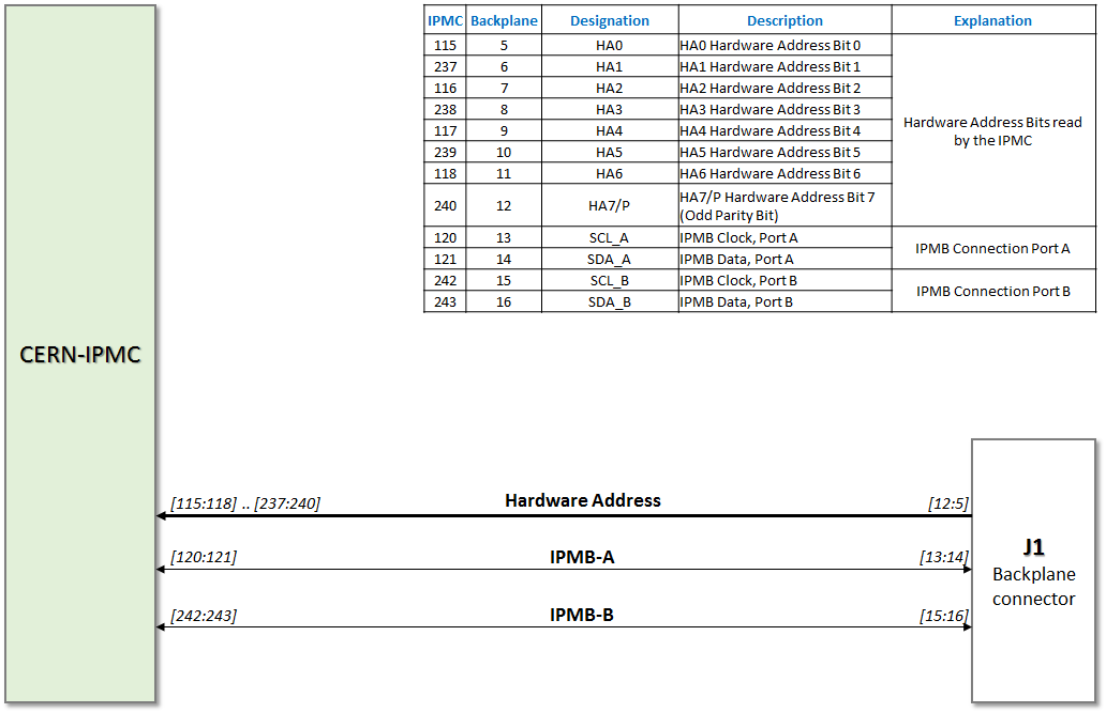

Figure 4: Zone1 interfaces connectivity

2.2 Front panel

A few signals, connected to the front panel, are used to get the handle switch state and to provide status (LEDs). By default, the IPMC waits for a low value on the “handle switch” signal to start the Power ON sequence and send a Power OFF request to the Shelf manager when the signal goes back to a high value. The line must be pulled-up to the reference voltage (3.3Volts) with a 10k resistor on the blade. De-bouncing is done in firmware. The LEDs are directly connected to controller I/Os and driven by a 3.3V output except the Blue LED signals, which is boosted by a TPS61070 to provide a 5V output. Figure 5 shows how the interfaces must be routed.

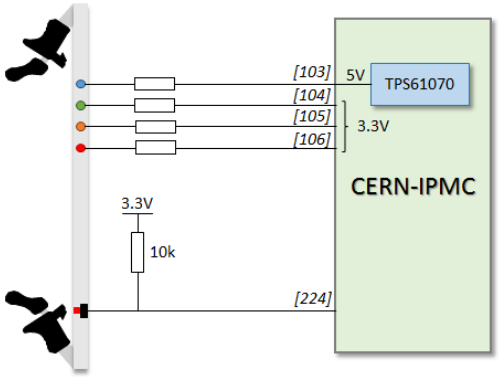

Figure 5: Front pannel features connectivity

2.3 Power management

The power management of the AdvancedTCA blade, carried out by the IPMC, is made using specific pins and the Mgt I2C bus available on the IPMC DIMM connector. Figure 6 shows a successfully tested implementation.

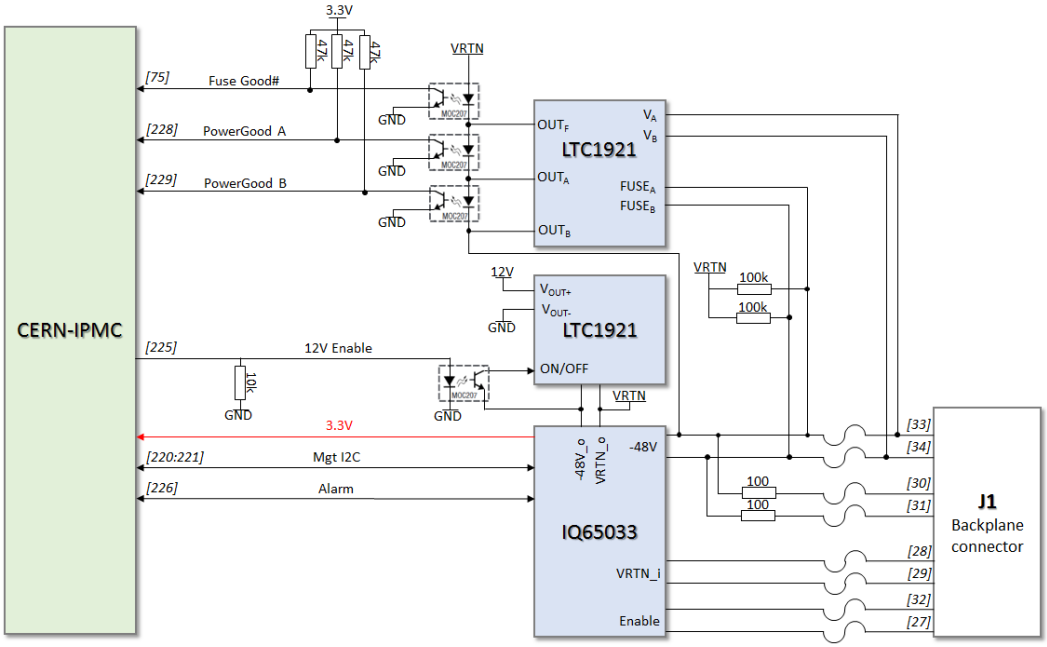

Figure 6: Power management example design

2.4 JTAG slave

The JTAG slave interface is used to configure the FPGA located on the IPMC mezzanine card using a FlashPro4 JTAG programmer. Figure 7 shows a possible connectivity of the JTAG slave interface to a front panel connector.

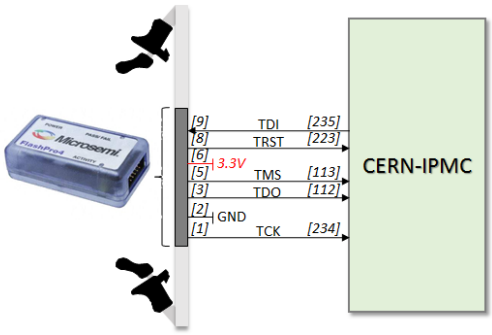

Figure 7: JTAG slave interface connectivity

2.5 JTAG master

The JTAG master interface, available on the CERN-IPMC mezzanine card is made of GPIO that runs JTAG commands at 5MHz. All of the pins are directly connected to controller I/Os (3.3V) with neither any additional pull-up/down nor capacitors. The connectivity between the ATCA on-board device and the JTAG master interface of the IPMC has to be handled by the user.

Note: *This feature has been successfully tested with Xilinx FPGA only.*

2.6 Ethernet

The Ethernet 10/100MBps interface can be used for multiple purposes. The lines available on the connector are ready to be connected to an RJ45 connector or to a switch (TS3L110), which can be used to provide a dual connectivity (Backplane and front panel). The required pull-up (3.3V) and the transceiver PHY are already located on the CERN-IPMC mezzanine card. Figure 8 shows a connectivity example for the Ethernet interface.

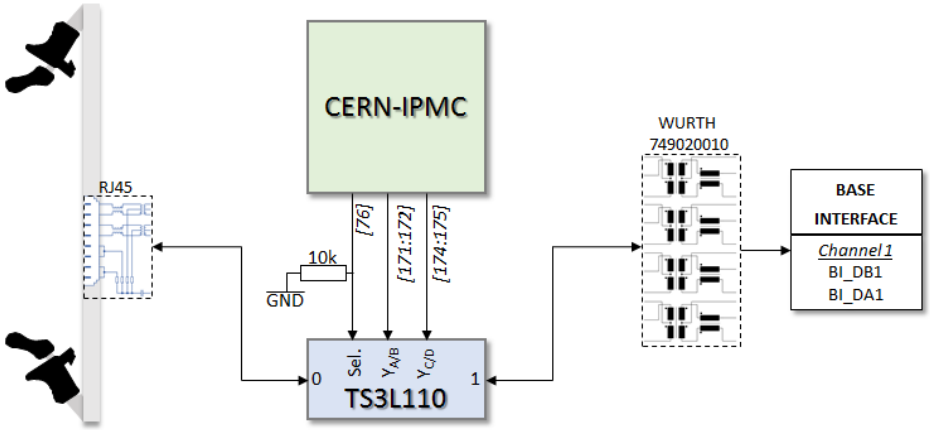

Figure 8: Ethernet connectivity

2.7 AMC/iRTM support

The CERN-IPMC supports up to 8 AMCs and 1 intelligent RTM through a set of signals available on the connector. In addition, several power management devices have been successfully tested (TPS2358/TPS2458, TPS2459 and LTC4222) but the controller must be able to control almost all of the components recommended for the AMC support. Finally, to ensure the hotswap compliance, I2C buffers must be implemented on the IPMB-L bus for each slot to avoid communication issues during the insertion/extraction processes. Figure 9 shows an implementation example for an AMC slot powered through a TPS2459 device.

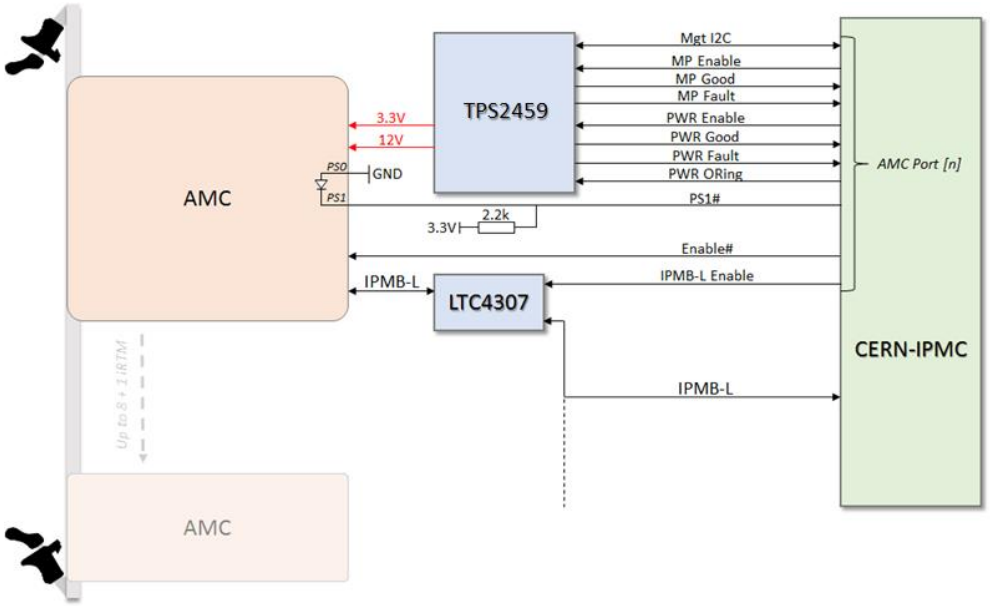

Figure 9: AMC implementation example based on a TPS2459 device