

REVISIONS				
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FFEX CONTROL MEZZANINE

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JTAG CHAIN

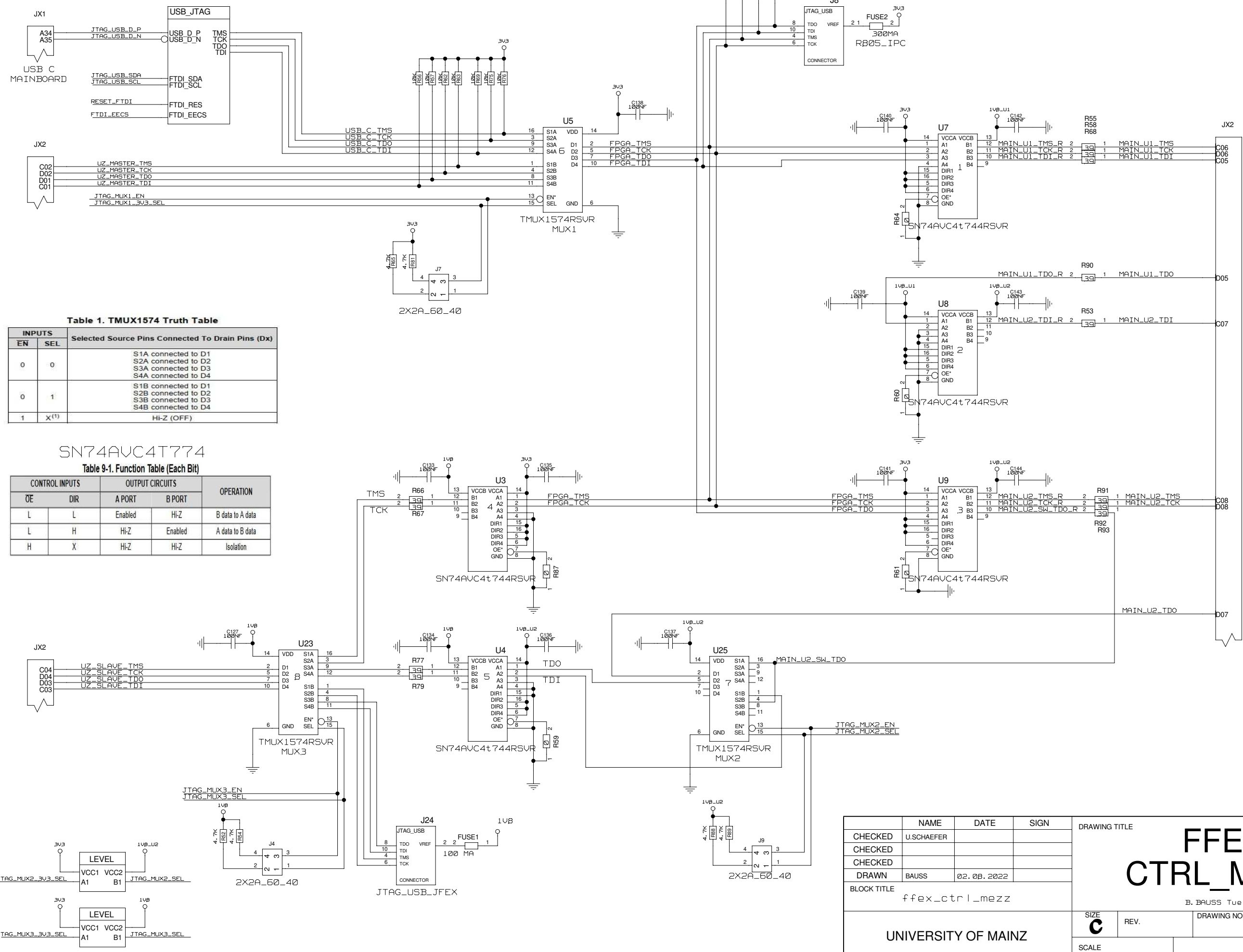


Table 1. TMUX1574 Truth Table

INPUTS		Selected Source Pins Connected To Drain Pins (Dx)
EN	SEL	
0	0	S1A connected to D1 S2A connected to D2 S3A connected to D3 S4A connected to D4
0	1	S1B connected to D1 S2B connected to D2 S3B connected to D3 S4B connected to D4
1	X ⁽¹⁾	Hi-Z (OFF)

SN74AUC4T774

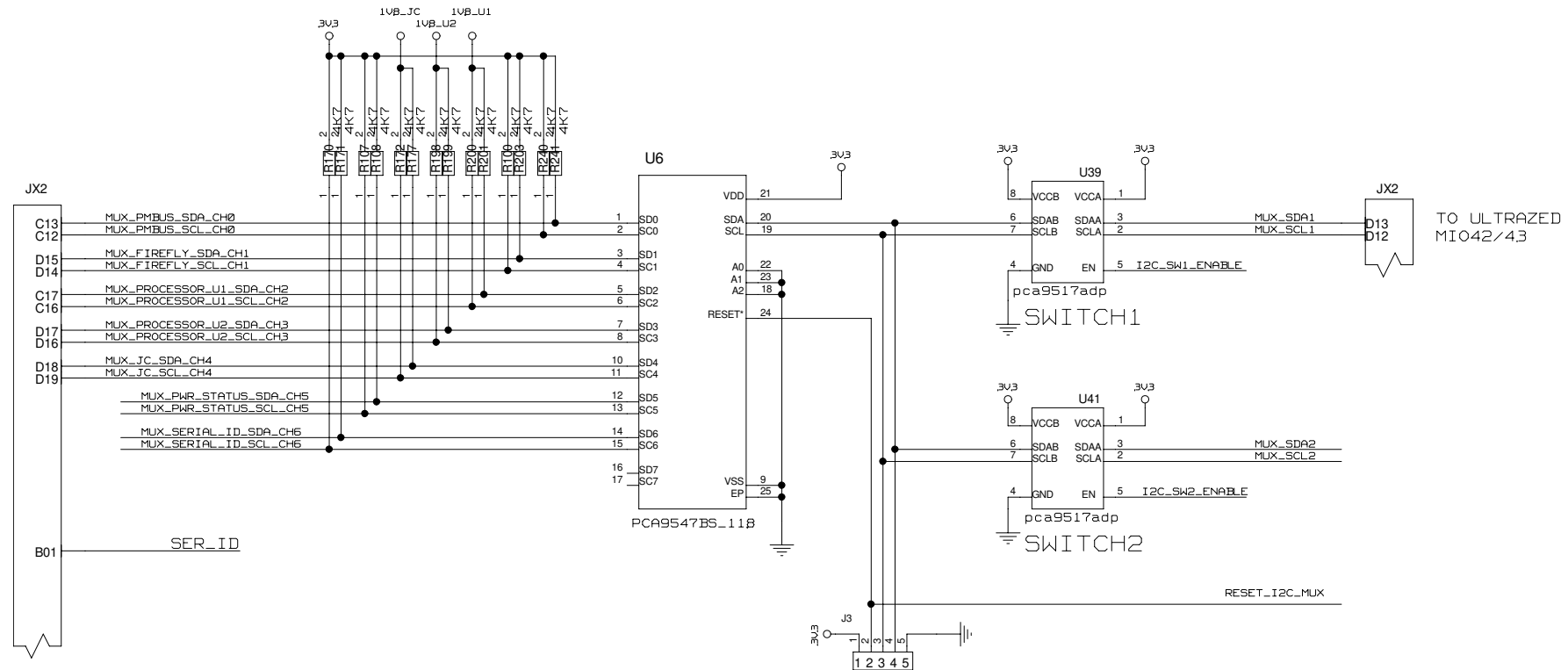
Table 9-1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

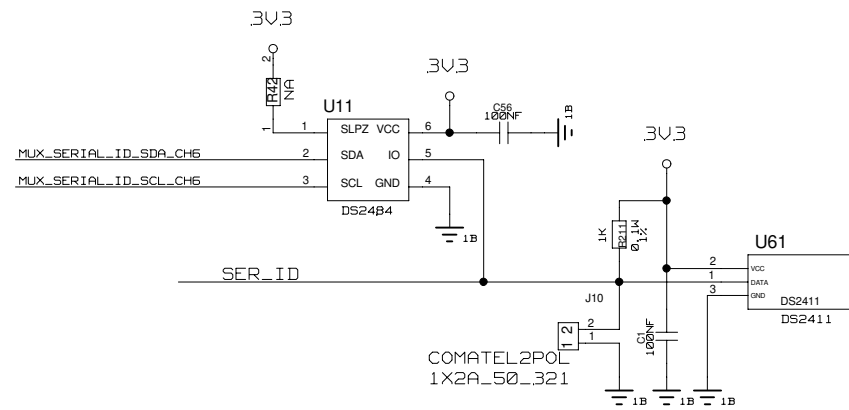
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I2C MULTIPLEXER



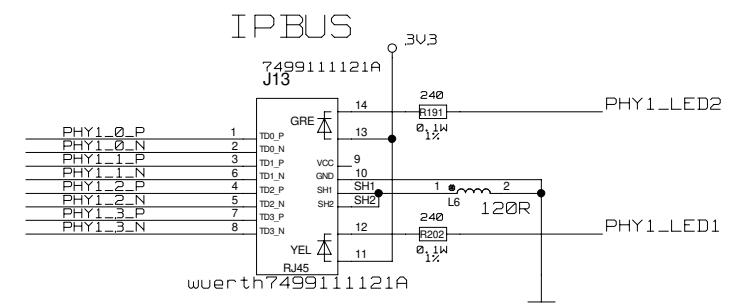
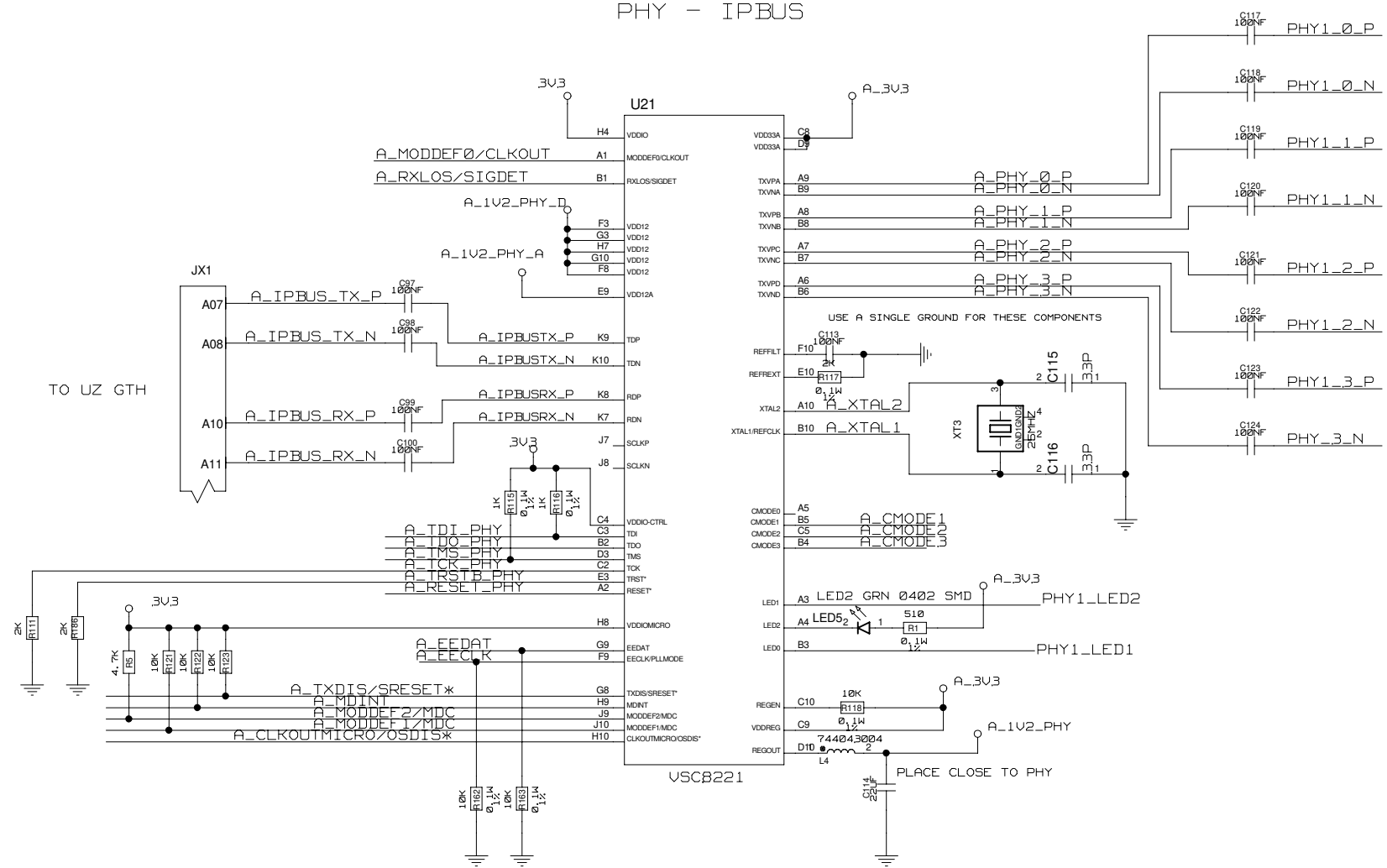
SERIAL BOARD ID



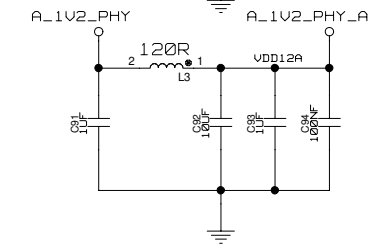
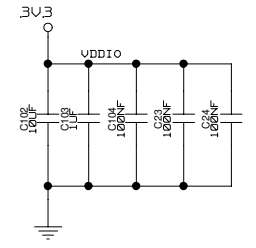
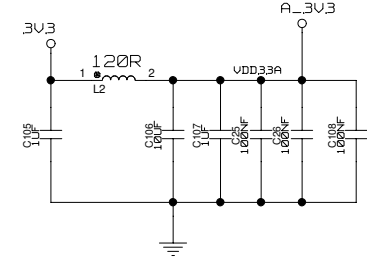
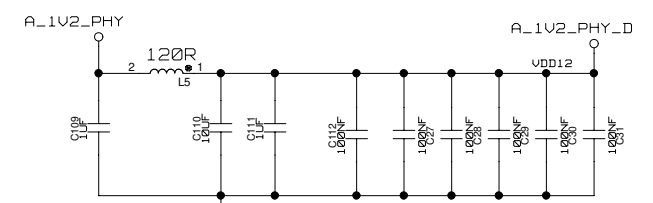
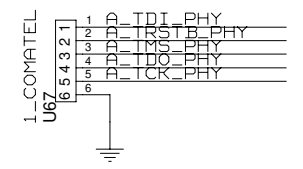
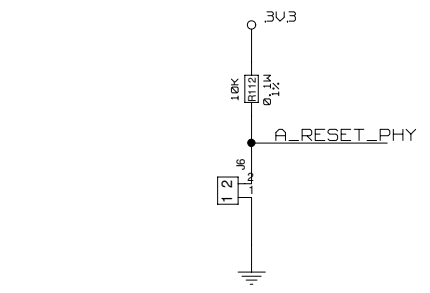
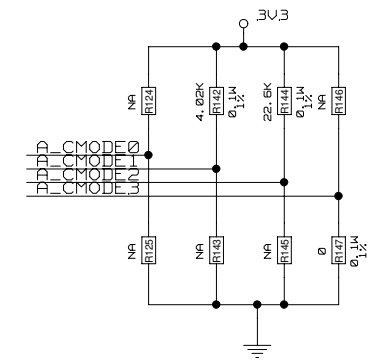
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PHY1
PHY - IPBUS



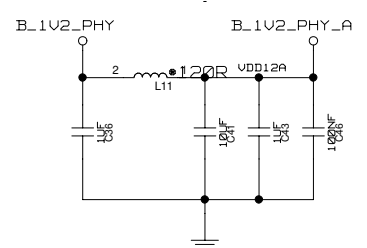
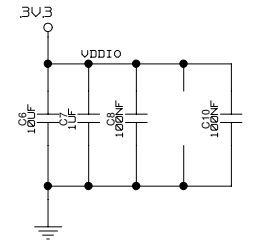
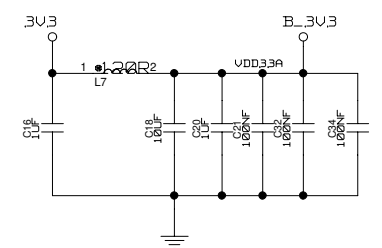
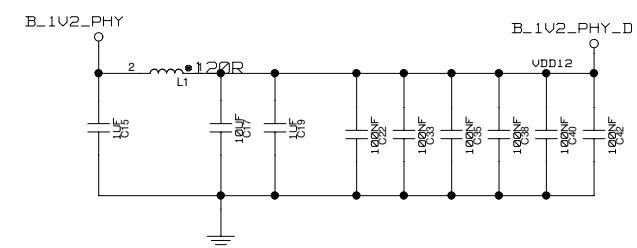
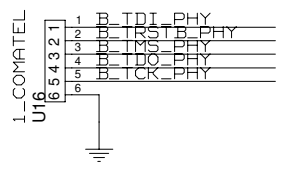
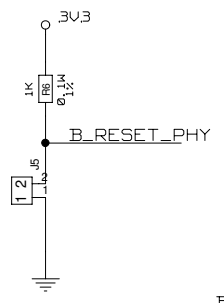
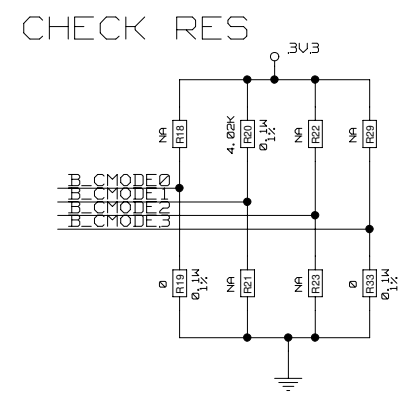
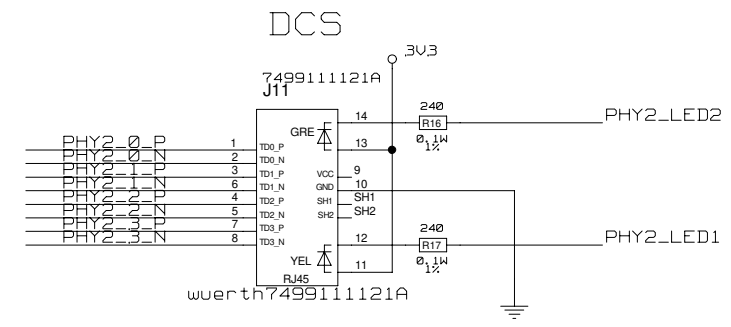
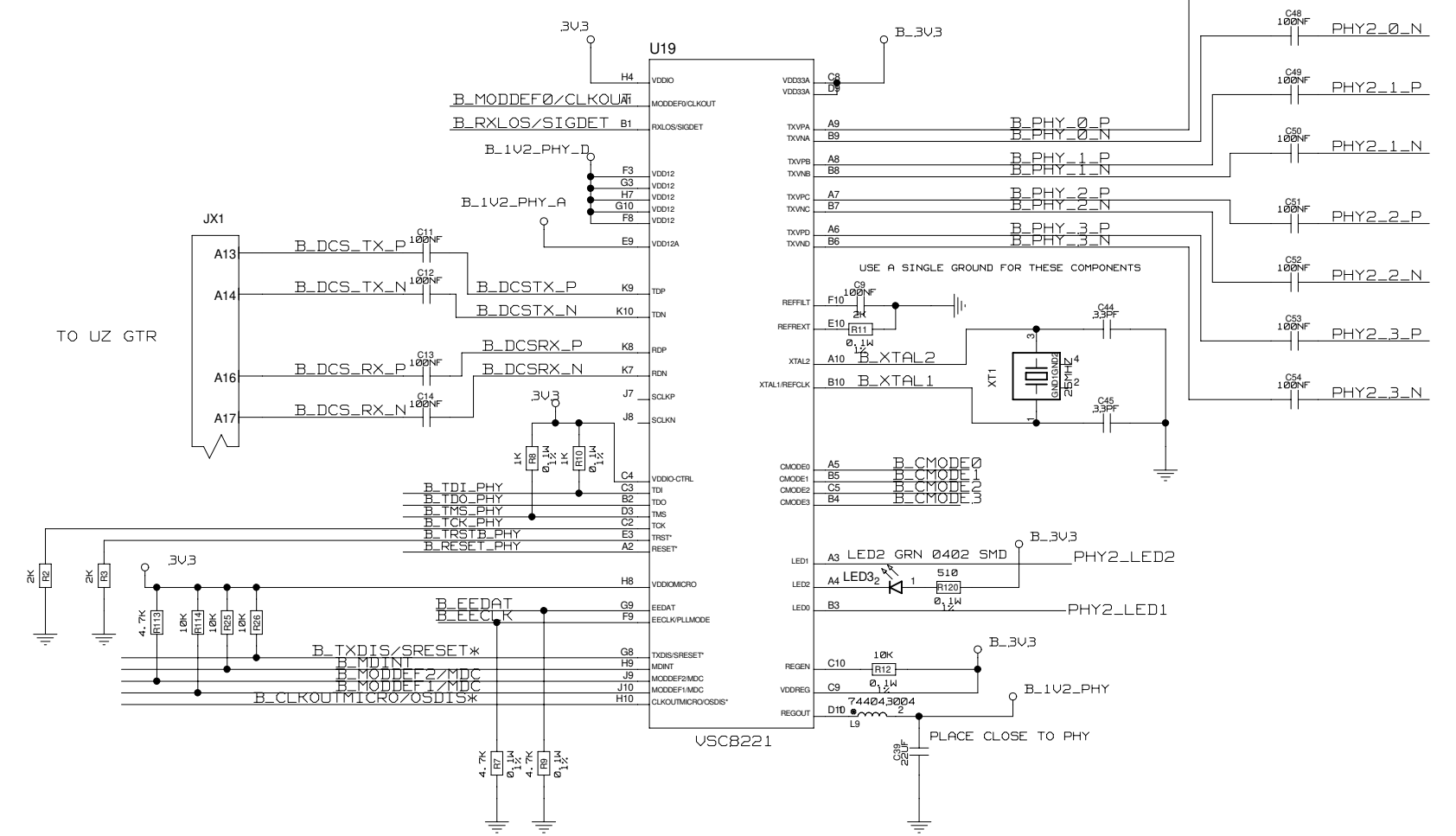
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PHY2
PHY - DCS

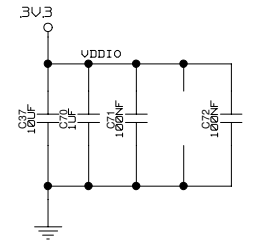
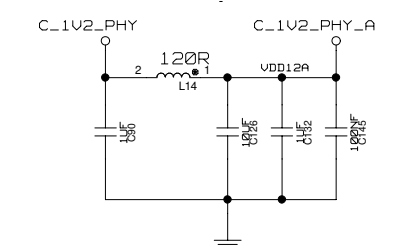
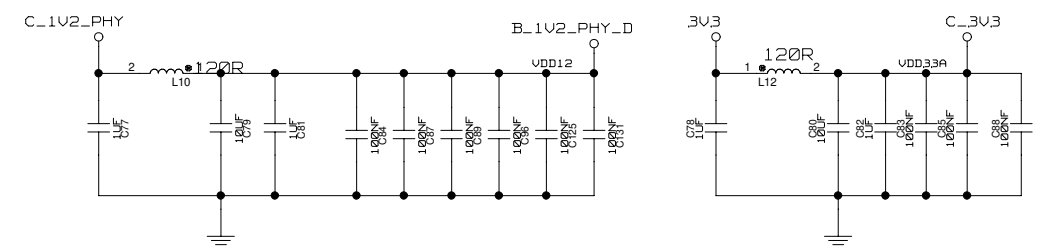
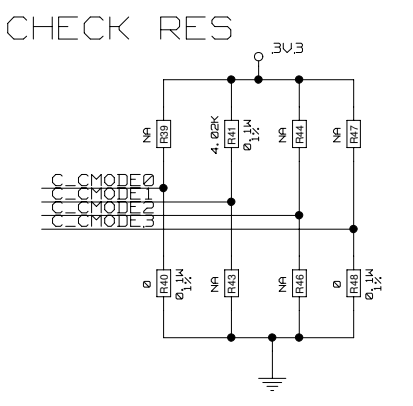
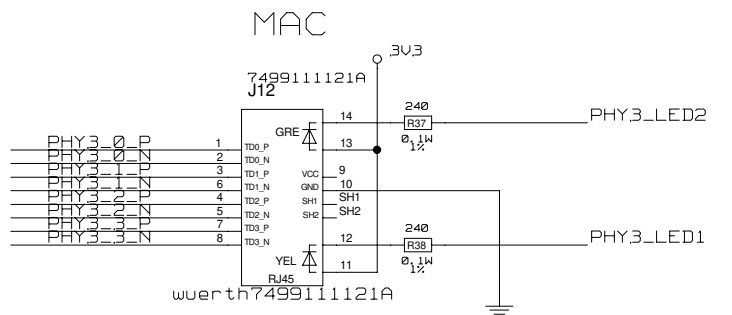
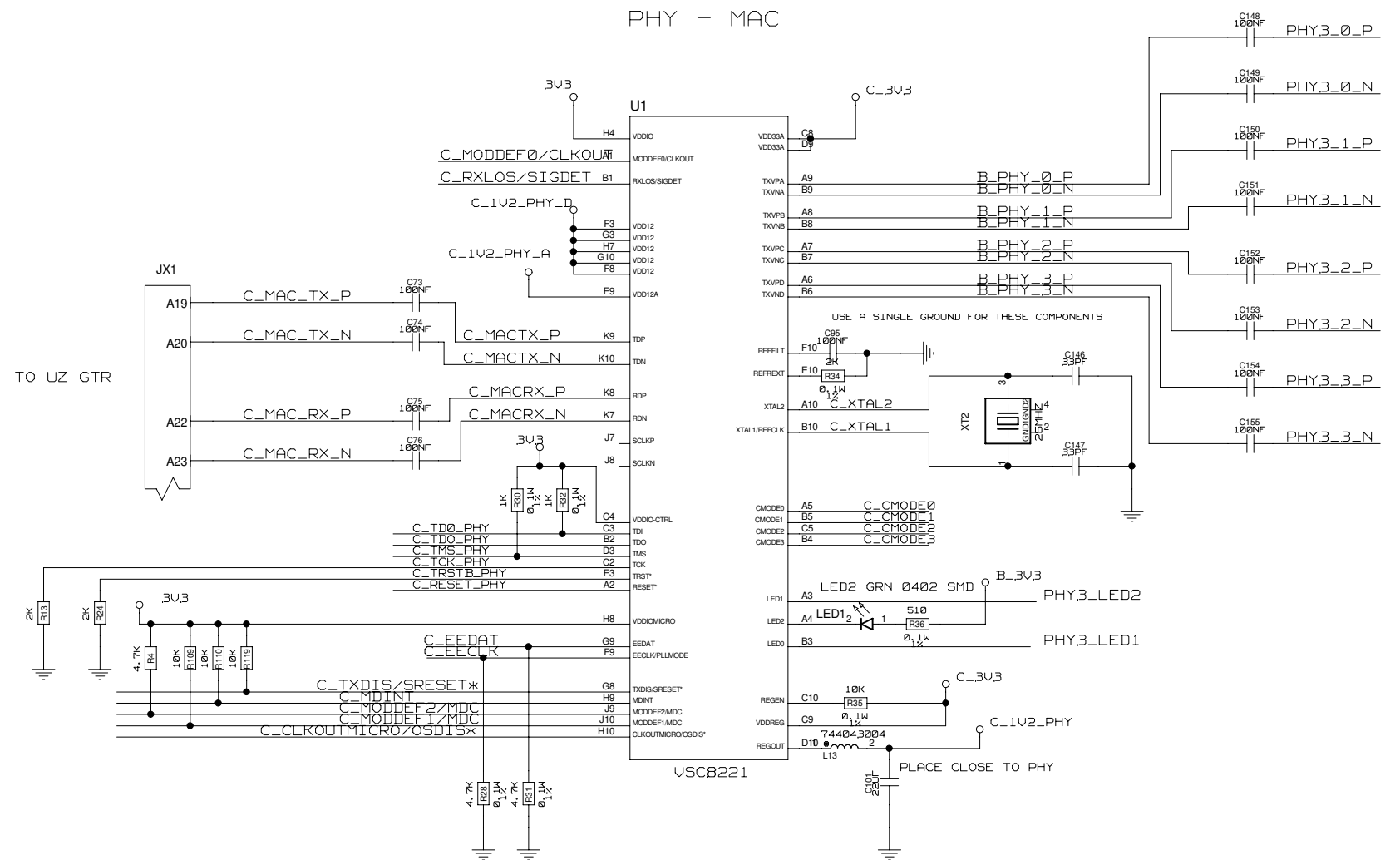


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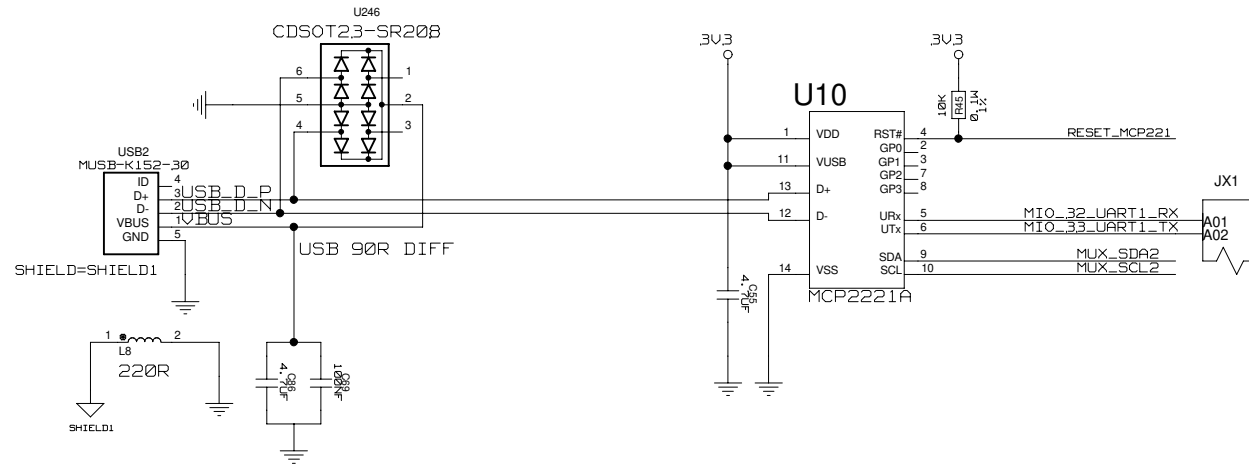
PHY3
PHY - MAC



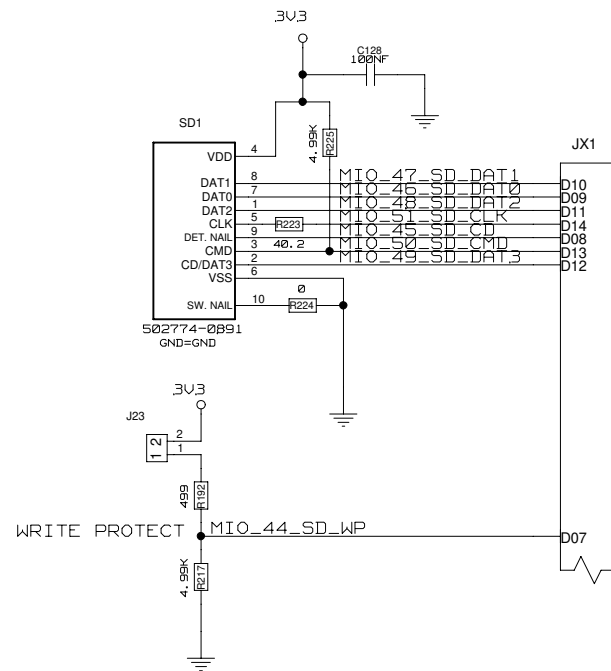
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USB UART1



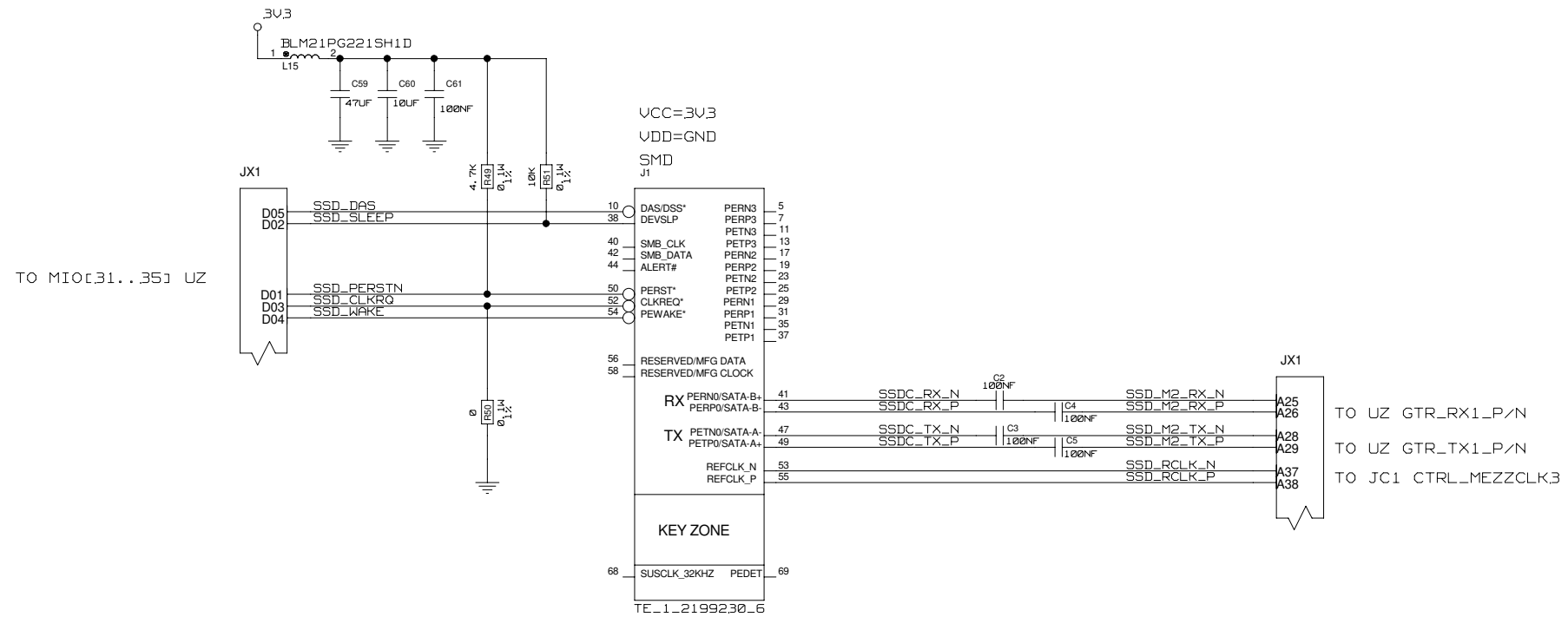
MICRO SD CARD



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SSD M.2 CONNECTOR

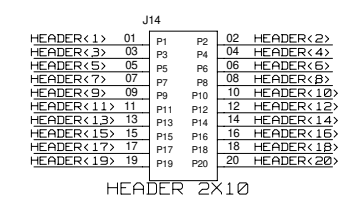
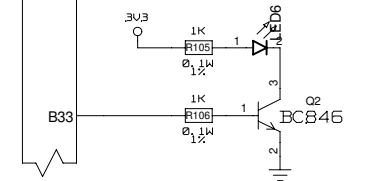
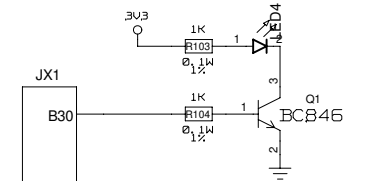
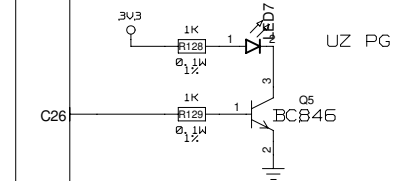
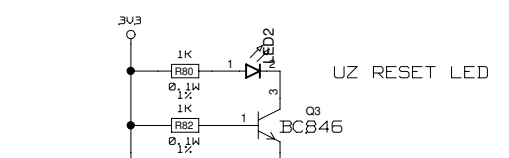
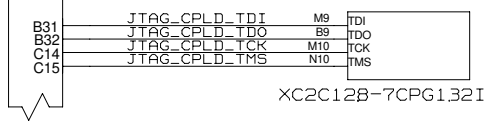
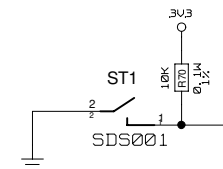
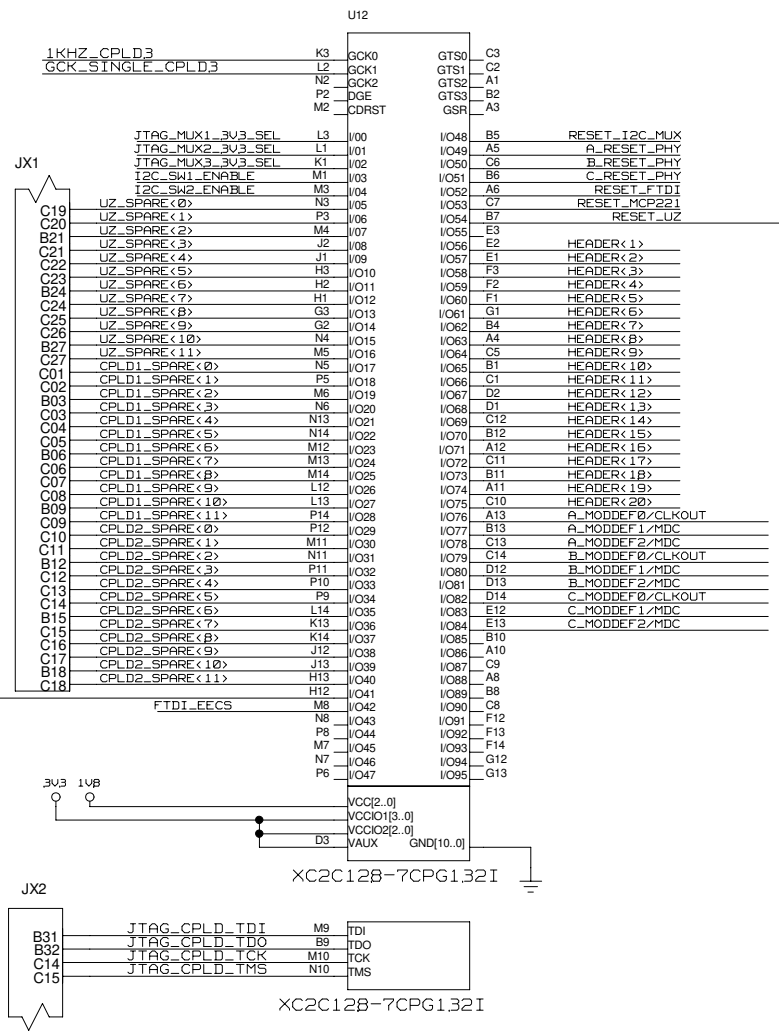


ONE QUIRK OF SATA IS THAT ITS B (RECEIVE) DIFFERENTIAL PAIR HAS A DIFFERENT POLARITY THAN THAT OF THE A (TRANSMIT) PAIR OR PCI EXPRESS RX/TX PAIRS, AND UNLIKE MOST PCIE IMPLEMENTATIONS, IT DOES NOT TOLERATE POLARITY INVERSION. SINCE THE CHIPSET'S SERDES EXPECTS THE SAME LANE POLARITIES IN BOTH SATA AND PCIE MODES, MOTHERBOARDS ACCOUNT FOR THIS QUIRK BY INVERTING THE POLARITY OF THE FIRST SATA/PCIE LANE GOING TO THE M.2 SLOT, TO SATISFY BOTH SATA (CANNOT BE INVERTED) AND PCIE (CAN BE INVERTED):

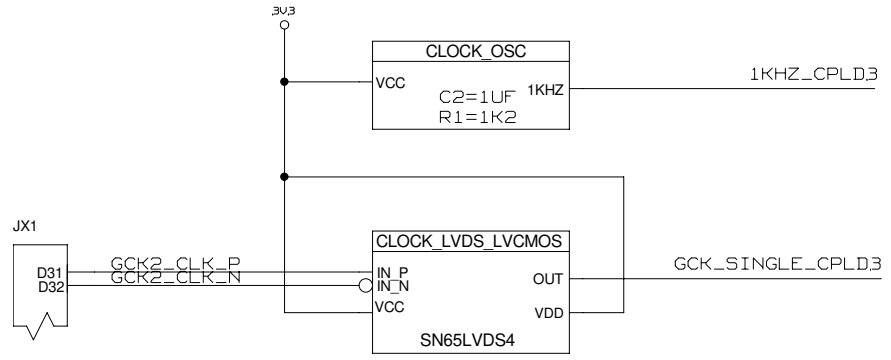
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CPLD.3



CPLD CLOCK

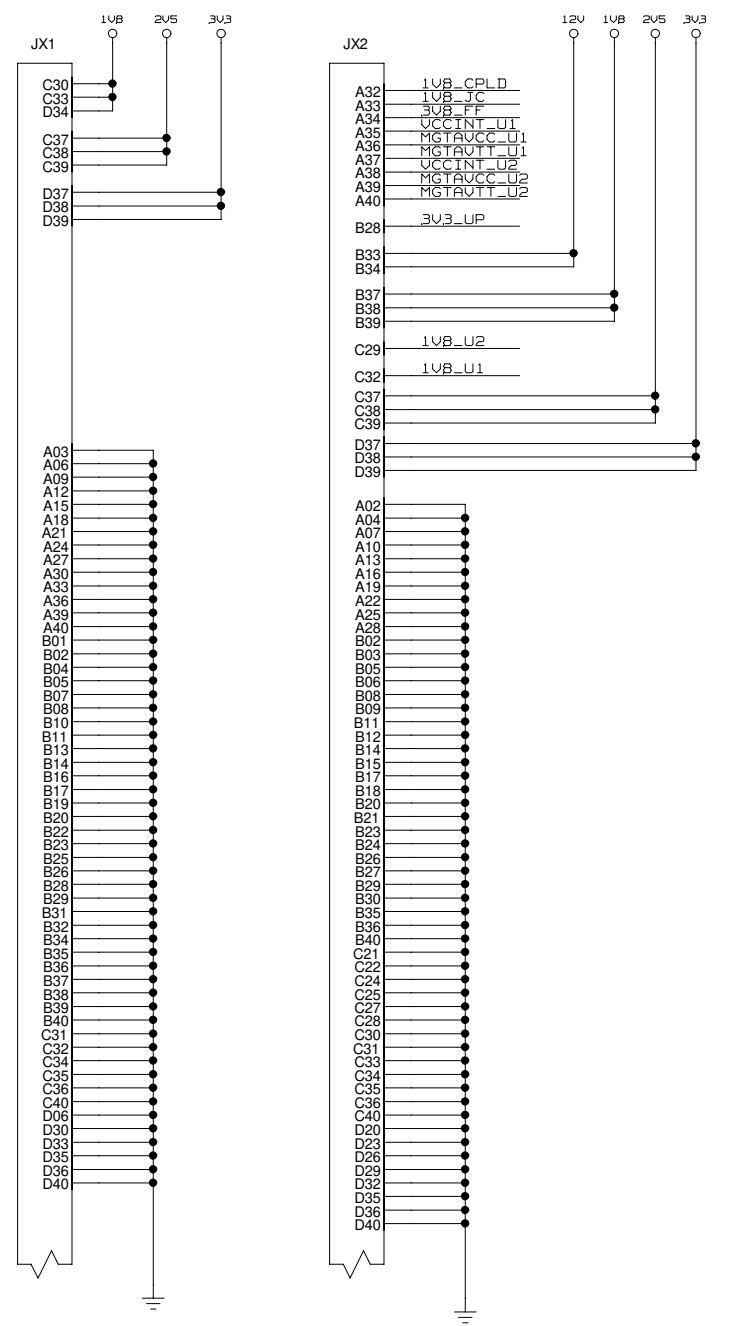


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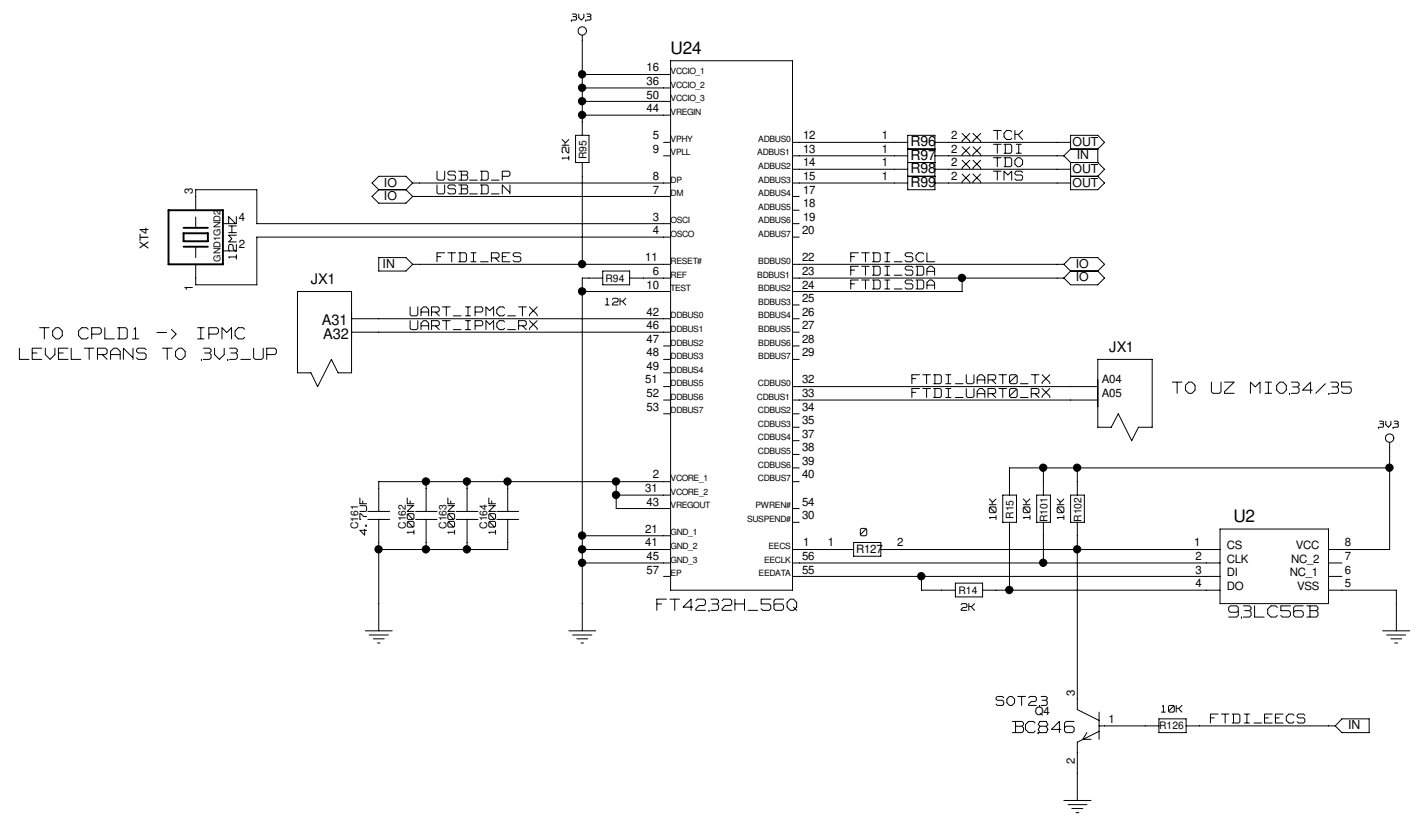
POWER CONNECTOR



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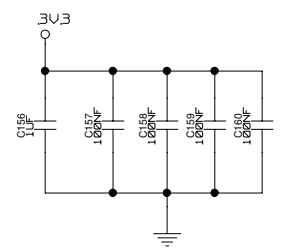
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JTAG FTDI



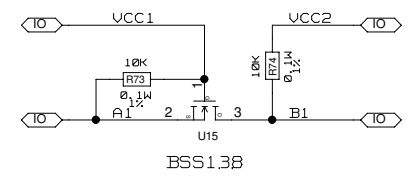
TO CPLD1 -> IPMC
LEVELTRANS TO 3V3_UP

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LEVEL TRANSLATOR

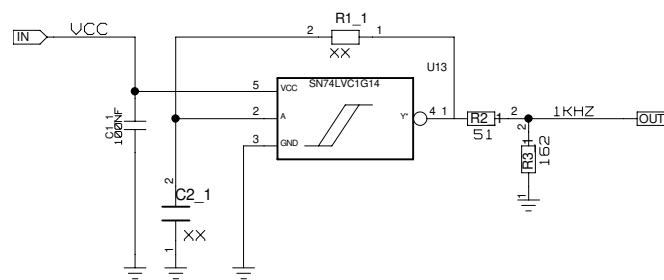


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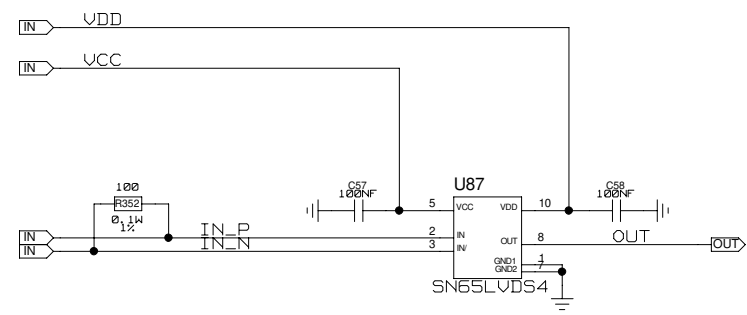
CLOCK_OSC



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CLOCK_LVDS_LVCMOS



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