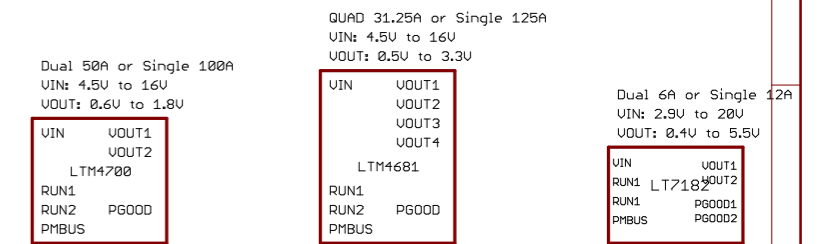


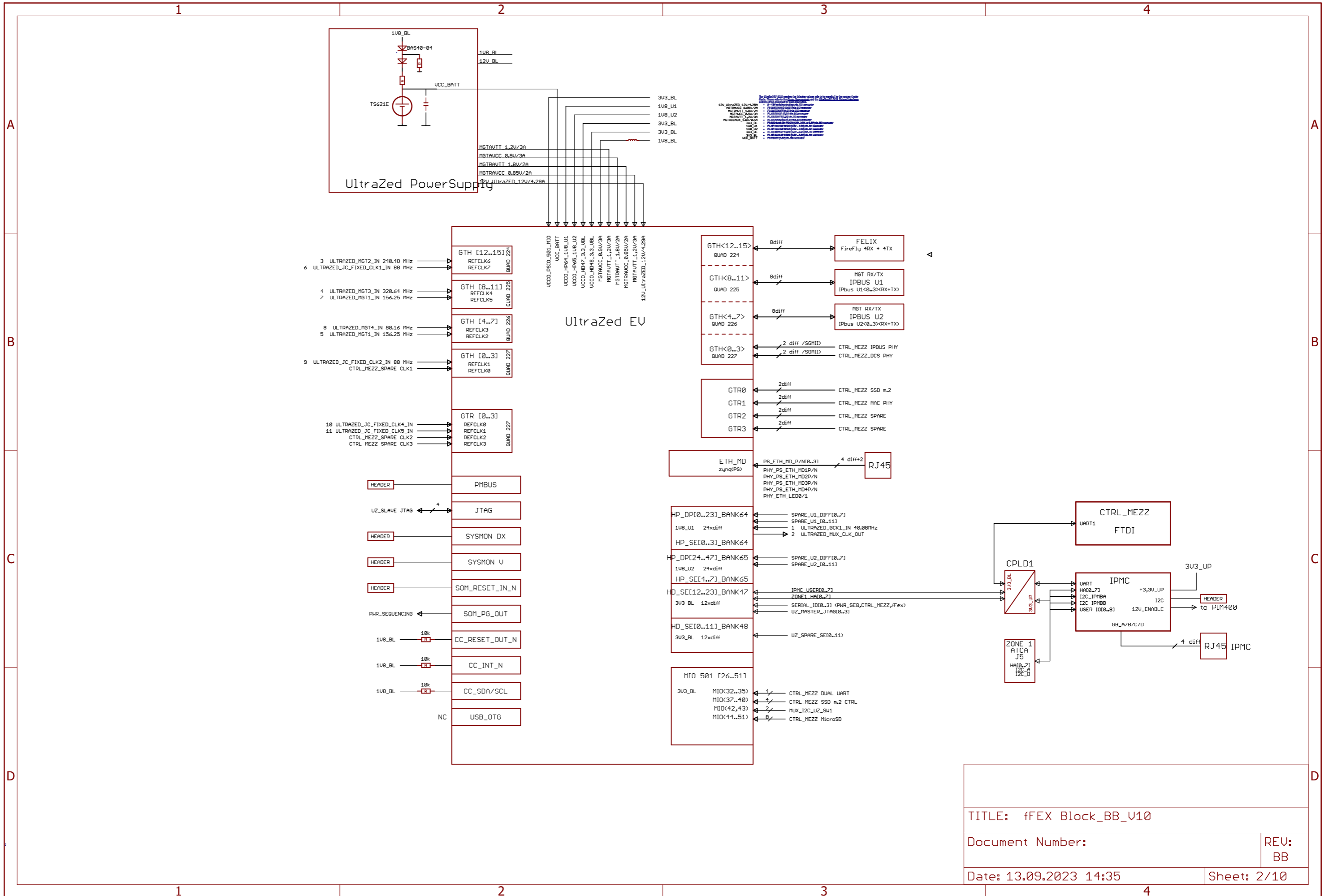
Sequencing an 3v3_UP ?????

has to be sorted

$UXx = 0.573 - 1.375V$
 $UPx = 0.573 - 1.375V$
 $1.250 - 3.000V$
 $2.500 - 6.000V$
 $UH = 2.50 - 6.00V$
 $= 6.00 - 14.40V$



POWER SUPPLY MAINBOARD	
TITLE: fFEX Block_BB_V10	
Document Number:	REV: BB
Date: 13.09.2023 14:35	Sheet: 1/10



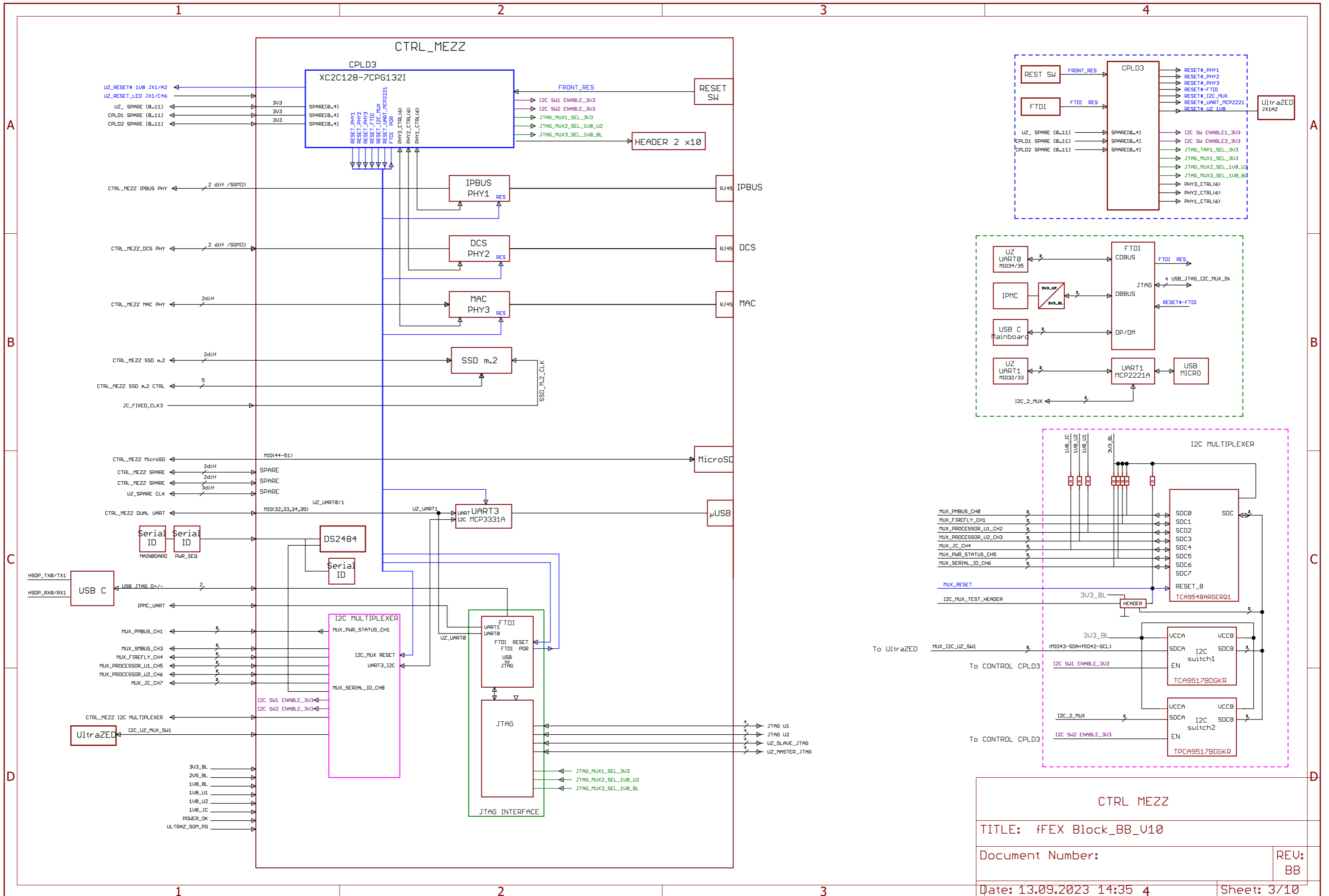
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BB

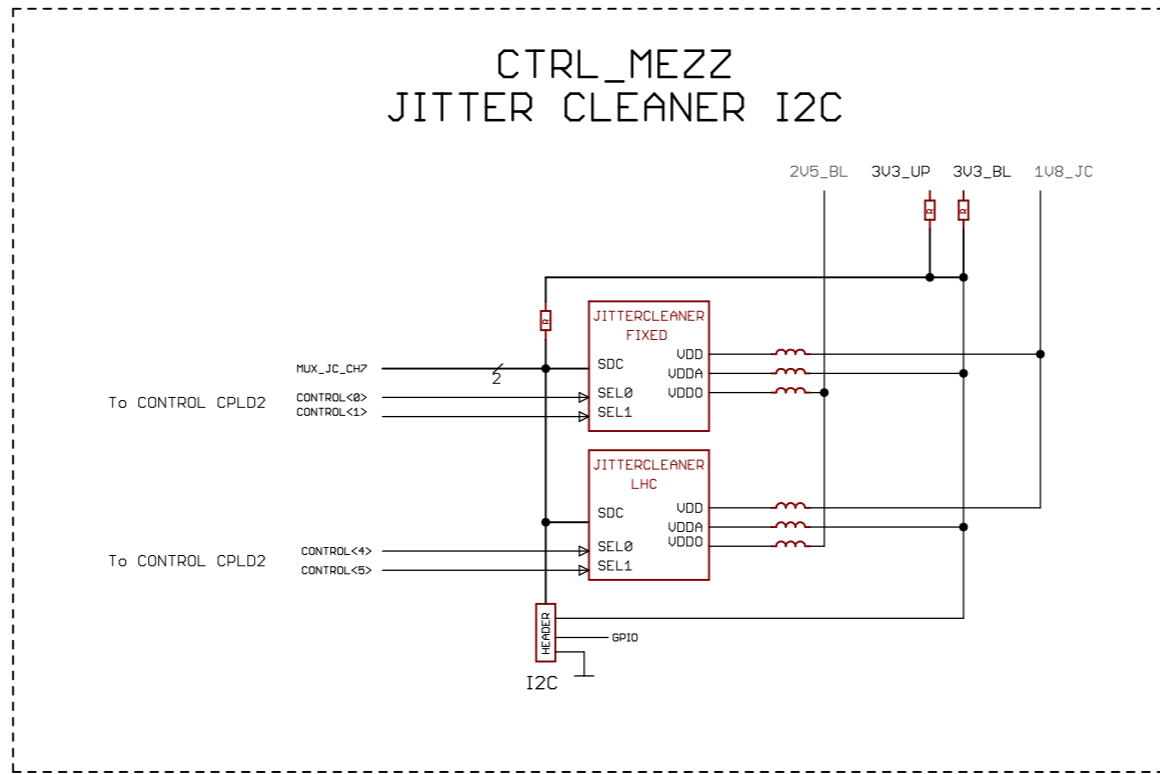
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Sheet: 2/10

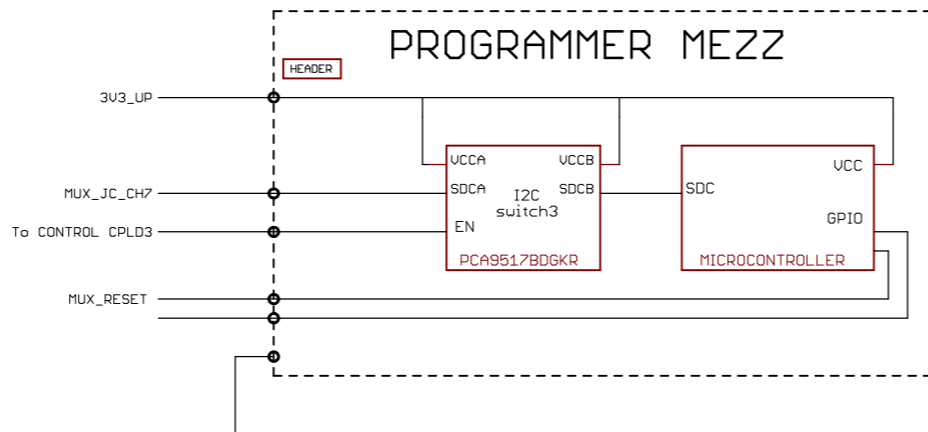


CTRL MEZZ	
TITLE: fFEX Block_BB_U10	
Document Number:	REV: BB
Date: 13.09.2023 14:35	4
Sheet: 3/10	

CTRL_MEZZ JITTER CLEANER I2C



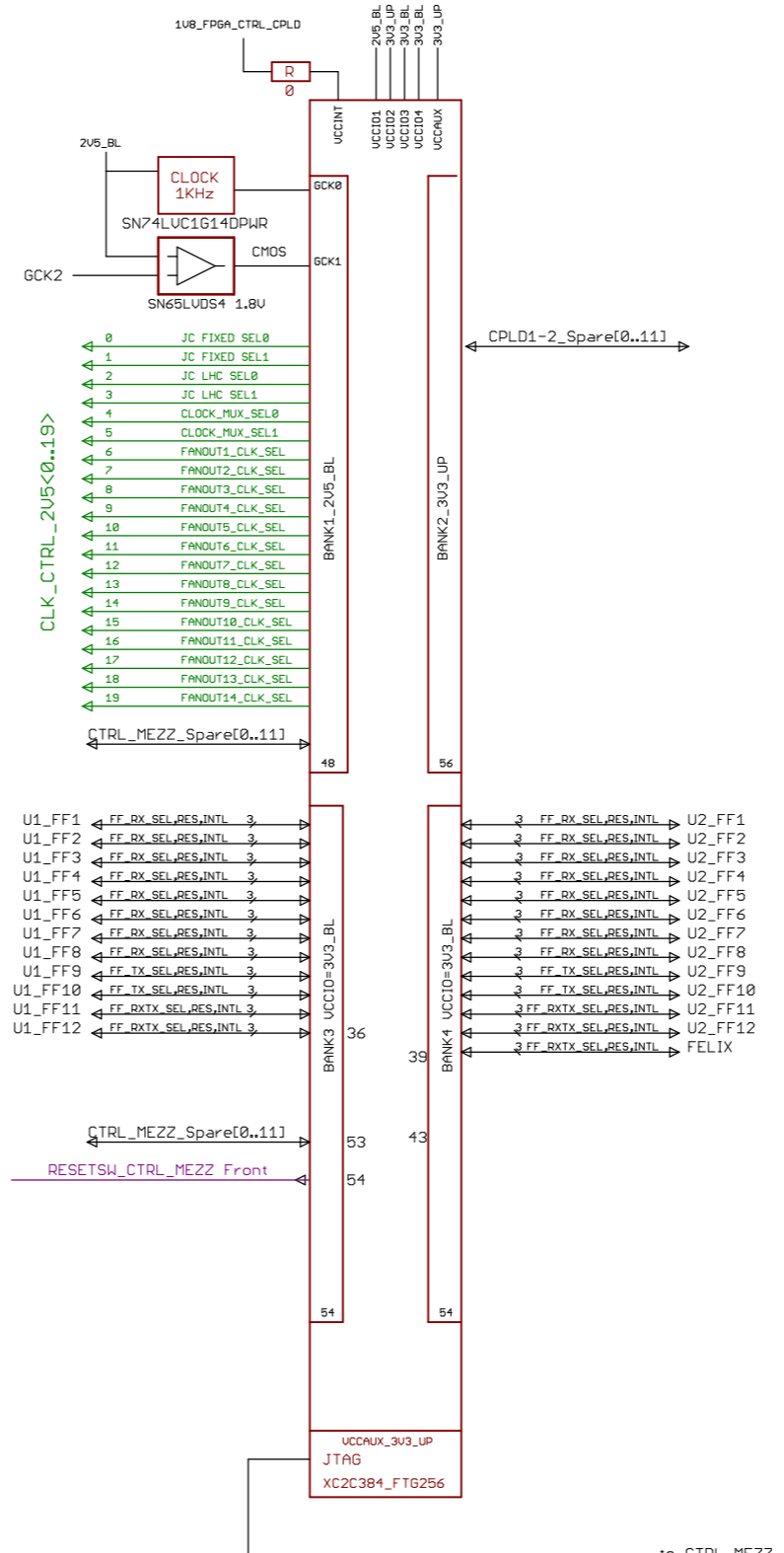
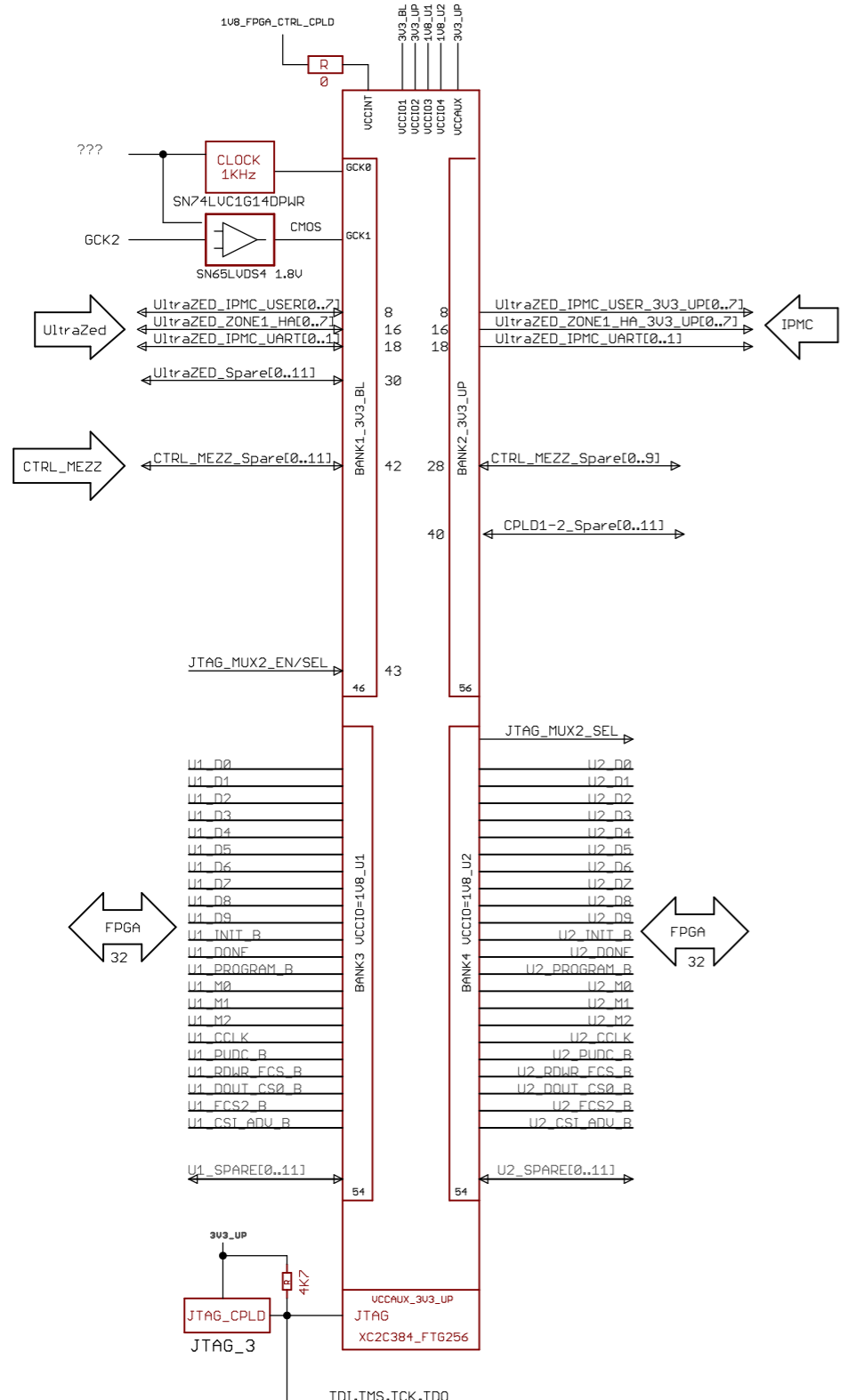
PROGRAMMER MEZZ



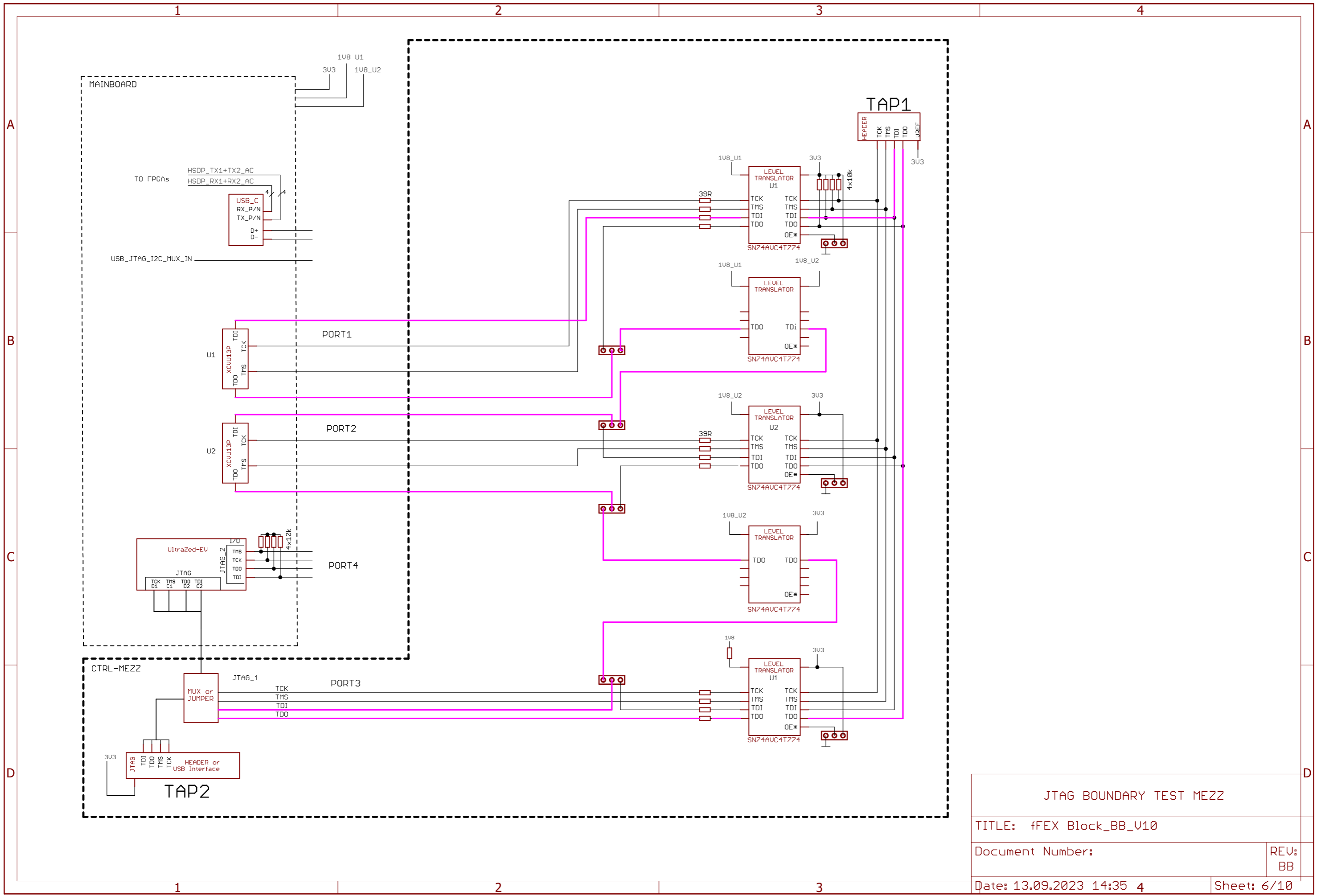
I2C PMBUS + FireFly CTRL Expander	
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Document Number:	REU: BB
Date: 13.09.2023 14:35 4	Sheet: 4/10

FPGA CONFIG_CPLD1

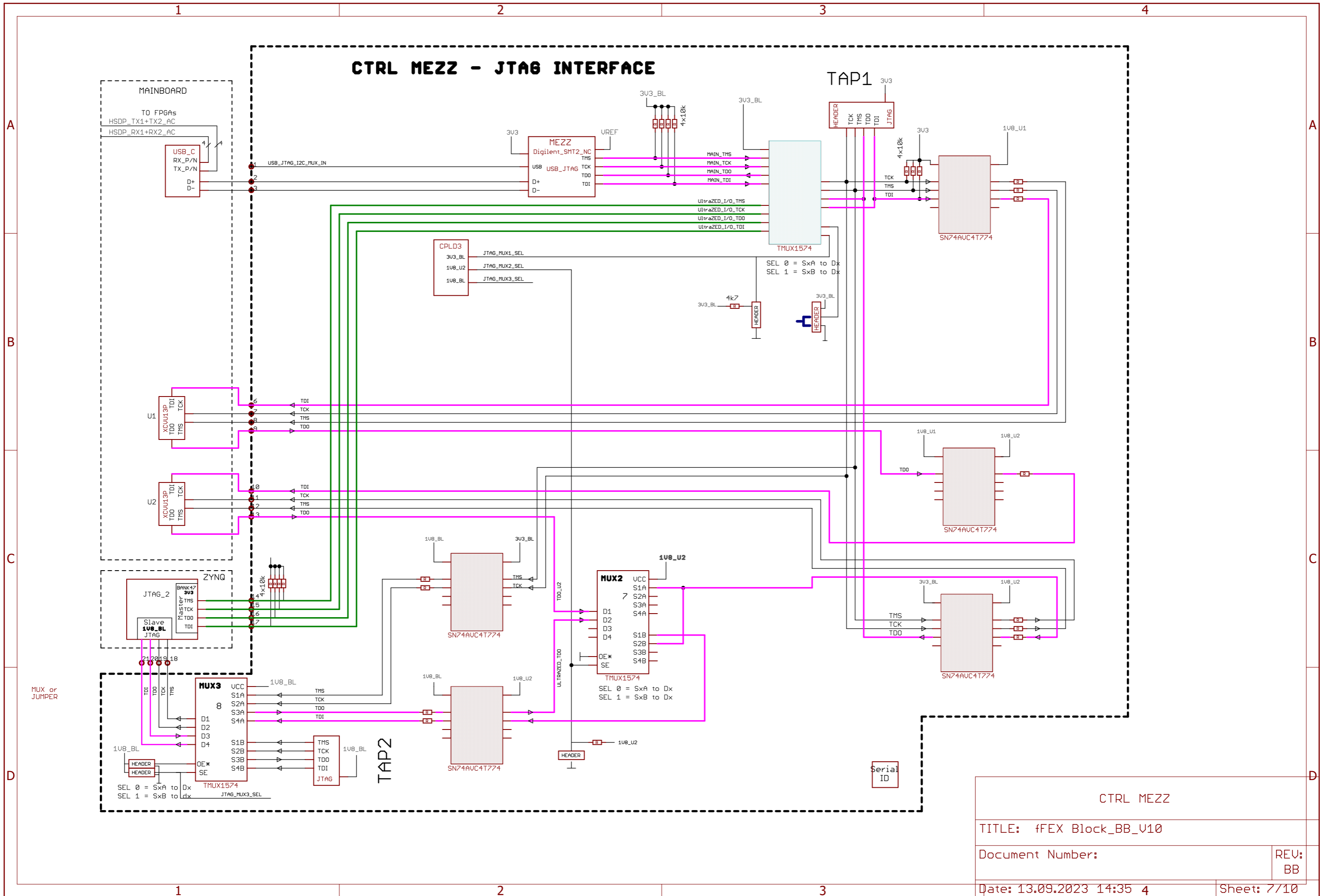
FireFly CONTROL CPLD2



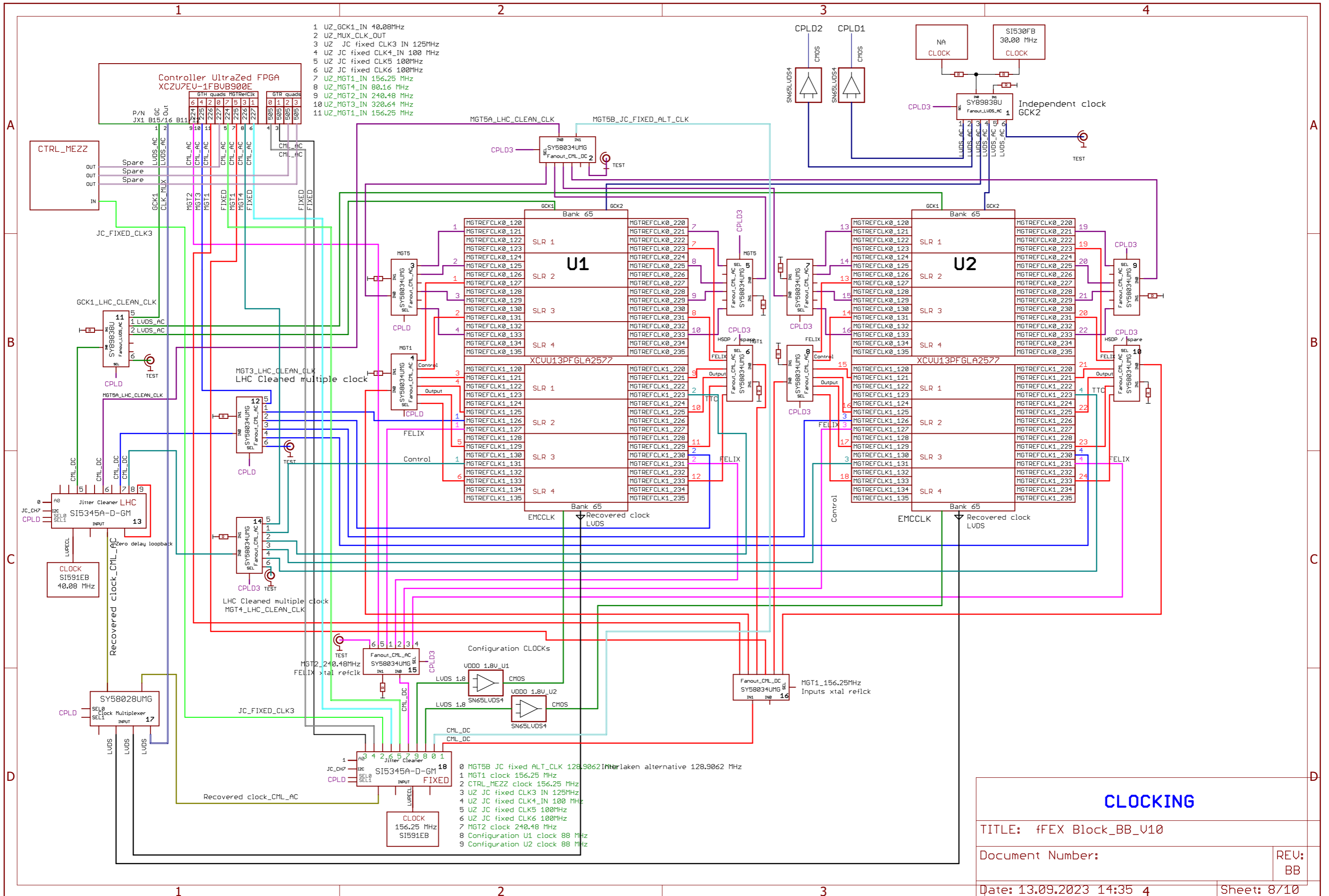
CONTROL CPLDs	
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Document Number:	REV: BB
Date: 13.09.2023 14:35	4
Sheet: 5/10	

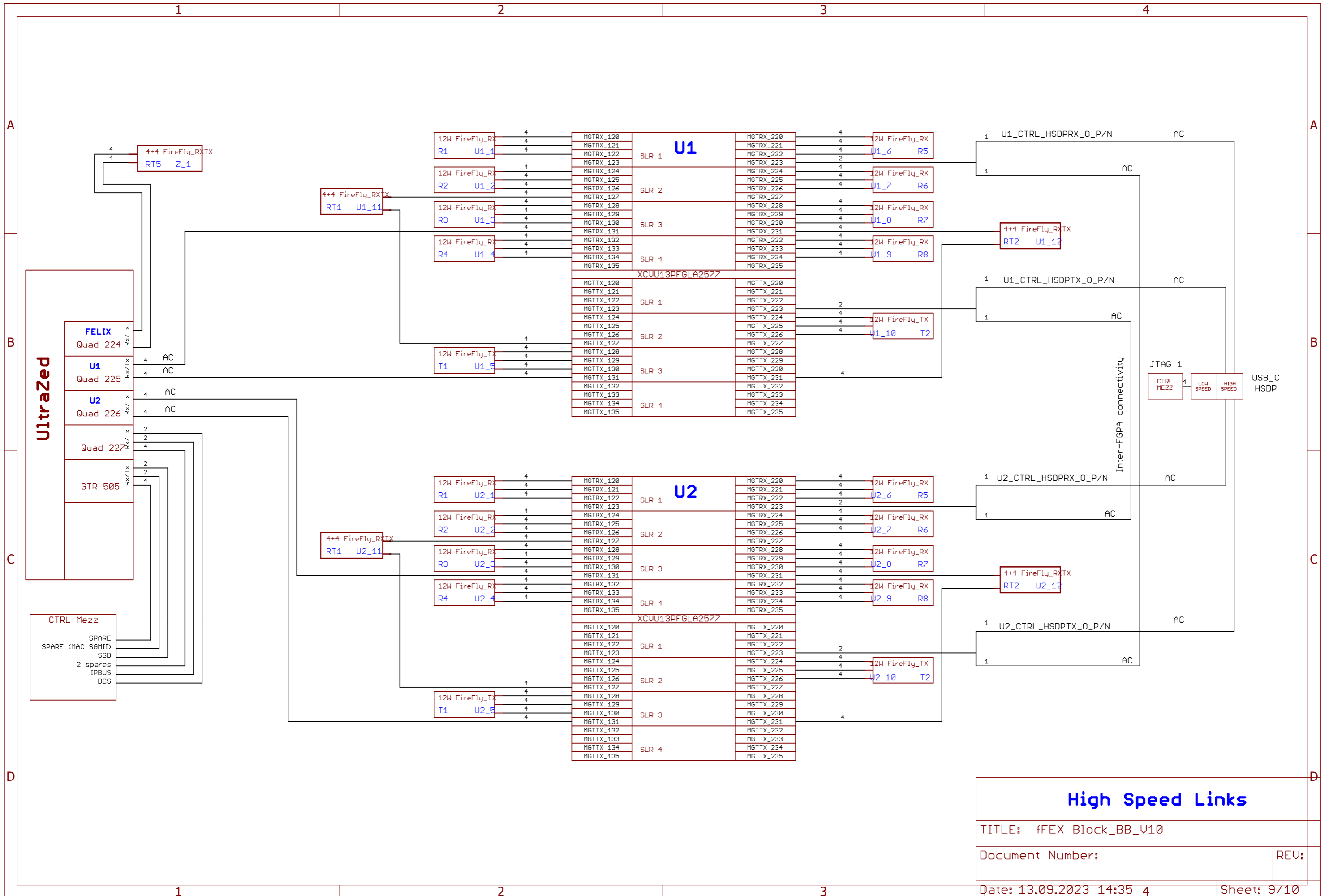


JTAG BOUNDARY TEST MEZZ	
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Document Number:	REU: BB
Date: 13.09.2023 14:35 4	Sheet: 6/10



CTRL MEZZ	
TITLE: fFEX Block_BB_U10	
Document Number:	REV: BB
Date: 13.09.2023 14:35	4
Sheet: 7/10	





High Speed Links

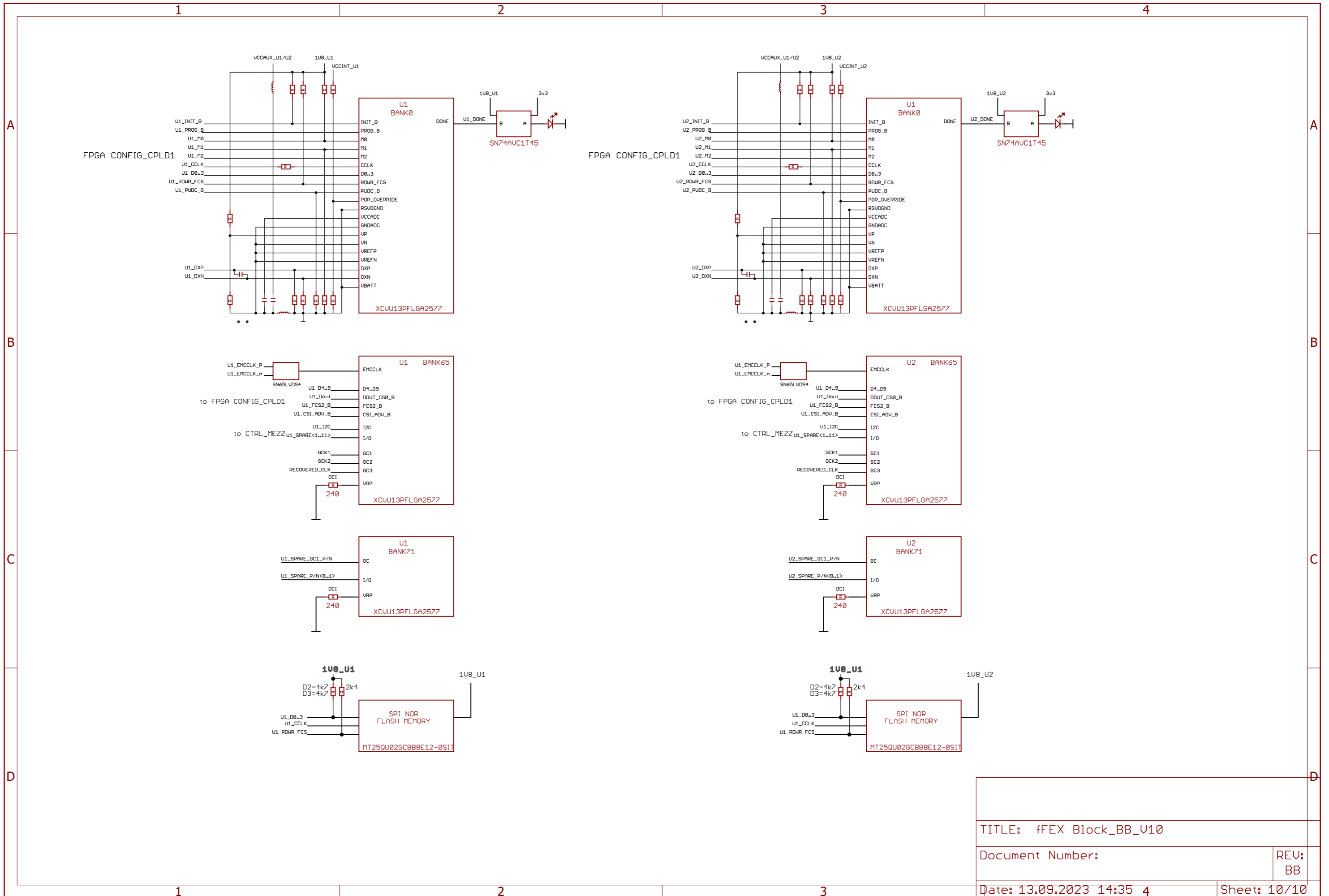
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Date: 13.09.2023 14:35 4

Sheet: 9/10



TITLE: fFEX Block_BB_U10	
Document Number:	REV: BB
Date: 13.09.2023 14:35 4	Sheet: 10/10