CPLD1

IPMC[0..7]

HA[0..7]

3V3_UP

VCCO2_U1+VZED

UltraZED

FOR DEBUG

HEADER

ZONE 1
ATCA
J5

HA[0..7]
I2C_A
I2C_B

-48V_AF
-48V_BF
-48V_ARTN
-48V_BRTN

PIM400

-48V_OUT
-48V_RTN
I2C
+3,3V_UP

-48V_IN
-48V_RTN
+12V_OUT

12V/400W

ON/OFF

HA[0..7]
I2C_IPMBA
I2C_IPMBB
IPMC[0..7]

IPMC

+3,3V_UP
Mgt_I2C
12V_ENABLE

HEADER

=1
XOR

+

12V_EN_CPLD
ADM_QBU_12V_EN

HEADER

SEquencing an 3v3_UP ?????

+12V_IN

ADM1260
VH
VX1 PD01
VX2 PD02
VX3 PD03
VX4 PD04
VX5 PD05
VP1 PD06
VP2 PD07
VP3 PD08
VP4 PD09
ICB PD010
I2C

VCCINT_U1 0.85V
MGTYAVCC_U1 0.9V
MGTYAVTT_U1 1.2V
VCCINT_U2 0.85V
MGTYAVCC_U2 0.9V
MGTYAVTT_U2 1.2V
3V3_BL
2V5_BL
1V8_BL

EN_VCCINT_U1
EN_MGTYVCC_U1
EN_MGTYAVTT_U1
VCCINT_U2
EN_MGTYVCC_U2
EN_MGTYAVTT_U2
EN_3V3_BL
EN_2V5_BL
EN_1V8_BL

CHIPBUS
SMBUS

ADM1260
VH
VX1 PD01
VX2 PD02
VX3 PD03
VX4 PD04
VX5 PD05
VP1 PD06
VP2 PD07
VP3 PD08
VP4 PD09
ICB PD010
I2C

3V8_FIREFLY_BIAS
1V8_U1
1V8_U2
U2_12V_IN
ULTRAZ_SOM_PG
1V8_CPLD
1V8_JC

EN_3V8_FF
EN_1V8_U1
EN_1V8_U2
EN_1V8_CPLD
EN_1V8_JC
ADM_QBU_12V_EN

ADM_SMBUS

ADM1260
VH
VX1 PD01
VX2 PD02
VX3 PD03
VX4 PD04
VX5 PD05
VP1 PD06
VP2 PD07
VP3 PD08
VP4 PD09
ICB PD010
I2C

UZ_MGTRAVCC 0.85V
UZ_MGTRAVTT 1.8V
UZ_MGTAVCC 0.9V
UZ_MGTAVTT 1.2V
UZ_MGTVCCAUX 1.8V

EN_UZ_12V_IN
EN_UZ_MGTRAVCC
EN_UZ_MGTAVCC
EN_UZ_MGTAVTT
EN_UZ_MGTRAVTT
EN_UZ_MGTVCCAUX

POWER_OK to CTRL_MEZZ

VUx = 0.573V - 1.375V
VPx = 0.573 - 1.375V
1.250 - 3.000V
2.500 - 6.000V
VH = 2.50 - 6.00V
= 6.00-14.40V

MUX_PMBUS_CH11

FOR DEBUG
HEADER

MEZZANINE_FPGA_A

VIN VOUT1 VOUT2
LTM4700
RUN1
RUN2 PG
PMBUS 2x50A

0.85V VCCINT_U1
0.9V MGTYAVCC_U1
1.2V MGTYAVTT_U1
1V8_U1
VCCAUX_U1
MGTVCCAUX_U1

MEZZANINE_FPGA_B

0.85V VCCINT_U2
0.9V MGTYAVCC_U2
1.2V MGTYAVTT_U2
1V8_U2
VCCAUX_U2
MGTVCCAUX_U2

MEZZANINE_BOARDLEVEL

VIN VOUT1 VOUT2 VOUT3 VOUT4
LTM4681
RUN1 PGOOD1
RUN2 PGOOD2
RUN3 PGOOD3
RUN4 PGOOD4
PMBUS 4x31A

3V3_BL
2V5_BL
1V8_U1
1V8_U2

VIN VOUT1 VOUT2
RUN1 LT7182
RUN1 PGOOD1
PMBUS PGOOD2
2x6A

1V8_BL
3V8_FIREFLY_BIAS
1V8_CPLD
1V8_JC

MEZZANINE_BOARDLEVEL

VIN VOUT
EN KTS1640
12V/4.29A_C

UZ_12V_IN

VIN VOUT1 VOUT2
RUN1 LT7182
RUN1 PGOOD1
PMBUS PGOOD2
2x6A

0.85V/2A UZ_MGTRAVCC
0.9V/3A UZ_MGTAVCC
1.2V/3A UZ_MGTAVTT
1.8V/1.5A UZ_MGTRAVTT

VIN VOUT
EN MIC94060

1.8V/0.5A UZ_MGTVCCAUX

MEZZANINE_UltraZED

UltraZED

Dual 50A or Single 100A
VIN: 4.5V to 16V
VOUT: 0.6V to 1.8V

VIN VOUT1 VOUT2
LTM4700
RUN1
RUN2 PGOOD
PMBUS

QUAD 31.25A or Single 125A
VIN: 4.5V to 16V
VOUT: 0.5V to 3.3V

VIN VOUT1 VOUT2 VOUT3 VOUT4
LTM4681
RUN1
RUN2 PGOOD
PMBUS

Dual 6A or Single 12A
VIN: 2.9V to 20V
VOUT: 0.4V to 5.5V

VIN VOUT1 VOUT2
RUN1 LT7182
RUN1 PGOOD1
PMBUS PGOOD2

POWER SUPPLY MAINBOARD

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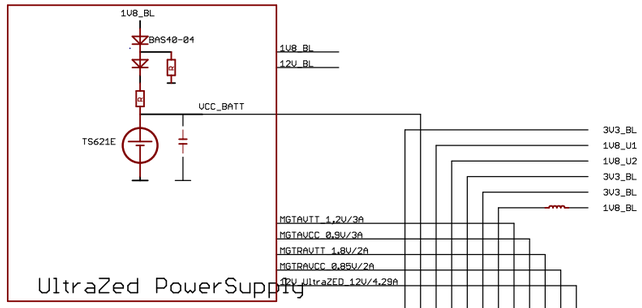

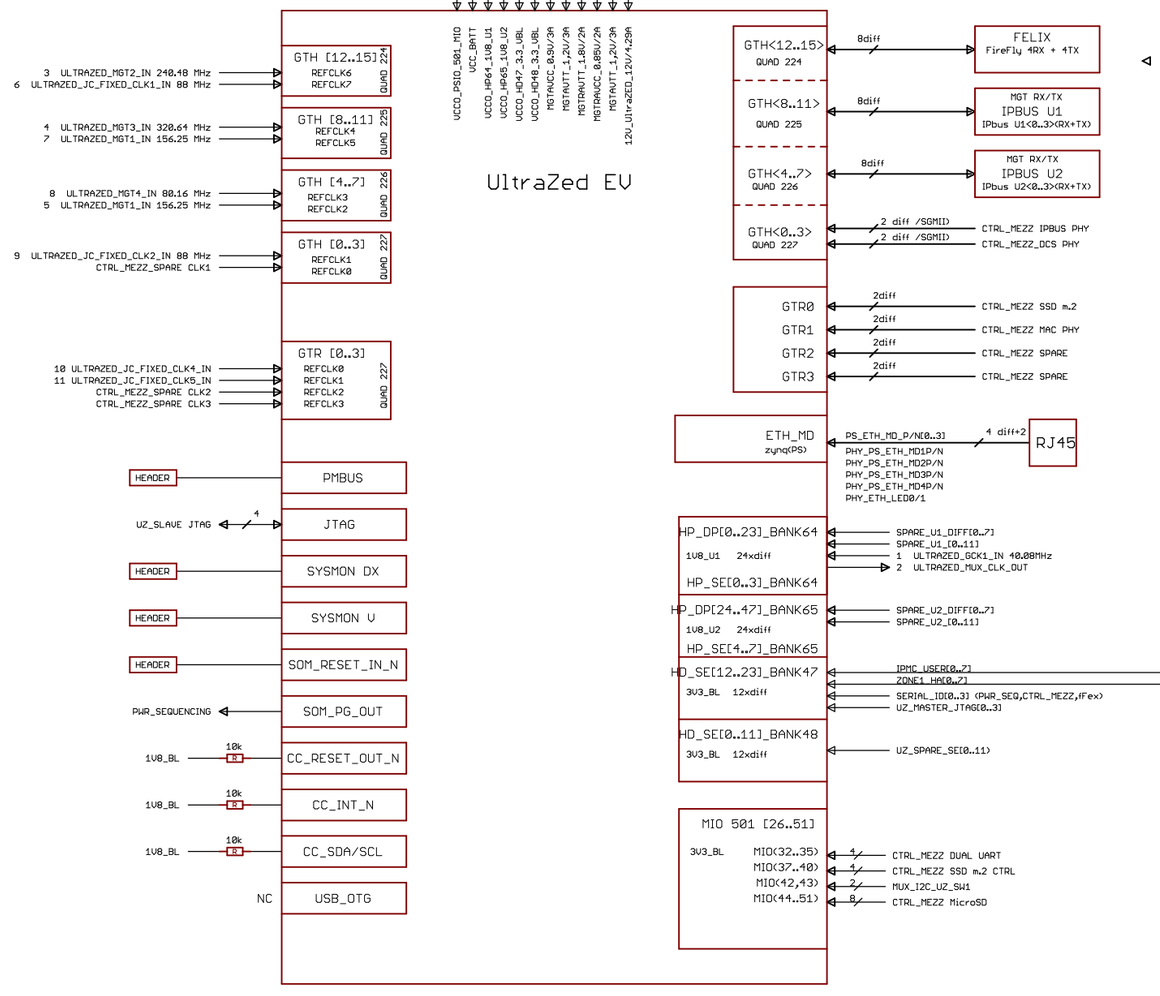

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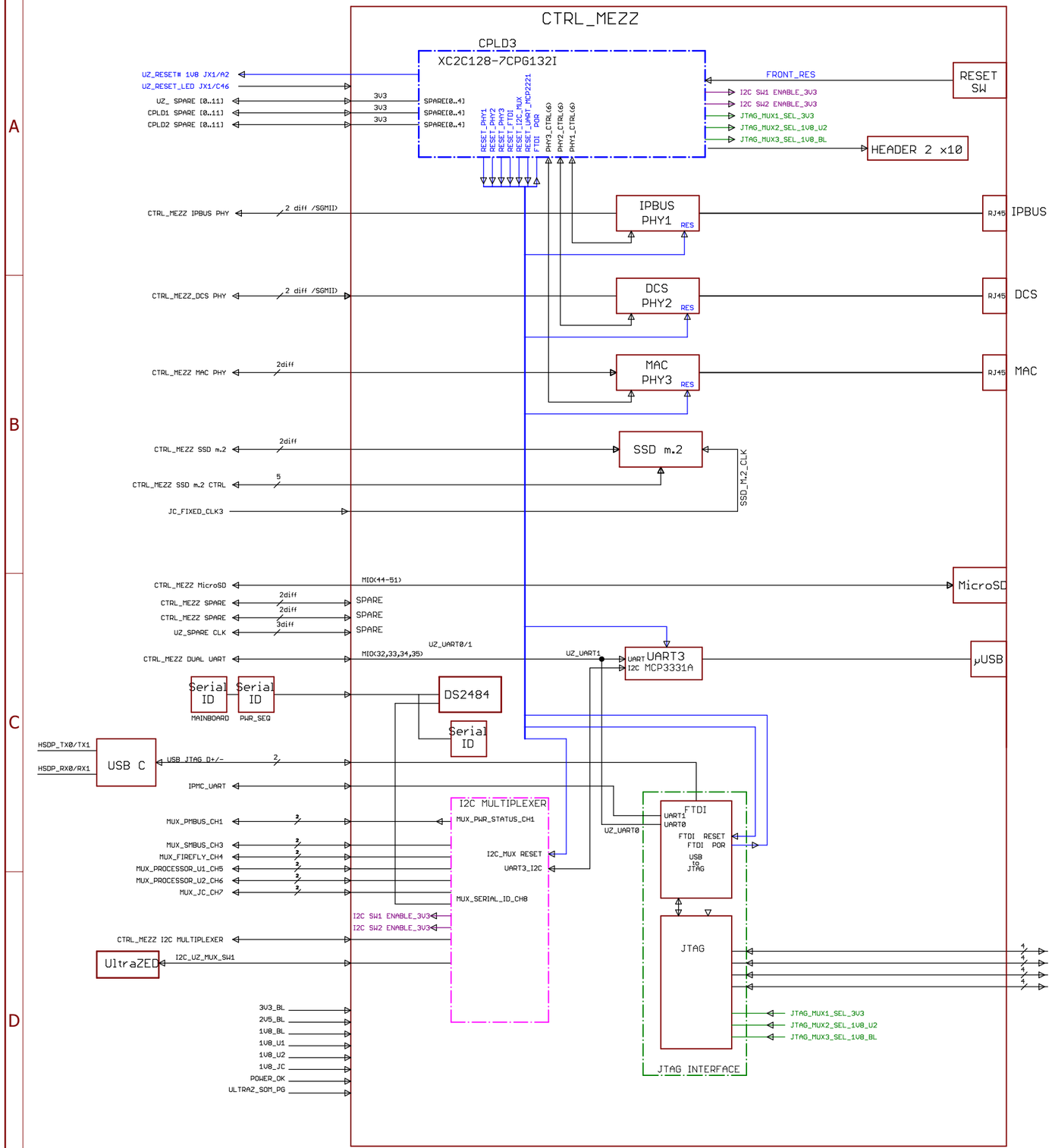

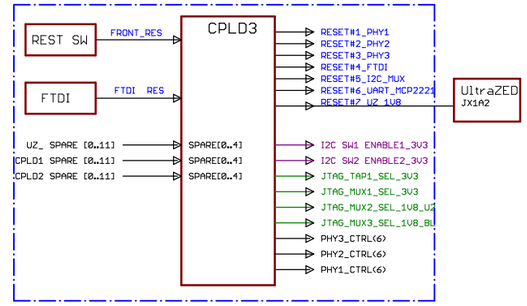

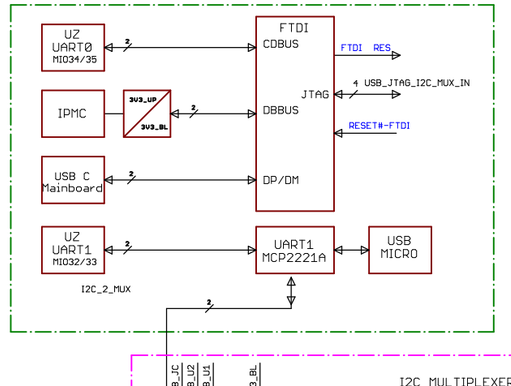

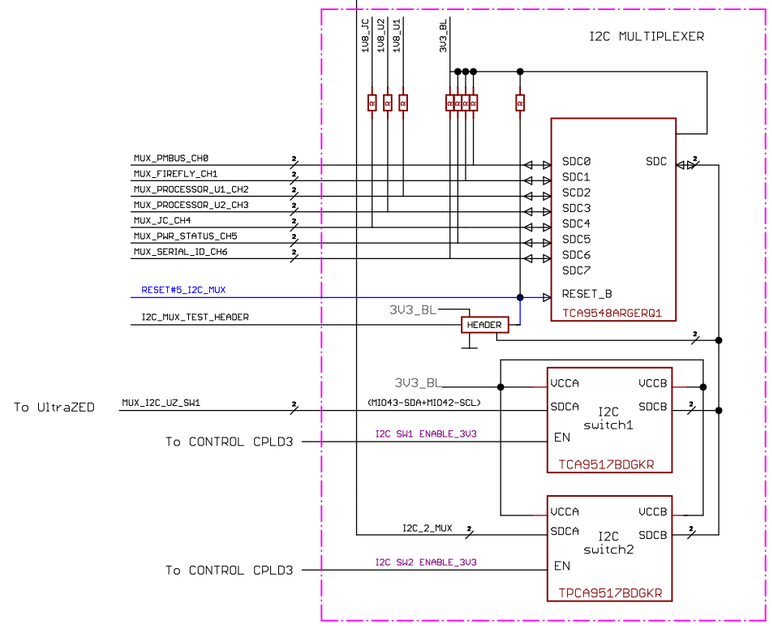

CTRL MEZZ

TITLE: fFEX Block_BB_V12

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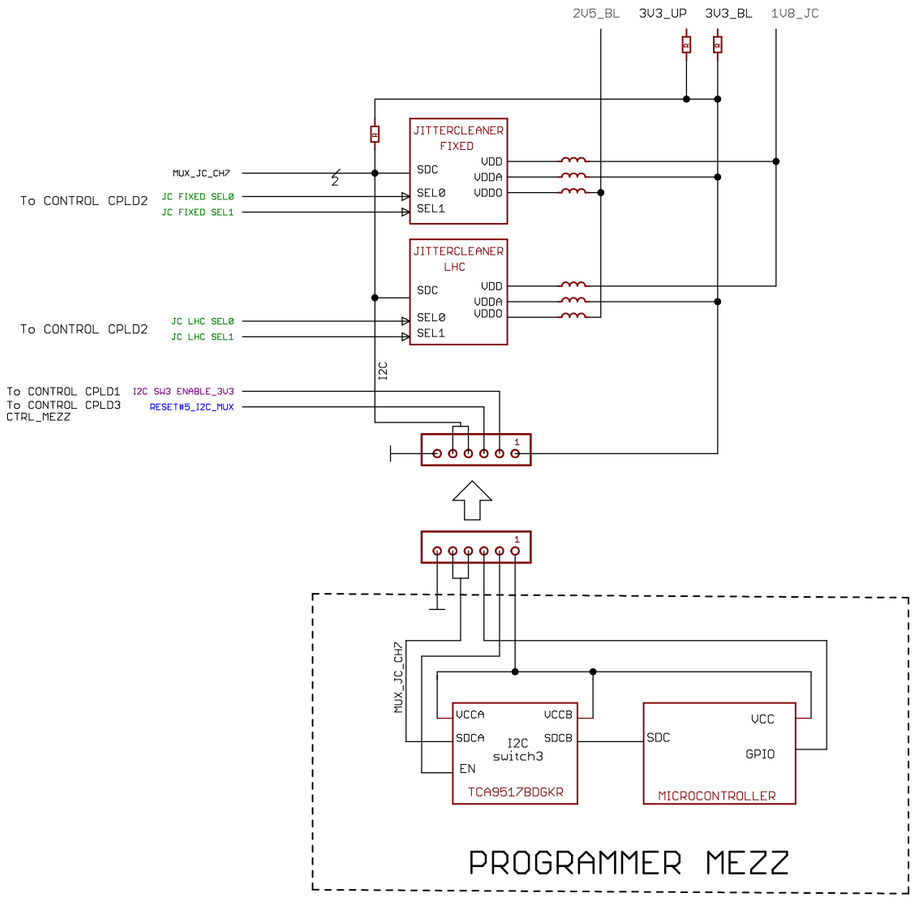
JITTER CLEANER I2C



Jitter Cleaner	
TITLE: fFEX Block_BB_V12	
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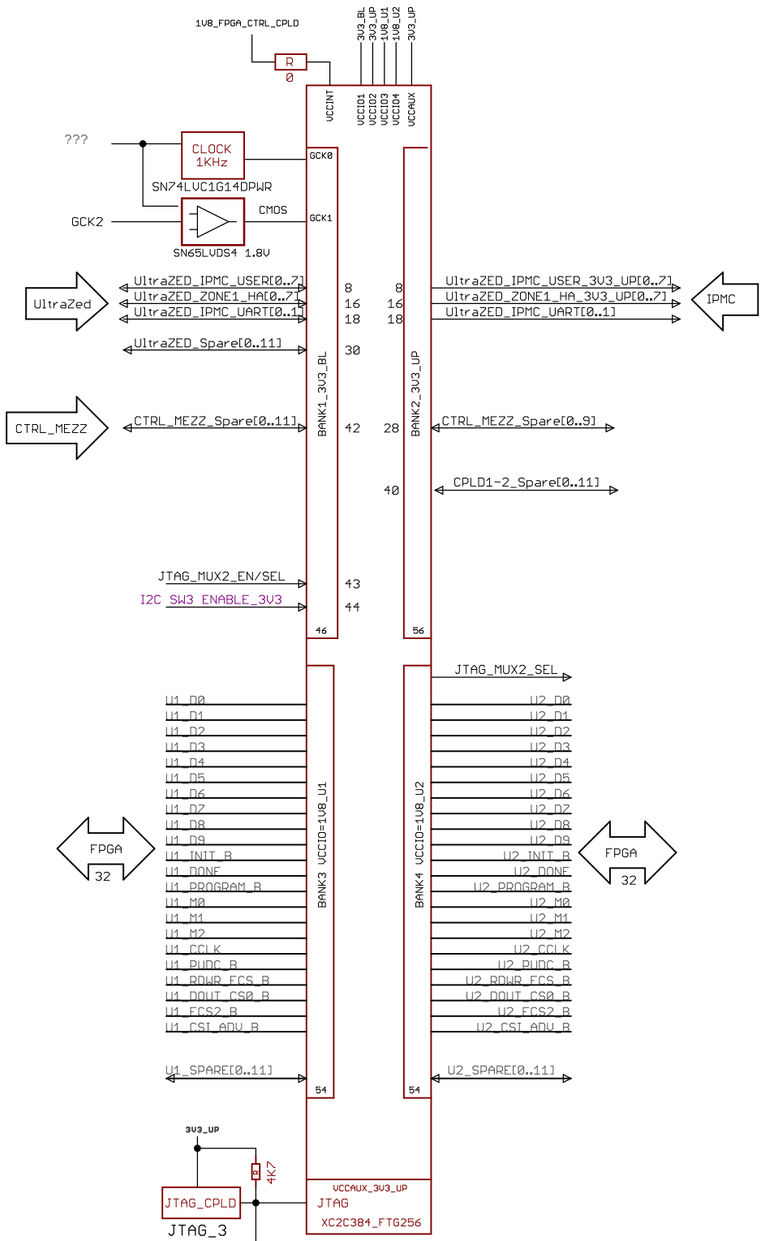
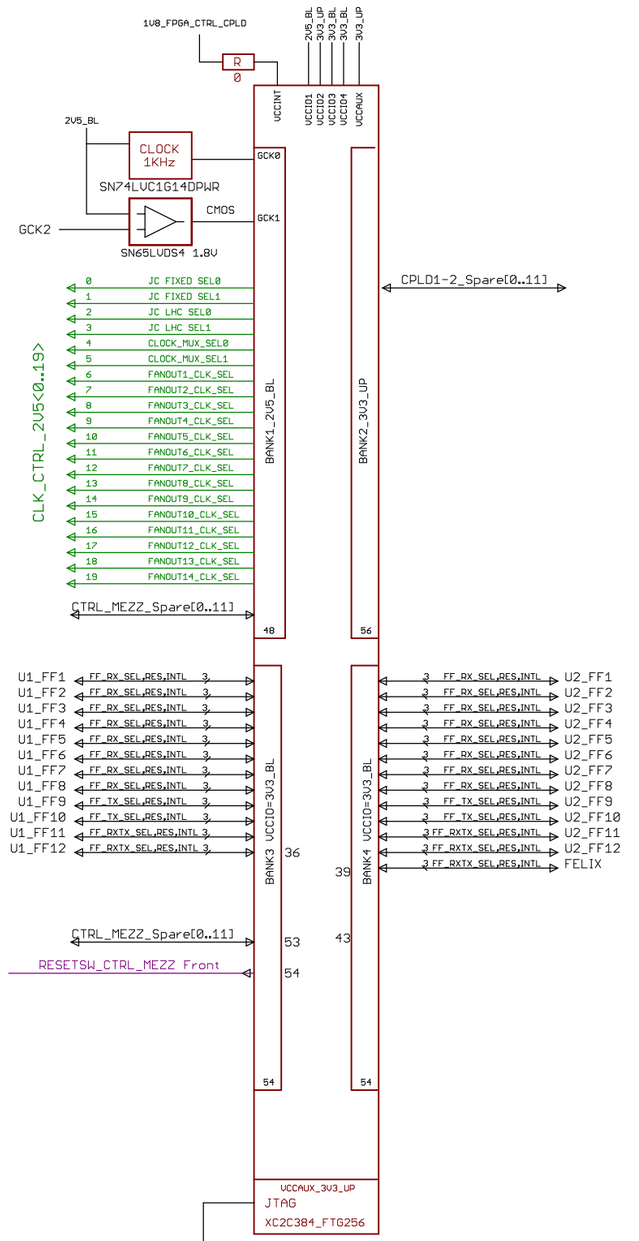
FPGA CONFIG_CPLD1



FireFly CONTROL CPLD2



CONTROL CPLDs	
TITLE: fFEX Block_BB_V12	
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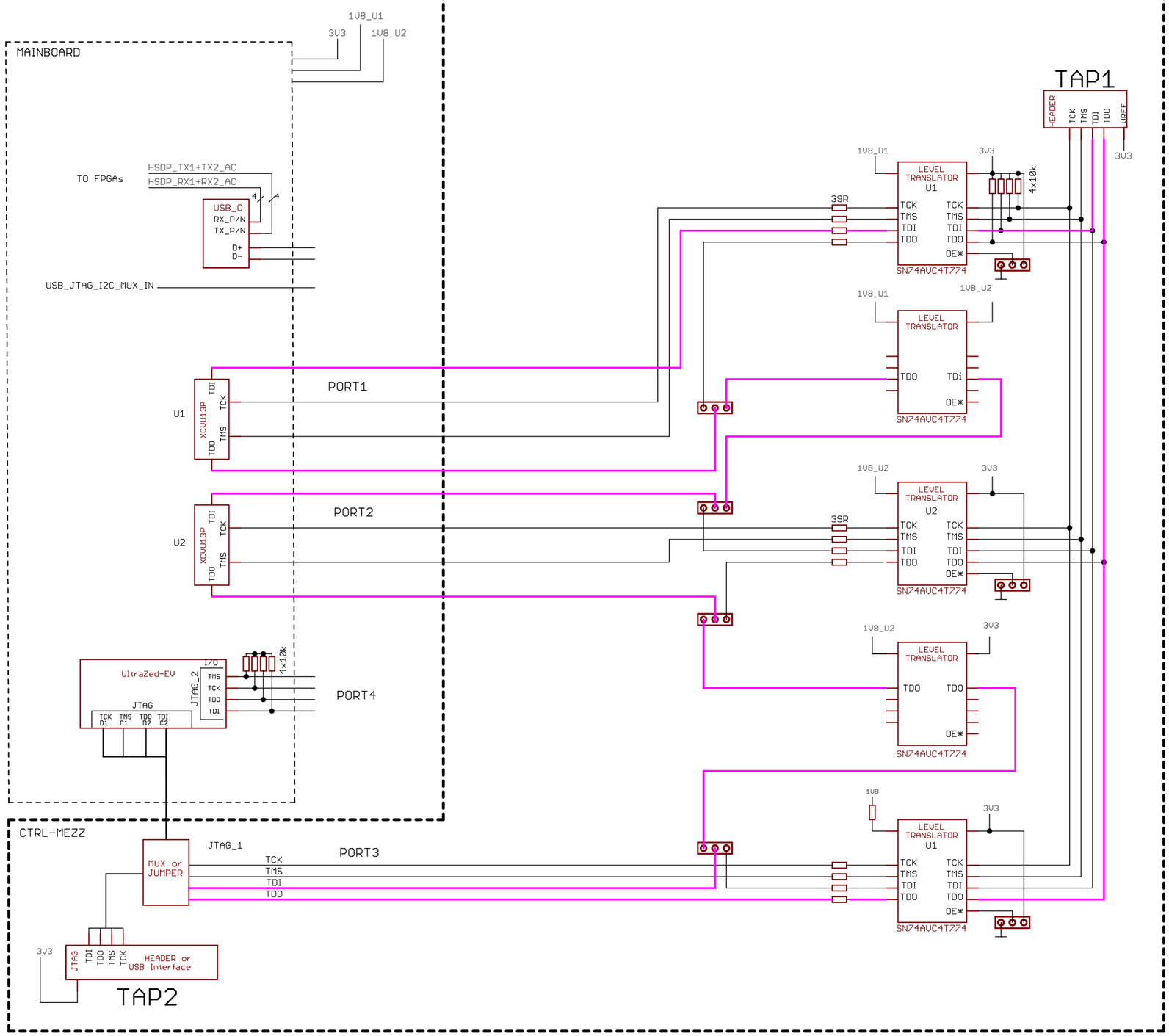

JTAG BOUNDARY TEST MEZZ	
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CTRL MEZZ - JTAG INTERFACE

MAINBOARD

TO FPGAs

HSDP_TX1+TX2_AC

HSDP_RX1+RX2_AC

USB_C

RX_P/N

TX_P/N

D+

D-

USB_JTAG_I2C_MUX_IN

MEZZ

Digilent_SMT2_NC

USB

USB_JTAG

TMS

TCK

TDO

TDI

VREF

3V3

3V3_BL

4x10k

MAIN_TMS

MAIN_TCK

MAIN_TDO

MAIN_TDI

TAP1

HEADER

JTAG

UltraZED_I/O_TMS

UltraZED_I/O_TCK

UltraZED_I/O_TDO

UltraZED_I/O_TDI

TMUX1574

SEL 0 = SxA to Dx

SEL 1 = SxB to Dx

CPLD3

3V3_BL

1V8_U2

1V8_BL

JTAG_MUX1_SEL

JTAG_MUX2_SEL

JTAG_MUX3_SEL

4k7

1V8_U1

SN74AUC4T774

U1

U2

XCVU13P

TDI

TCK

TMS

TDO

ZYNQ

JTAG_2

BANK47

3V3

Master

Slave

1V8_BL

JTAG

21 20 19 18

MUX or JUMPER

MUX3

MUX2

D1

D2

D3

D4

S1A

S2A

S3A

S4A

S1B

S2B

S3B

S4B

VCC

OE*

SE

TAP2

ULTRAZED_TDO

Serial ID

CTRL MEZZ	
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1 UZ_GCK1_IN 40.08MHz
2 UZ_MUX_CLK_OUT
3 UZ JC fixed CLK3 IN 125MHz
4 UZ JC fixed CLK4_IN 100 MHz
5 UZ JC fixed CLK5 100MHz
6 UZ JC fixed CLK6 100MHz
7 UZ_MGT1_IN 156.25 MHz
8 UZ_MGT4_IN 80.16 MHz
9 UZ_MGT2_IN 240.48 MHz
10 UZ_MGT3_IN 320.64 MHz
11 UZ_MGT1_IN 156.25 MHz

Controller UltraZed FPGA
XCZU7EV-1FBVB900E
GTH quads MGTRefClk
GTR quads
P/N JX1 B15/16 B11
GC Out
CTRL_MEZZ
Spare
Spare
Spare
JC_FIXED_CLK3
GCK1_LHC_CLEAN_CLK
MGT5A_LHC_CLEAN_CLK
MGT3_LHC_CLEAN_CLK
LHC Cleaned multiple clock
MGT5A_LHC_CLEAN_CLK
MGT5B_JC_FIXED_ALT_CLK
CPLD2
CPLD1
NA CLOCK
SI530FB 30.00 MHz CLOCK
Independent clock GCK2
Bank 65
SLR 1
SLR 2
SLR 3
SLR 4
U1
U2
XCVU13PFGLA2577
EMCCLK
Recovered clock LVDS
Jitter Cleaner LHC SI5345A-D-GM
Zero delay loopback
CLOCK SI591EB 40.08 MHz
Recovered clock_CML_AC
SY58028UMG Clock Multiplexer
Jitter Cleaner SI5345A-D-GM FIXED
CLOCK 156.25 MHz SI591EB
LHC Cleaned multiple clock
MGT4_LHC_CLEAN_CLK
MGT2_240.48MHz FELIX xtal refclk
Configuration CLOCKs
VDDO 1.8V_U1
VDDO 1.8V_U2
SN65LVDS4
MGT1_156.25MHz Inputs xtal reflck
Recovered clock_CML_AC

0 MGT5B JC fixed ALT_CLK 128.9062 Interlaken alternative 128.9062 MHz
1 MGT1 clock 156.25 MHz
2 CTRL_MEZZ clock 156.25 MHz
3 UZ JC fixed CLK3 IN 125MHz
4 UZ JC fixed CLK4_IN 100 MHz
5 UZ JC fixed CLK5 100MHz
6 UZ JC fixed CLK6 100MHz
7 MGT2 clock 240.48 MHz
8 Configuration U1 clock 88 MHz
9 Configuration U2 clock 88 MHz

CLOCKING

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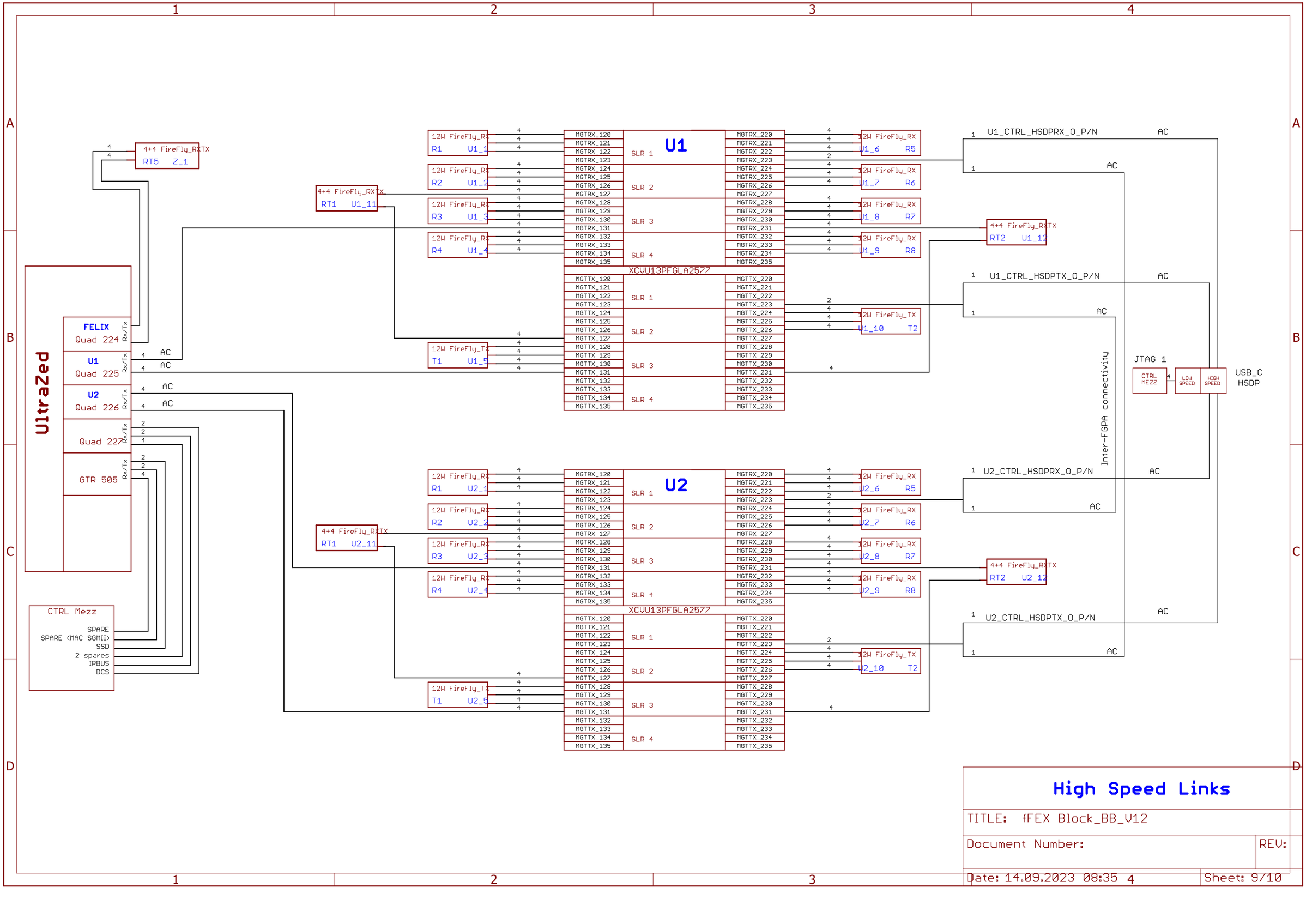

High Speed Links

TITLE: fFEX Block_BB_V12

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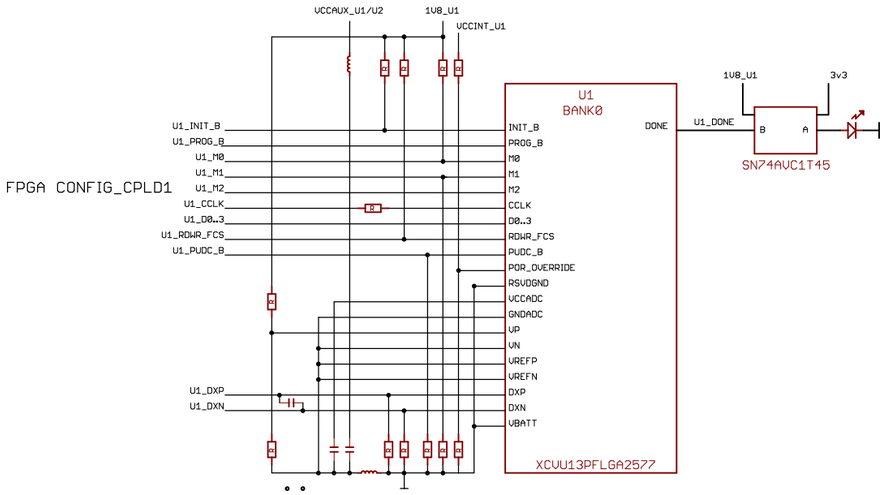

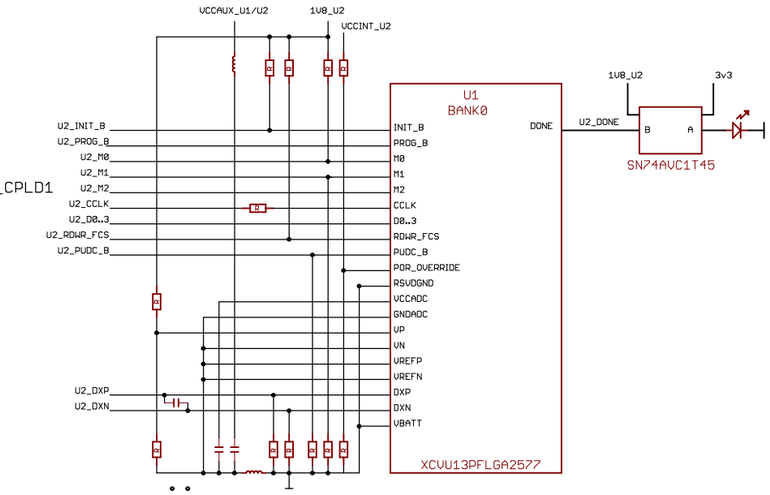

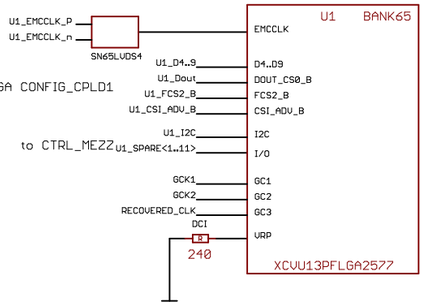

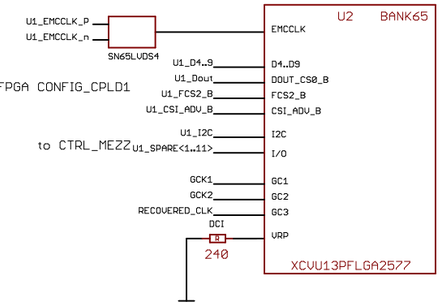

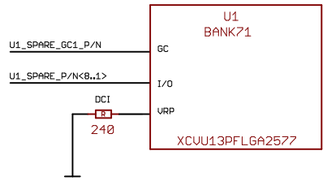

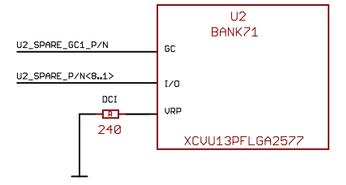

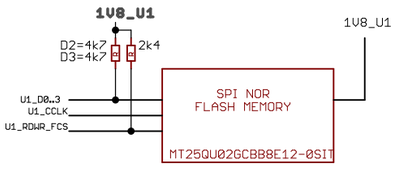

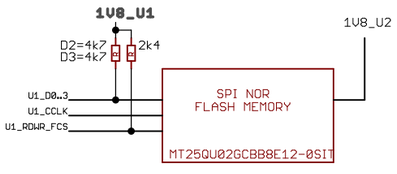

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