

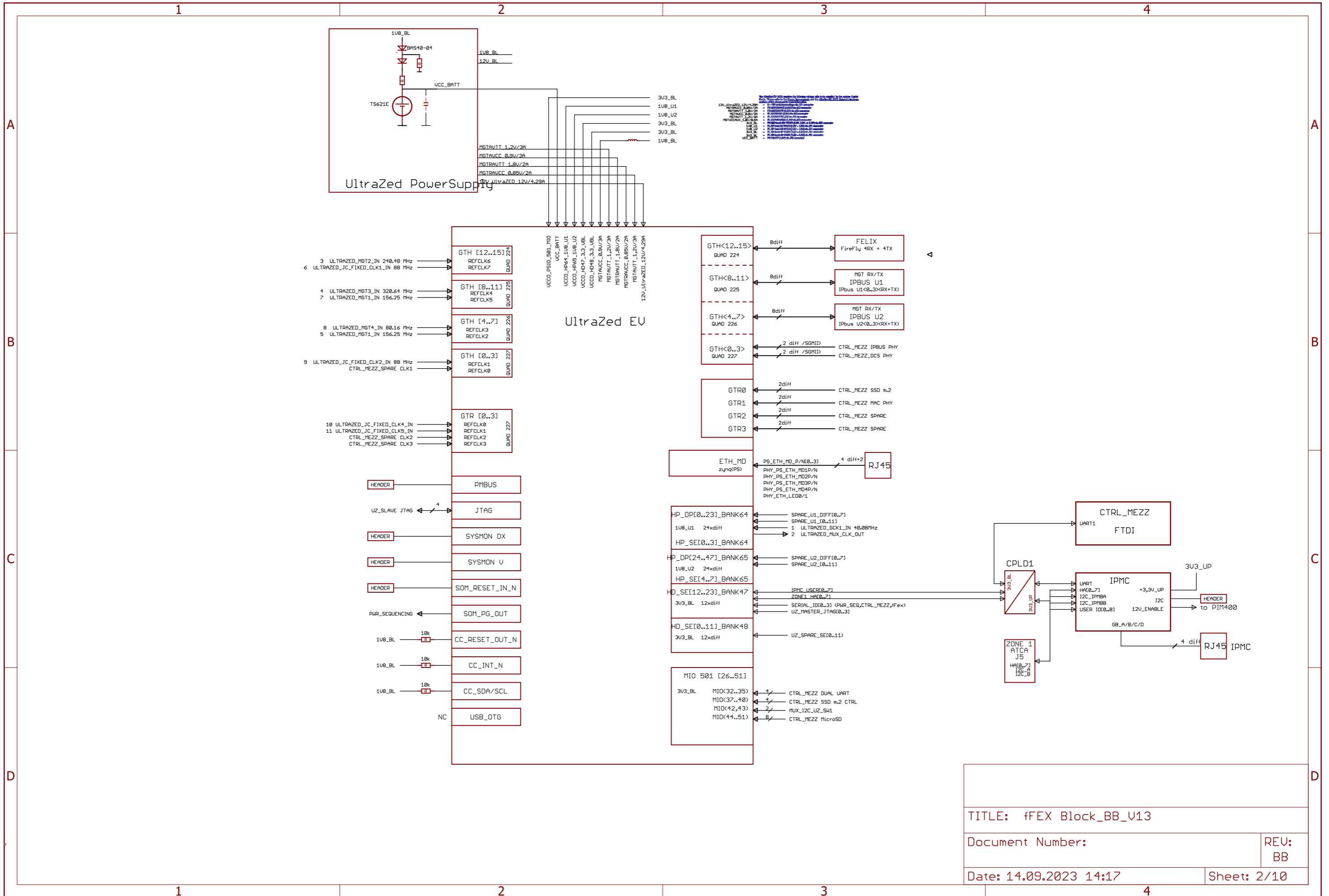
Sequencing an 3v3_UP ?????

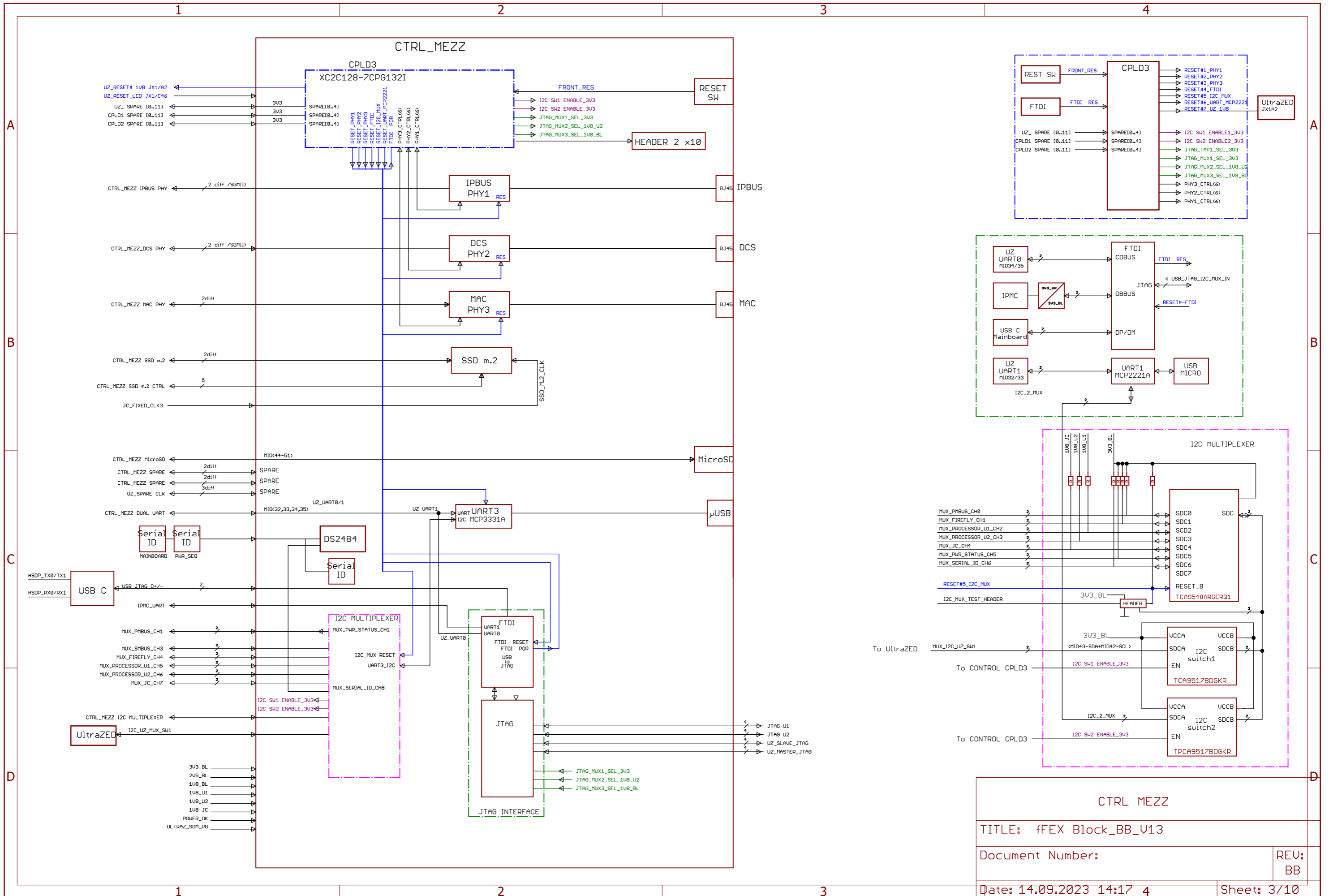
has to be sorted

$UXx = 0.573 - 1.375V$
 $UPx = 0.573 - 1.375V$
 $1.250 - 3.000V$
 $2.500 - 6.000V$
 $UH = 2.50 - 6.00V$
 $= 6.00 - 14.40V$

Dual 50A or Single 100A VIN: 4.5V to 16V UOUT: 0.6V to 1.8V LTM4700 RUN1 P6000 RUN2 P6000 PMBUS	QUAD 31.25A or Single 125A VIN: 4.5V to 16V UOUT: 0.5V to 3.3V LTM4681 RUN1 P6000 RUN2 P6000 PMBUS	Dual 6A or Single 12A VIN: 2.9V to 20V UOUT: 0.4V to 5.5V LTM4681 RUN1 LT718 RUN2 LT718 PMBUS
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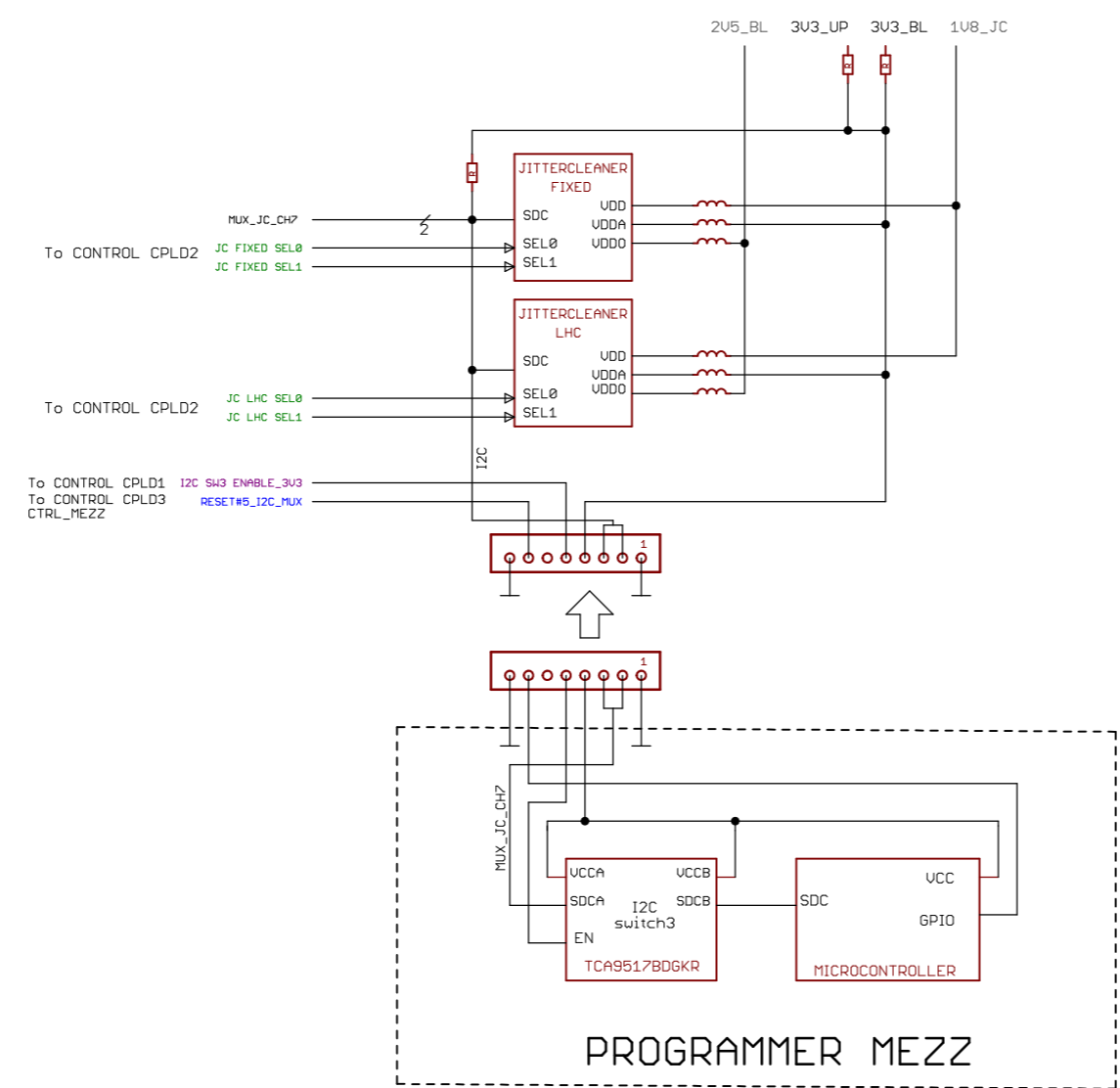
POWER SUPPLY MAINBOARD	
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Document Number:	REV: BB
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CTRL MEZZ	
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Document Number:	REV: BB
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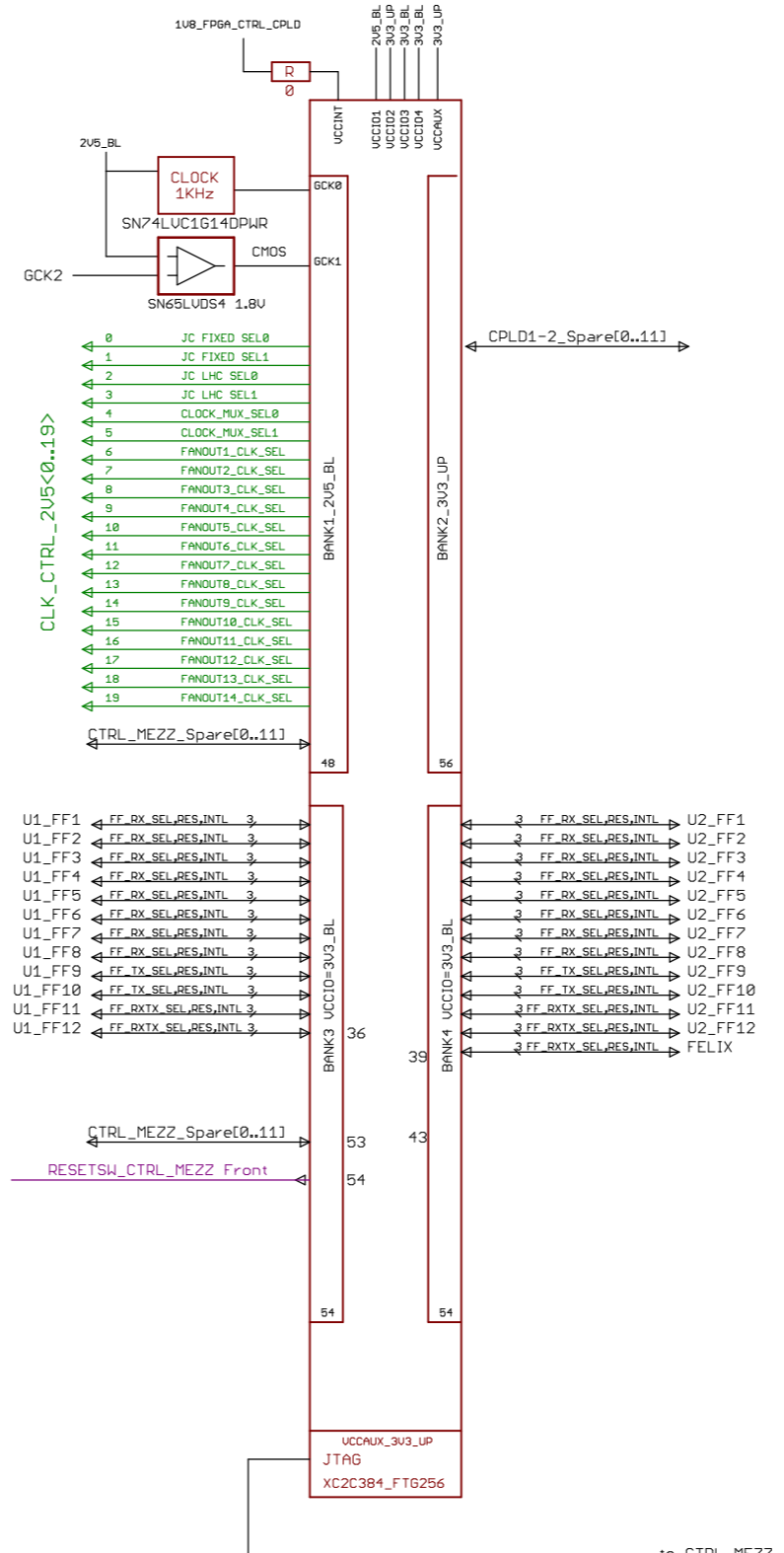
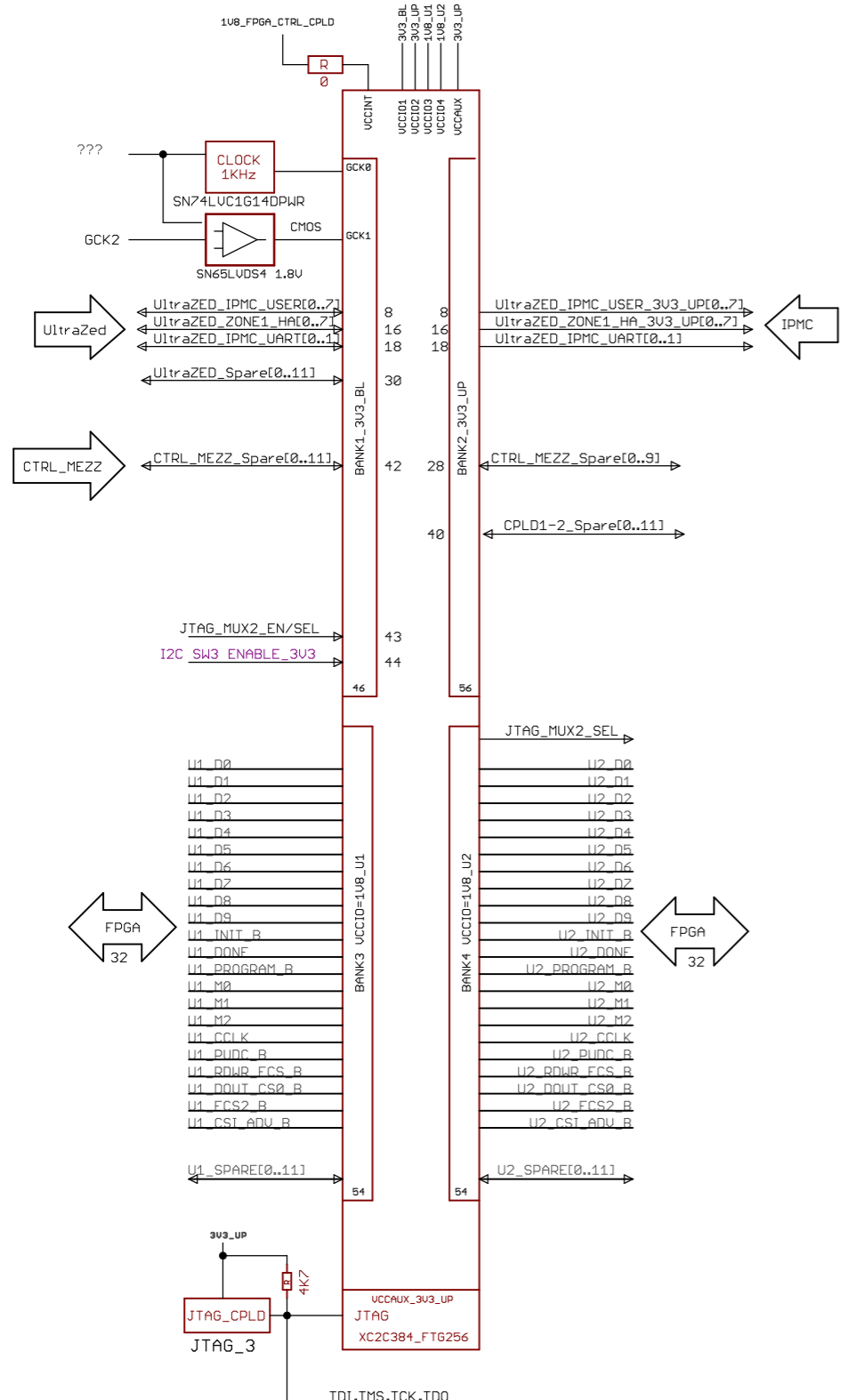
JITTER CLEANER I2C



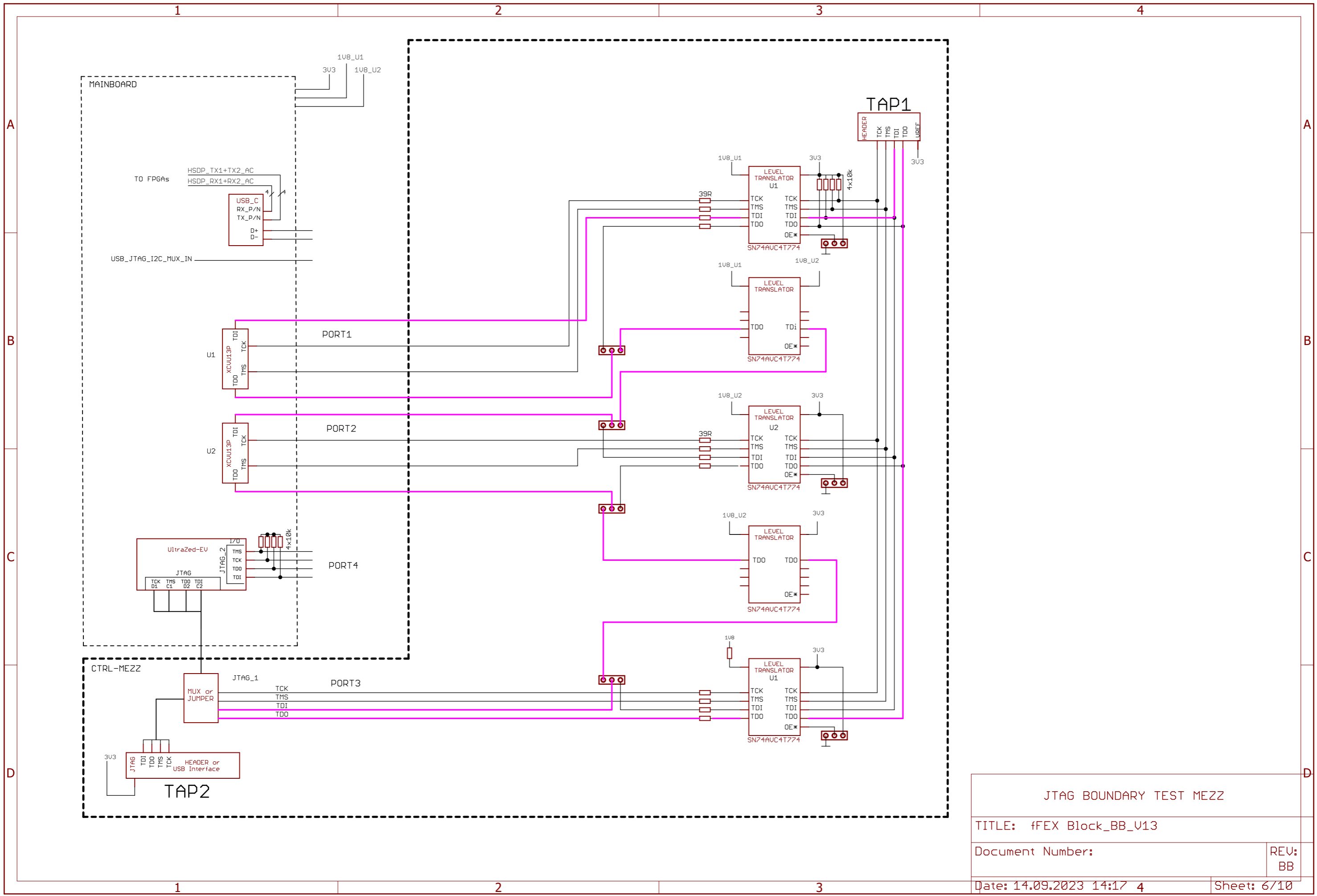
Jitter Cleaner	
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Document Number:	REU: BB
Date: 14.09.2023 14:17 4	Sheet: 4/10

FPGA CONFIG_CPLD1

FireFly CONTROL CPLD2

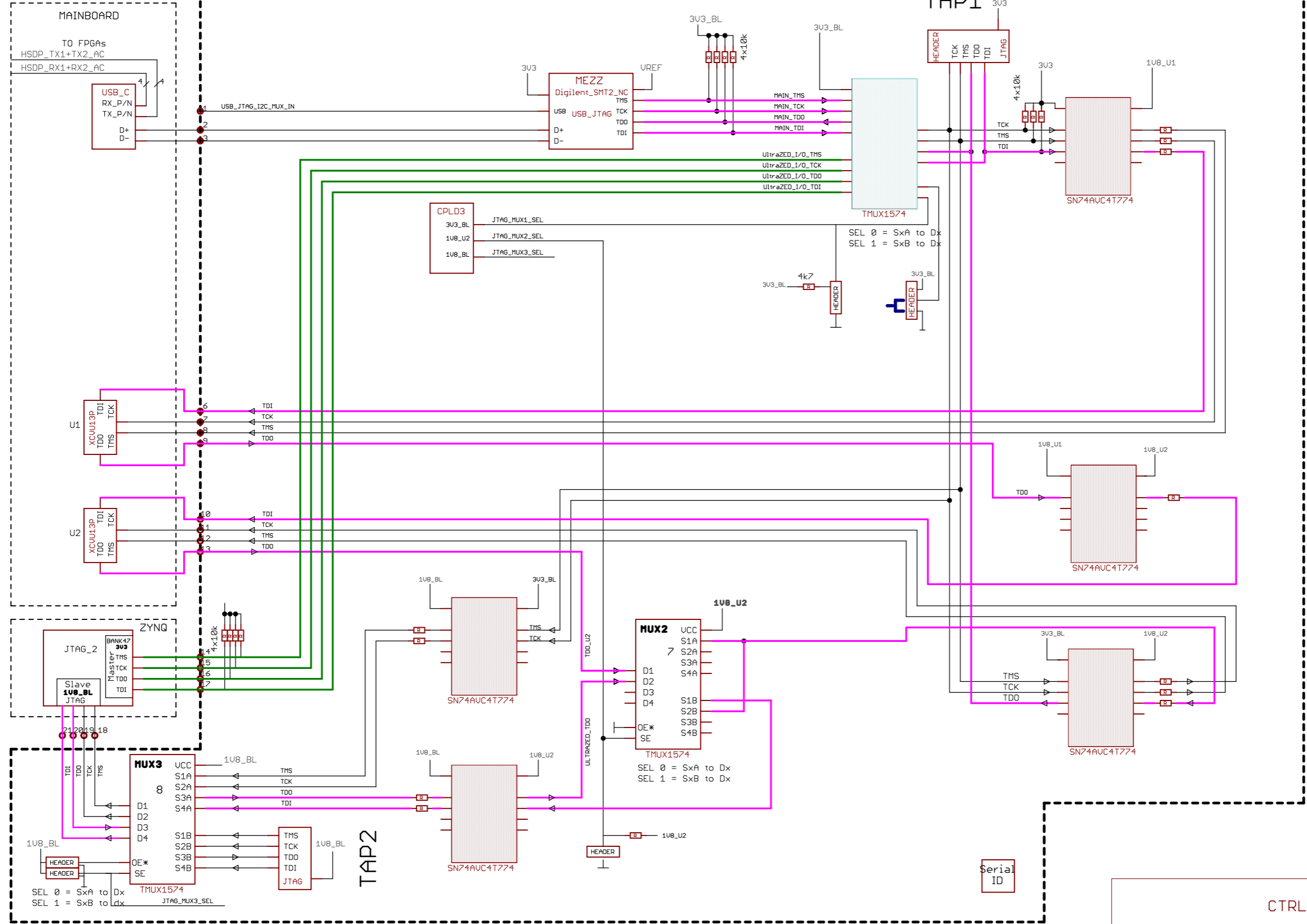


CONTROL CPLDs	
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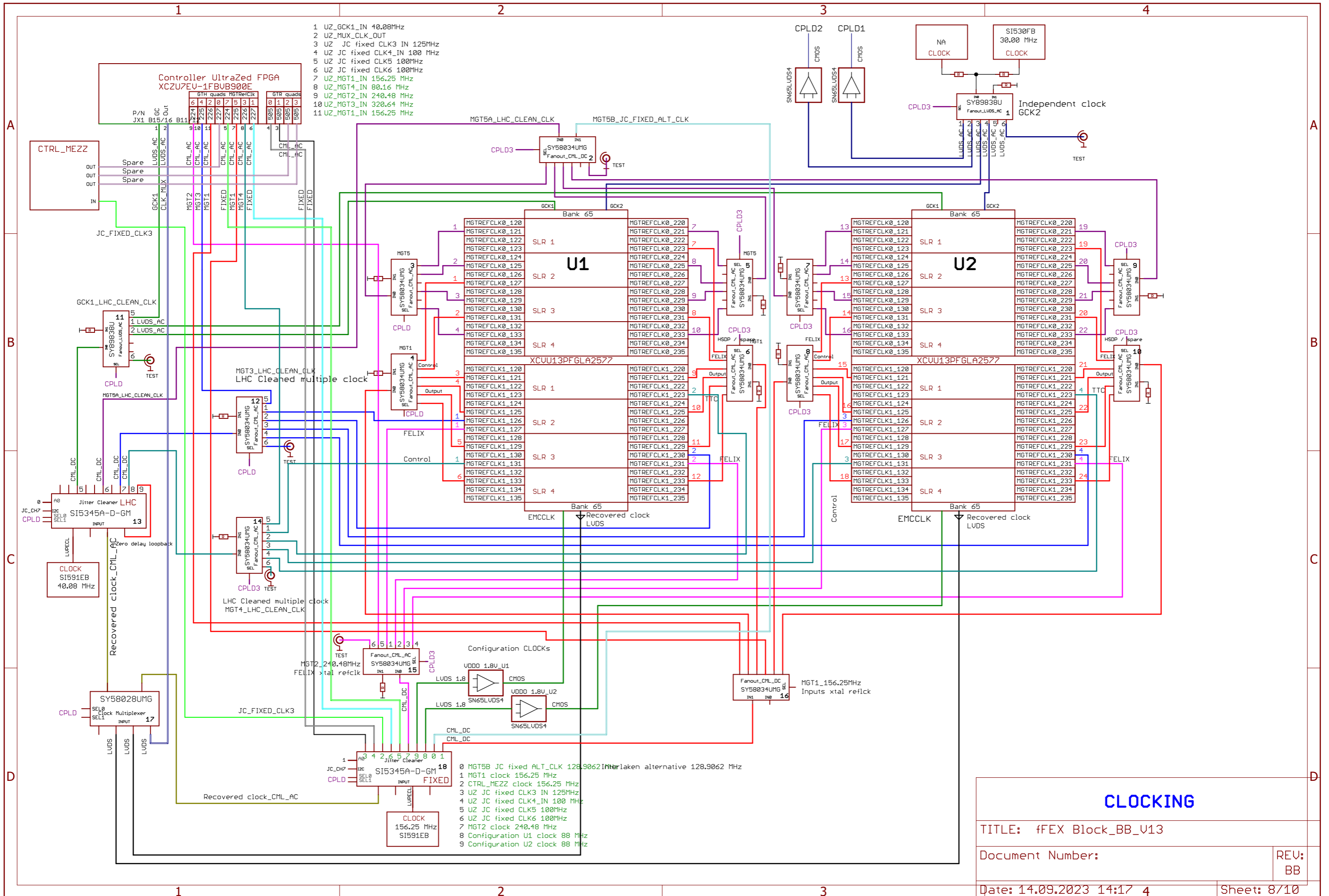


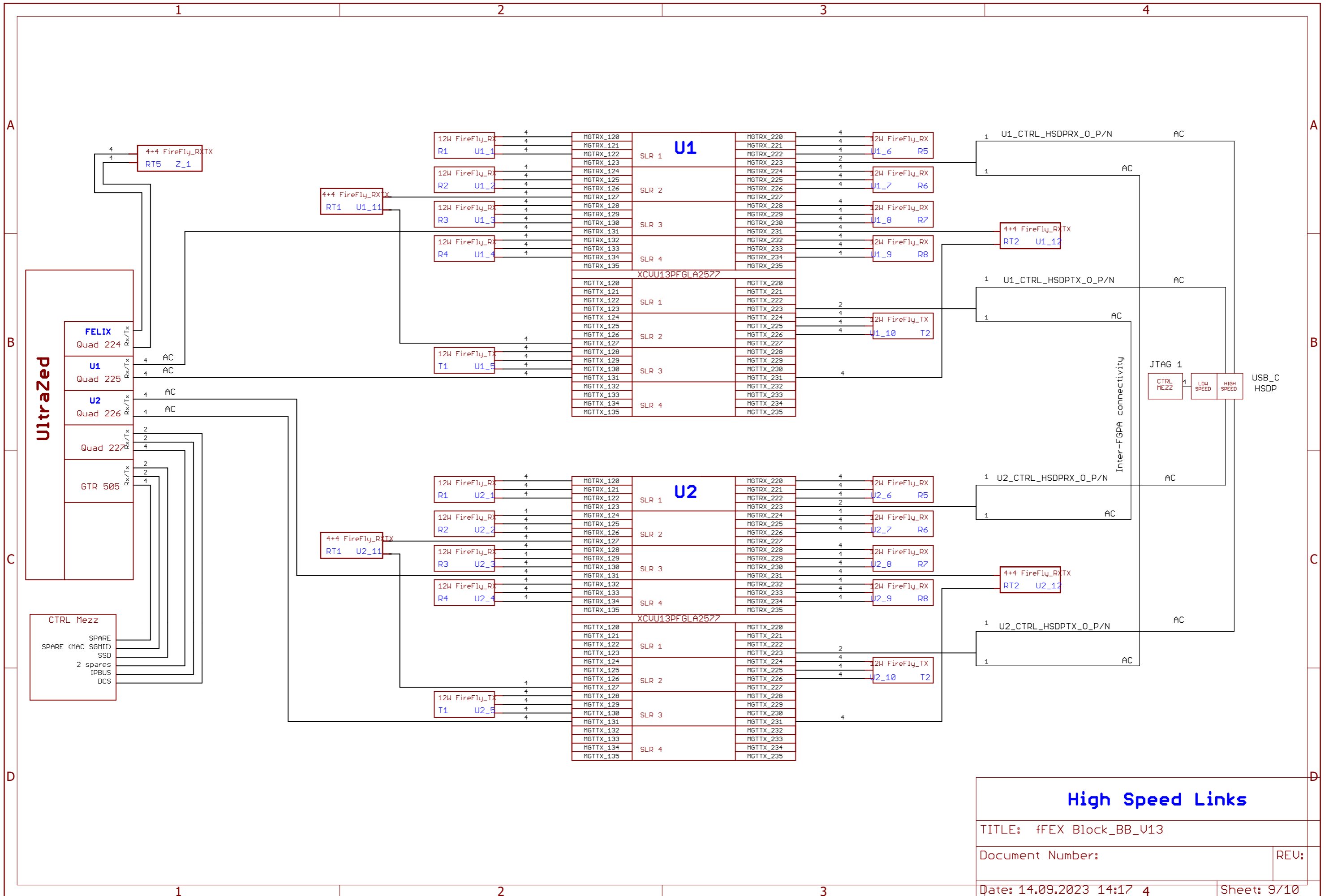
JTAG BOUNDARY TEST MEZZ	
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CTRL MEZZ - JTAG INTERFACE



CTRL MEZZ	
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High Speed Links

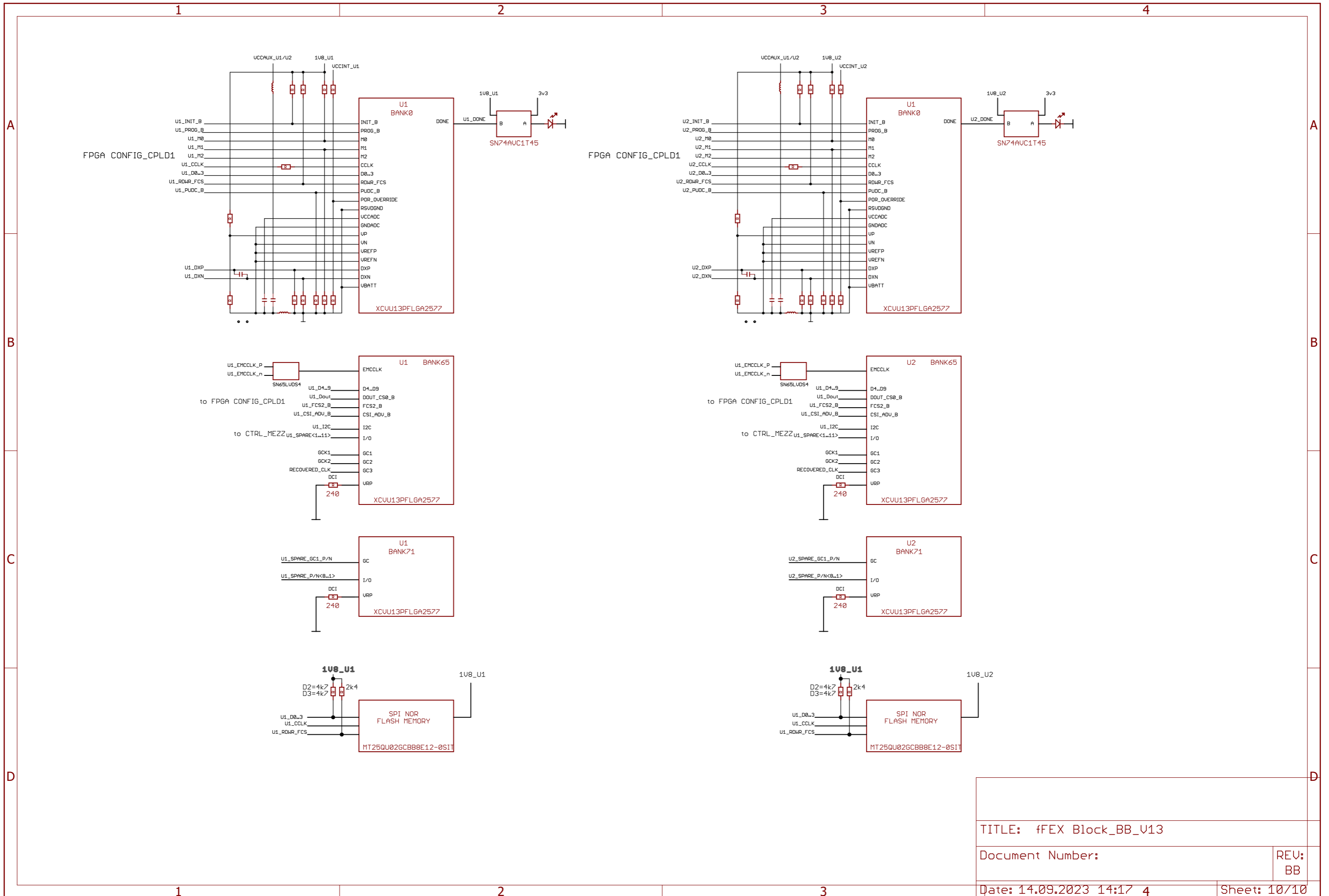
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Sheet: 9/10



TITLE: fFEX Block_BB_U13	
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