Important Product Information

Xilinx Device Errata
Virtex-II Family

Dear Xilinx Customer,

Thank you for your interest in Virtex-II devices. We would like you to be aware that under certain application and operating conditions, Virtex-II devices have shown possible issues with proper initialization of the device during power-up cycle. This errata applies to all Virtex-II family devices in all packages.

How to Determine Whether This Applies to Your Design (all conditions must apply)

- If Vccint is applied to the FPGA after Vcco/Vccaux, and
- If the Vccint ramp rate is longer than 10 msec, and
- If the configuration mode is set to Master Mode

General Description:

During power-up of the Virtex-II devices, under the conditions stated above, the FPGA might fail to initiate the CCLK and might fail to signal proper initialization by enabling the INIT pin. Failure to initiate CCLK consequently fails the configuration cycle of the FPGA in Master Mode.

Solutions:

These recommendations are offered to resolve this issue and can be applied at various stages of design and/or manufacturing cycles, as necessary. You need to consider only one of the following solutions:

1. Apply Vccint before or in tandem with Vcco.

2. If Vccint is applied after Vcco, assure the Vccint ramp rate of ≤10 msec.

3. Add a 1µf capacitor from the PROG_B pin (which has an internal pull-up to Vccaux) to ground.

4. Reset the PROG_B pin after power-up cycle to initiate CCLK.

If there are any issues or you have additional questions, please contact your Xilinx FAE or Xilinx Hotline for assistance. See: http://www.xilinx.com/support/services/contact_info.htm for the phone number in your area.