JEM Testing

Rainer Stamen (Universität Mainz)

Jem PRR

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Connectivity Tests

System Tests

Software

Connectivity Tests

To be performed at Mainz and CERN:

- after preproduction (1 week)
- during volume production
- before installation

Confirm channel mapping and connectivity

- LVDS - Input/Jet/Sum FPGA
- FIO tests
- glink tests

Not to be done

- stress tests (-> system tests)
- high statistics (-> system tests)

Connectivity Tests

LVDS - Input/Jet/Sum FPGA

source LSM (running 1) -> FPGAs -> readout Spies on FPGAs

- dump data
- standalone program for checking

-> alternative Firmware check (high statistics)

Status:

test vector:	to be modified
readout:	ready
standalone checking program:	to be done

Connectivity Tests

FIO tests

-> neighbouring boards have to be connected and read out

source Playback memories (running 1) -> FIO

-> readout Spies on neighbouring Jet-FPGAs

- dump data
- standalone program for checking

Status:

test vector:	ready
readout:	ready
standalone checking program:	to be done (done by hand so far)

Connectivity Tests

glink tests

source FPGAs (ramp) -> DSS

-> readout DSS

- check increasing pattern

Status

Firmware (pattern generation): ready

readout ready

checking ready

System Tests

System tests:

- to be performed at RAL/Birmingham and CERN
- after preproduction (10 JEMs + CMMs + CPMs)
- before and during installation

Stress patterns and high statistics:

- use only boards which pass all other tests before
- VME noise
- LSMs as input
- alternating 0,1s + signal (Jet at threshhold)

Software

- ready
  - test vectors (mostly)
  - readout of Spies
  - Glink checking program
- to be done
  - standalone checking program for patterns
  - timing software
- storage of test results
  - depends on amount of data we want to store
  - EXCEL spread sheet or Heidelberg database

JOHANNES GUTENBERG UNIVERSITÄT MAINZ