ATLAS Level-1 Calorimeter Trigger Upgrade

Backplane Tester Module

Project Specification

Version 0.2b

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1 Introduction

This document describes the specification for a backplane tester module, built to measure bit error rates on the L1Calo trigger processor backplane.

1.1 Overview

The Cluster Processor (CP) and the Jet / Energy Processor (JEP) share a common custom-made monolithic backplane carrying all communications signals used in the respective processors. There are VMEbus (VME⁻⁻), timing control (TTC), slow control (CAN), and real-time data signals routed across the backplane. The real-time data path on this backplane connects neighbouring processor modules (in total 14 CPMs or 16 JEMs per crate) to one another and collects data from the individual processors to consolidate them in two merger modules (CMMs), located to the left and to the right of the processor modules. The merger transmission lines have so far been operated successfully at 40 Mbit/s data rate. First measurements suggest that the backplane might be usable at higher data rates. Screen shots of eye diagrams are shown in Figure 1.
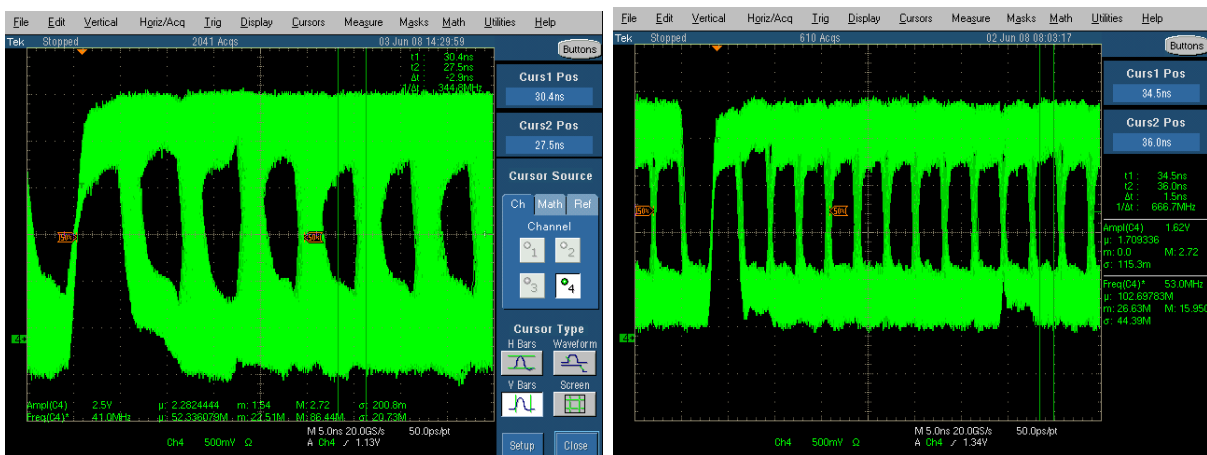

Figure 1: Data at 160 Mb/s source terminated (left) and 320 Mb/s sink terminated (right)

The module described here is built to qualify the merger transmission lines for increased data rates. To that end it will be operated in the two CMM slots in the processor crates and will analyse incoming data, so as to determine bit error rates at selected data rates.

The backplane test module carries circuitry to analyse the data in real time and accumulate error statistics. VME access to the module will be provided so as to configure the module and read out error counters. Module timing will be based on the LHC TTC system. The electrical representation of the TTC signal is available on the backplane at LVPECL level. Since the module is intended to be a test module only, the DCS interface, that's found on all L1Calo modules so far, will not be implemented on this module. Additional circuitry may be added to the module, beyond the bare backplane tester functionality, since in the course of hardware development for the L1Calo upgrade further component tests might be necessary, which can thus be done at limited overhead.

The backplane tester will be built entirely from programmable logic. Therefore functionality will be limited by logic capacity of selected devices and PCB based connectivity only. The baseline implementation will be a single FPGA for the real-time data path plus a CPLD for basic VME access.

The modules currently operated in the L1Calo trigger processor crates and used along with this backplane test module are described at http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html.

1.1.1 Real-time data path

Data from the up to 16 processor modules are received on 25 signal lines per module (Figure 2). On the current CMMs they are used for 24 data bits plus a single parity bit. They are strobed in at the LHC bunch clock distributed via the TTC system. On a future incarnation of the CMM, operating at higher data rates, the accuracy

of the TTC sub-system might be inadequate and source synchronous data transmission might be required. Therefore the backplane tester will allow for a clock signal being forwarded along with 24 bits of data. If not needed as clock lines, the signals can be used as ordinary data lines.
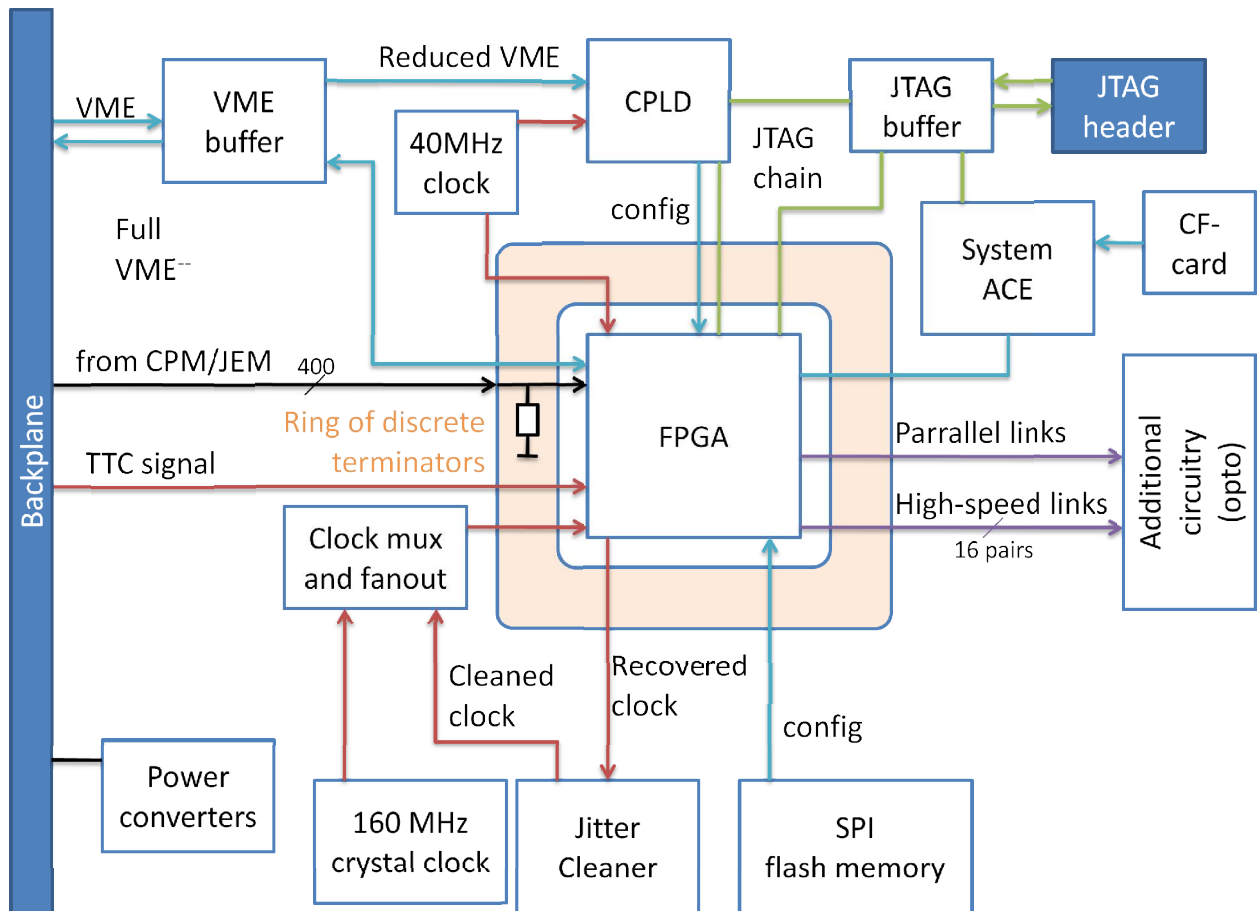

Figure 2: Block diagram of backplane tester module

1.1.2 Timing, control and VME access

The global timing of the module is derived from the TTC signal available as an encoded LVPECL differential signal. On the backplane tester the encoded data channel is not required. Therefore the clock will be extracted in the FPGA. So as to improve timing accuracy, the recovered clock will be subjected to a jitter reduction in a commercial device and redistributed as a differential LVPECL signal.

VME access to the module will be implemented in programmable logic. FPGA configuration will be done processor-based or via flash ROM.

Connectivity tests of all B/Scanable components will be possible through a JTAG header.

2 Functional requirements

The role of the backplane tester is to determine bit error rates on the incoming merger lines and make error statistics available via the VME bus.

This section outlines the requirements for all functions of the backplane tester. Implementation details are located in Section 3 of this document. For information on interfaces with other system components, see section 7.

2.1 Real-time data path

The requirements are:
- Receive 25 signals (Px_0-Px_24) from the processor backplane from each of the 16 processors per crate (total signal count is 400, signal type is 1.5V-2.5V CMOS)
- Terminate signals into 60 Ω resistors at half rail voltage, if required (soldering option)
- Run clock line Px_0 into a suitable (clock) pad of the FPGA
- Run data lines Px_1-Px_24 into suitable I/O pads
- Internally terminate the signals into 60 Ω Thevenin equivalent, if required (FPGA configuration)
- Subject clock and data lines to phase correction (VME controlled)
- Compare incoming data to expected pattern
- Calculate bit errors and make error count available to VME readout

2.2 Clocks

The backplane tester module makes use of both a global TTC clock and forwarded clocks from each of the modules.
The requirements are:
- Receive and terminate differential PECL level TTC signal from the backplane
- Recover the clock from the TTC signal
- Attenuate clock jitter
- Fan out global clock
- Receive and handle forwarded clocks as described above

2.3 VME

The backplane tester needs to be controlled and read out via the VME‾ bus described elsewhere.
The requirements are:
- Buffer all VME data, address, and control lines near the backplane connector
- Route a subset of the signals to a CPLD implementing basic VME functionality for limited access immediately after power-up
- Route all signals to the FPGA carrying a fully functional VME interface after configuration

2.4 JTAG access

Even though only a limited number of JTAG accessible devices will be employed, connectivity tests should be done to the extent possible.
The requirements are:
- Connect all JTAG devices to a chain
- Buffer / terminate JTAG signals as necessary
- Allow separation of the FPGA chain for easier configuration download

2.5 Configuration

The FPGA needs to be configured prior to board operation.
The requirements are:
- Provide a standard JTAG header for FPGA configuration during firmware development
- Provide an SPI flash memory for automatic configuration upon power-up
- Provide a VME accessible configuration path through the VME CPLD

2.6 Board level issues: Power and line impedances

The backplane tester is a large module, carrying large numbers of high-speed signal lines of various signal levels. FPGAs tend to generate considerable system noise. Due to built-in analogue circuitry (PLLs, high speed links) they are susceptible to power supply noise. Strict rules concerning PCB layout and bypass capacitors have to be followed to control system noise. The majority of signal lines carries signals of up to 320 Mb/s. Therefore track impedances will have to be tightly controlled. The processor FPGA will have considerable power dissipation of the order of 15W. A heat sink will be required.

The requirements with respect to signal integrity and thermal management are:
- Use low-noise local step-down regulators on the module, placed far from susceptible components. Observe FPGA ramp-up requirements
- Allow for external control of the input bank V_{CCO} voltage to adapt to JEMs and CPMs
- provide a source/sink termination voltage regulator of suitable current capacity, regulating to input bank mid rail voltage
- run all supply voltages on power planes, facing a ground plane where possible, to provide sufficient distributed capacitance
- Provide at least one local decoupling capacitor for each active component
- For FPGAs, follow the manufacturer's guidelines on staged decoupling capacitors (low ESR)
- Observe capacitance limitations possibly imposed by the voltage convertors
- Minimise the number of different V_{CCO} voltages per FPGA to avoid fragmentation of power planes
- Route all long-distance high-speed signals on properly terminated, controlled-impedance lines of 10% tolerance:
  - Route single ended incoming merger lines with 60Ω impedance
  - Terminate single ended input lines close to the FPGA
  - Route differential signals on short micro-strip lines of 100 Ω differential mode impedance
  - Use internal termination of differential lines where possible
  - Terminate all other differential lines close to the sink into 100 Ω resistors
  - Run FPGA configuration and FPGA JTAG clock lines on 60 Ω point-to-point source terminated lines
- have all micro strip lines facing one ground plane
- have all strip lines facing two ground planes or one ground plane and one continuous power plane
- avoid sharply bending signal tracks
- minimise cross talk by running buses as widely spread as possible
- minimise the lengths of all non-terminated high-speed signal lines
- route all clocks into dedicated clock pads (FPGA, CPLD)
- provide the processor with a suitable heat sink

3   Implementation details

The backplane tester is a module built from programmable logic devices. Data processing is performed at multiples of the LHC bunch clock, up to 320 Mb/s. Most signals enter and leave the module through rear edge connectors via the backplane. The module is connected to the backplane through more than 800 signal and ground pins, plus three high-current power pins.

The backplane tester is a 9U (366mm) module that fits a standard 9U 21-slot crate with IEEE 1101.10 mechanics. The module is mechanically strengthened with help of bracing bars along the top, the bottom, and the backplane. ESD strips are provided at top and bottom, connected to signal ground via 1M resistors. The front panel is not electrically connected to the module and will be grounded through the crate mechanics only. The module is built on a multi-layer PCB with ground and power planes and impedance-controlled strip line and micro strip layers. A sketch of the module is shown in Figure 3.
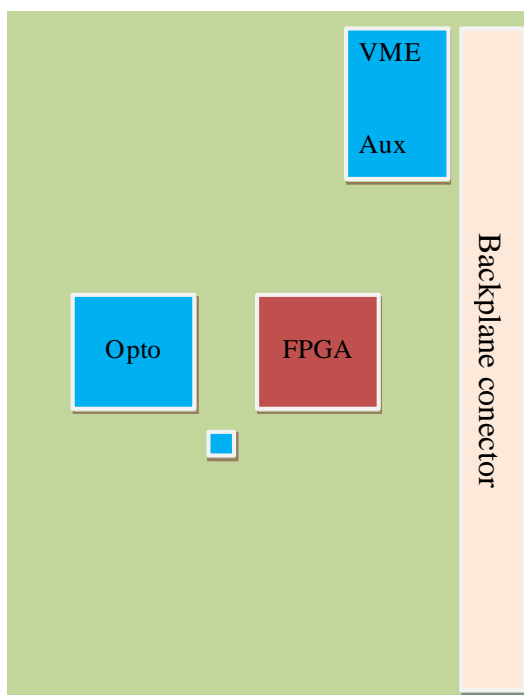

Figure 3 : backplane tester module

3.1   Real-time data path

The backplane tester module receives real-time data from the CPM / JEM boards. Since the module is built for test purposes only, there is no limit imposed on latency. Data will, however, have to be processed in real-time, since the backplane transmission should be tested down to very low error rates. This precludes CPU based data analysis.

3.1.1   Signal reception

The incoming real-time data are routed from the backplane pins to the FPGA on 60Ω strip lines. The track length on the module is of the order of 15-25 cm. The total signal track length comprises the sections on the processor modules, the backplane tracks up to full backplane length, and the tracks on the tester. On the backplane tester no attempt will be made to route signal tracks of equal length, since on modern FPGA families fine-grain skew control is available on all input pins. A software based delay scan will be employed to measure and adjust the channel timing at the input registers.

The incoming signals will have to be terminated to the line impedance. Baseline termination scheme is FPGA-internal "DCI" termination. The termination uses a Thevenin equivalent to terminate to mid-rail voltage. This termination scheme will dissipate a significant amount of power. With 2.5V (nominal) CMOS signals and 2.5V input rails the total power dissipation on 400 inputs might be of the order of 15W. Actual dissipation depends on the actual voltage swing. As a backup solution a fraction of ??% of the channels will be equipped with discrete terminators. The termination voltage will require a source/sink capable regulator with a nominal voltage of half the voltage of the FPGA input bank supply. This bank voltage should be controllable so as to allow for customization to JEM and CPM needs. Most likely the JEMs would be operated with 1.5V low impedance CMOS drivers that require parallel termination. The need for parallel termination of the CPMs' 2.5V source terminated signals is not yet clear.

3.1.2 FPGA

All signal conditioning and processing takes place in a single FPGA. A Virtex-5 device (XC5VFX70T) in an 1136-ball package has been chosen. In addition to its parallel link connectivity of 640 lines, used up by incoming links and control lines, the device has 16 high speed serial links. They will be wired to connectors suitable for connection to SNAP12/MSA and SFP optical modules. This functionality will be required for Mainz ATLAS (and non-ATLAS) research activities anyway. The high speed link and electro-optical design is not scope of this document.

So as to operate incoming parallel links off one forwarded clock per JEM/CPM slot, regional clock resources in the FPGA must be used. Regional clocks are tied to I/O banks, of which on the chosen device unfortunately only 14 are large enough in pin count to allow for all 24 data lines to be strobed into the device in the most effective way (use of serdes block)[1]. This is not considered a problem on the backplane tester module. It will, however, make firmware design somewhat more complicated.
The algorithm inside the FPGA is taking a low amount of resources. Input deskew will take place on the I/O pads under software control. Deserialisation will be done on most input pins in dedicated serdes hardware. Simple error detection might consist of parity checks and/or pattern comparison. A very simple data pattern suitable for fast comparison is a binary counter pattern. Any pattern that can be generated and detected in programmable logic might be used. Playback/spy operation with CPU based comparison is not anticipated.

The numbers of errors observed will be counted in a single register per channel and can be read out via VME.

3.2 Timing and control

The VME¨ interface implements a subset of standard VME-64 signals and commands. It allows for D16/A24 access to the module. 3.3V-CMOS bus transceivers are used. To improve testability, boundary scannable devices have been chosen . Basic VME access is implemented in a CPLD. The CPLD reads the geographic address lines of the module to determine the VME address range. It poses as a CMM. The CPLD guarantees that any access to the module's address space is terminated with a /DTACK signal. Data and addresses are fed into the FPGA. For ease of implementation the VME port is operated synchronous with the bunch clock rate. This scheme is currently in successful operation on the JEM.

JTAG boundary scan access is implemented in 3 separate chains connecting up CPLD, FPGA, and non-programmable devices. JTAG will be used for connectivity tests after module assembly. To this end the three chains will be joined via a common connector. The CPLD will be flashed through its JTAG interface. The FPGA can be configured via JTAG as well, if required for firmware development.

FPGAs are RAM-based programmable logic circuits that need to be configured after power-up. The default configuration method is via an on-board SPI flash memory. All necessary lines will be made available to connect, if required, to a System ACE sub-system that has been the standard configuration circuit for some of the L1Calo processors so far.

For debug purposes configurations can be loaded into the FPGAs directly from VME. This route bypasses the flash memories and makes use of the JTAG configuration path of the FPGA. The required software is available for the Virtex-II devices on the JEM. It will have to be adapted to Virtex-5 if required for the backplane tester. Alternatively serial slave configuration mode might be used.

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[1] Alternatively global clock resources could be used, if available

System timing is based on clock and data distribution by the TTC system. All current L1Calo processor modules have their own TTCrx chip mounted on a TTCDec daughter module and can derive all required board level timing signals from the two deskewed bunch clock signals and accompanying command and data words. This scheme is considered unnecessary for the backplane tester. There is no obvious need for TTC data and control functionality. The only purpose is recovery of a global clock.

The TTC signal arriving from the backplane on a differential pair is terminated on the FPGA. The clock edge is extracted with help of an XOR gate. The resulting pulse train is divided to a clock signal and jitter is eliminated in a PLL on the FPGA. So as to reduce the jitter even further an external low bandwith PLL will be employed (part number National Semiconductors LMK03000). The clock signal will be fanned out by a PECL mux buffer. A low jitter 160 MHz PECL crystal clock will be provided as a backup.

4   Time line

The detailed design will start immediately (Oct.20, 2008). Schematic capture should be finished by mid November. Layout will take 3 weeks. PCB production and assembly is dependent on availability of a time slot with the manufacturer. PCB production and assembly in one stop shop, if possible.

5   Deliverables

Two PCBs will be made. Initially one of them will be assembled. Input terminators will not be assembled. Opto module connectors will be assembled if available in time.

6   Firmware and software

Firmware will be required for basic VME operation, for data reception and comparison to simple data patterns (parity check and linear ramp detection). The firmware style will be mainly behavioural VHDL code, text only, Xilinx ISE compatible.

VME computer based control software will be in C under Linux, command line controlled, no graphical interfaces, with access to low-level CERN VME routines.

7 Interfaces : connectors and pinouts

SYSRESET	1
A[23..1]	23
D[15..0]	16
DS0*	1
Write*	1
DTACK*	1
Total Number	**43**

Table 1 VME signals

7.1 Front panel

#	Socket type	Socket use

Add drawing and update tables !

#	LED colour	LED use

7.2 Backplane connector layout

For the backplane connector pinout see appendix B of the backplane specifications at

http://hepwww.rl.ac.uk/Atlas-L1/Modules/Backplane/BackplaneFDR1_1.pdf

8 Glossary

The following lists some of the terms and acronyms used in the text.

CMM	Common Merger Module
CP	Cluster Processor sub-system of the Calorimeter Trigger [2]
CPLD	Complex Programmable Logic Device
CPM	Cluster Processor Module [2]
CTP	Central Trigger Processor
DCS	Detector Control System
DLL	Delay-Locked Loop
FIO	Fan in / fan out signal lines on the backplane
FPGA	Field Programmable Gate Array
JEM	Jet/Energy processor module
JEP	Jet/Energy Processor sub-system of the Calorimeter Trigger
JEP crate	Electronics crate processing two quadrants of trigger space with 16 JEMs
JTAG	Joint Test Action Group
L1Calo	Level-1 calorimeter trigger
LVDS	Low-Voltage Differential Signalling
PB, Backplane	Multi-purpose high-speed common backplane within JEP and CP crate [2]
PHY	Physical layer interface chip
SMB	System management bus
TCM	Timing and Control Module [2]
TTC	Timing ,Trigger and Control
TTCdec	Timing receiver daughter module [2]
TTCrx	Timing receiver chip

9 Figures and tables

Change log:

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[2] Documentation available at http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html
and http://hepwww.rl.ac.uk/Atlas-L1/Modules/Components.html

2008-10-21 some cleanup
2008-10-17 add high speed links
2008-10-15 initial version