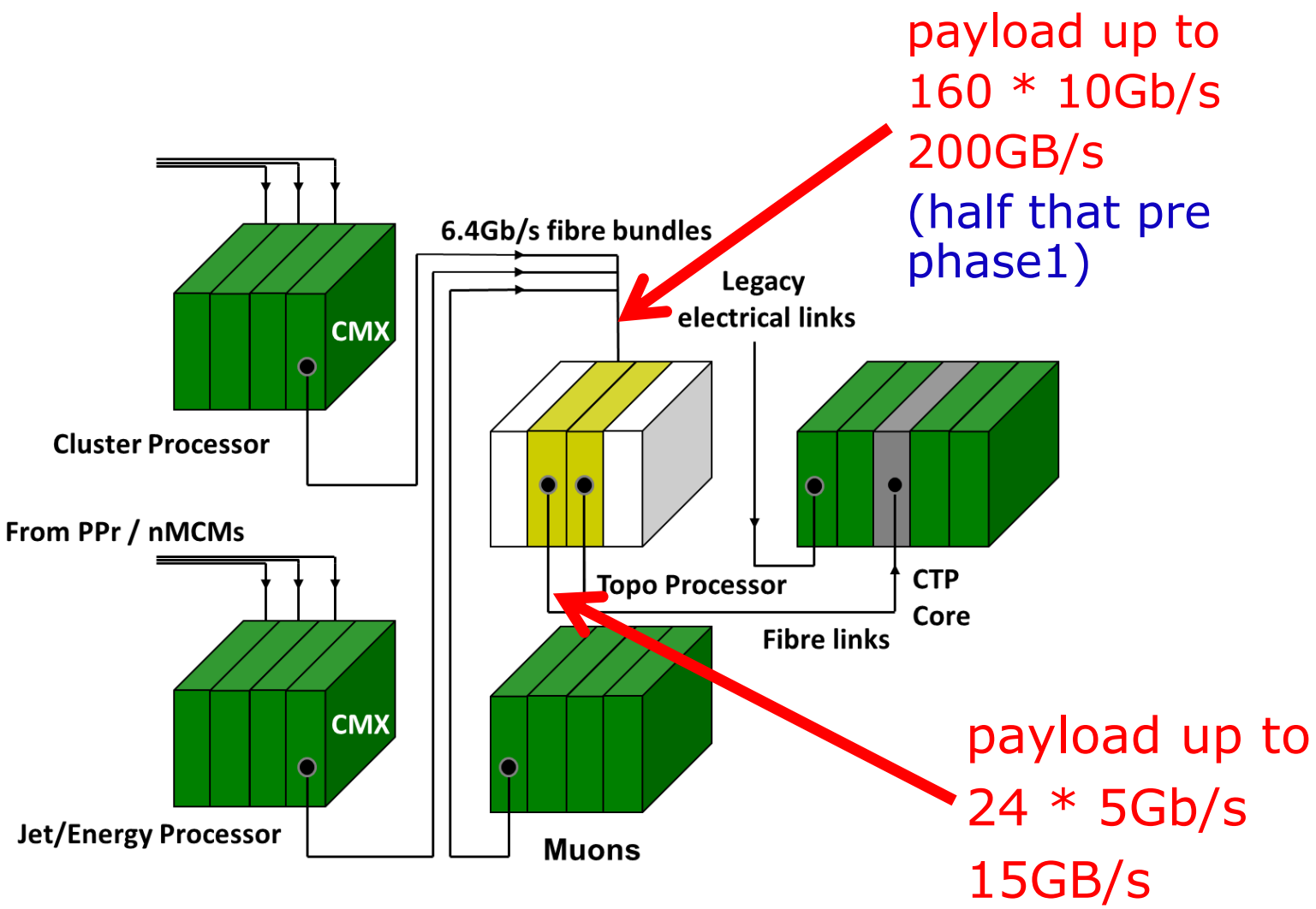
L1Topo review

www.staff.uni-mainz.de/uschaefe/browsable/L1Calo/Topo

Uli

Intro – LVL-1 2013/14



Intro

Allow for any conceivable topological algorithm:

Route a maximum fibre count / data volume into individual module / processor

- Bandwidth estimate :
  (cf. www.staff.uni-mainz.de/uschaefe/browsable/L1Calo/Topo/L1Topo_Algorithms_0_2.pdf)
  - Electrons, tau, jets, MET : 553 Gb/s (pre phase 1 , all available data)
  - Muons 267 Gb/s (phase 1)
  - Total aggregate bandwidth 820 Gb/s
  - Achievable @ 6.4Gb/s line rate
- Bandwidth available for phase 1 with FEXes
  - twice that @ 13Gb/s line rate
  - supported by FPGAs
  - Roadmap for pluggable opto components unknown
- Scalable in terms of bandwidth and processing power
  - FPGA type
  - Module count
- Consider some electrical, low latency real-time path

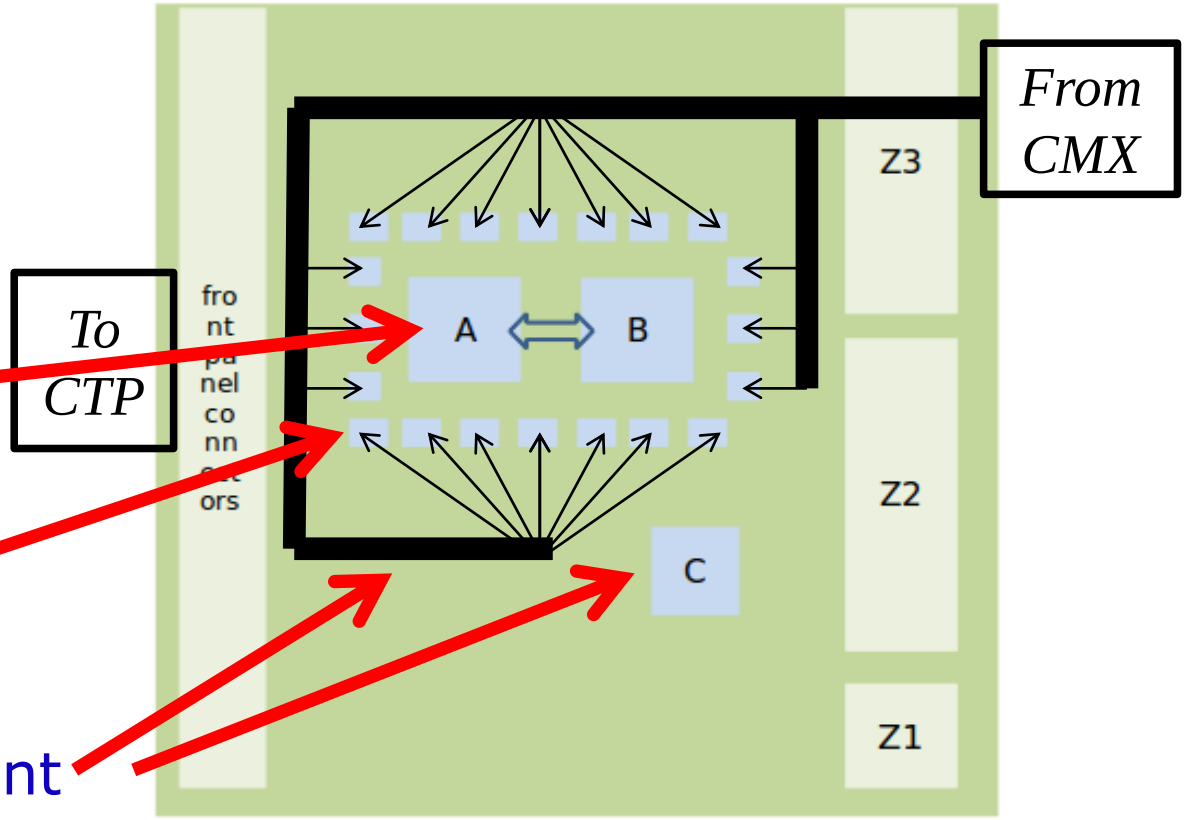
Floor plan, critical components…

Design goal : Keep compact, with short traces and no on-board signal duplication

Form factor : advancedTCA

→ require:

- 2 processor FPGAs
  A, B: XC7V485T
  → XC7V690T
- High-density mid-board o/e converters (miniPOD)
- High density fibre plant
- Controller XC7K325T (C)

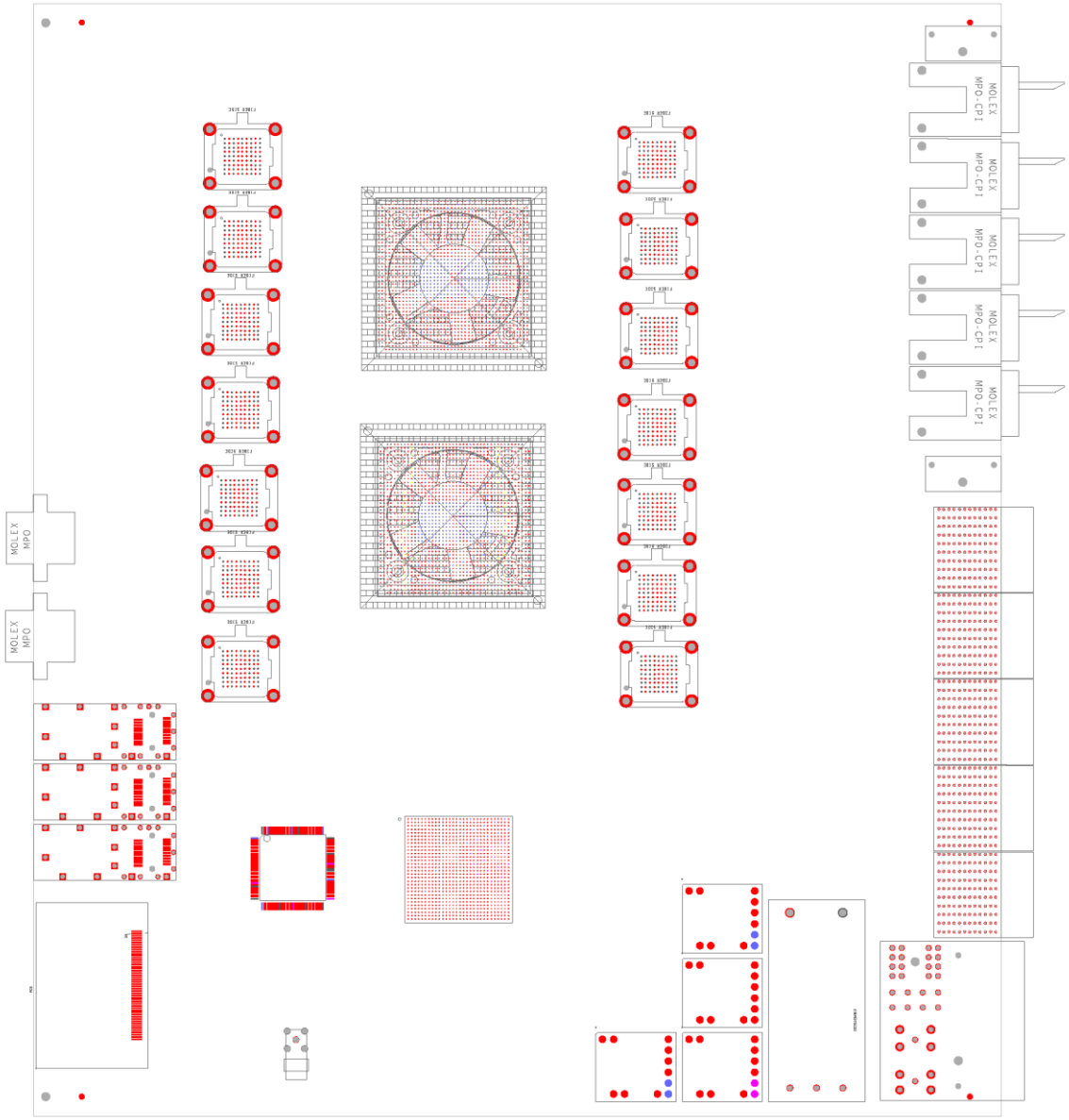


numerology

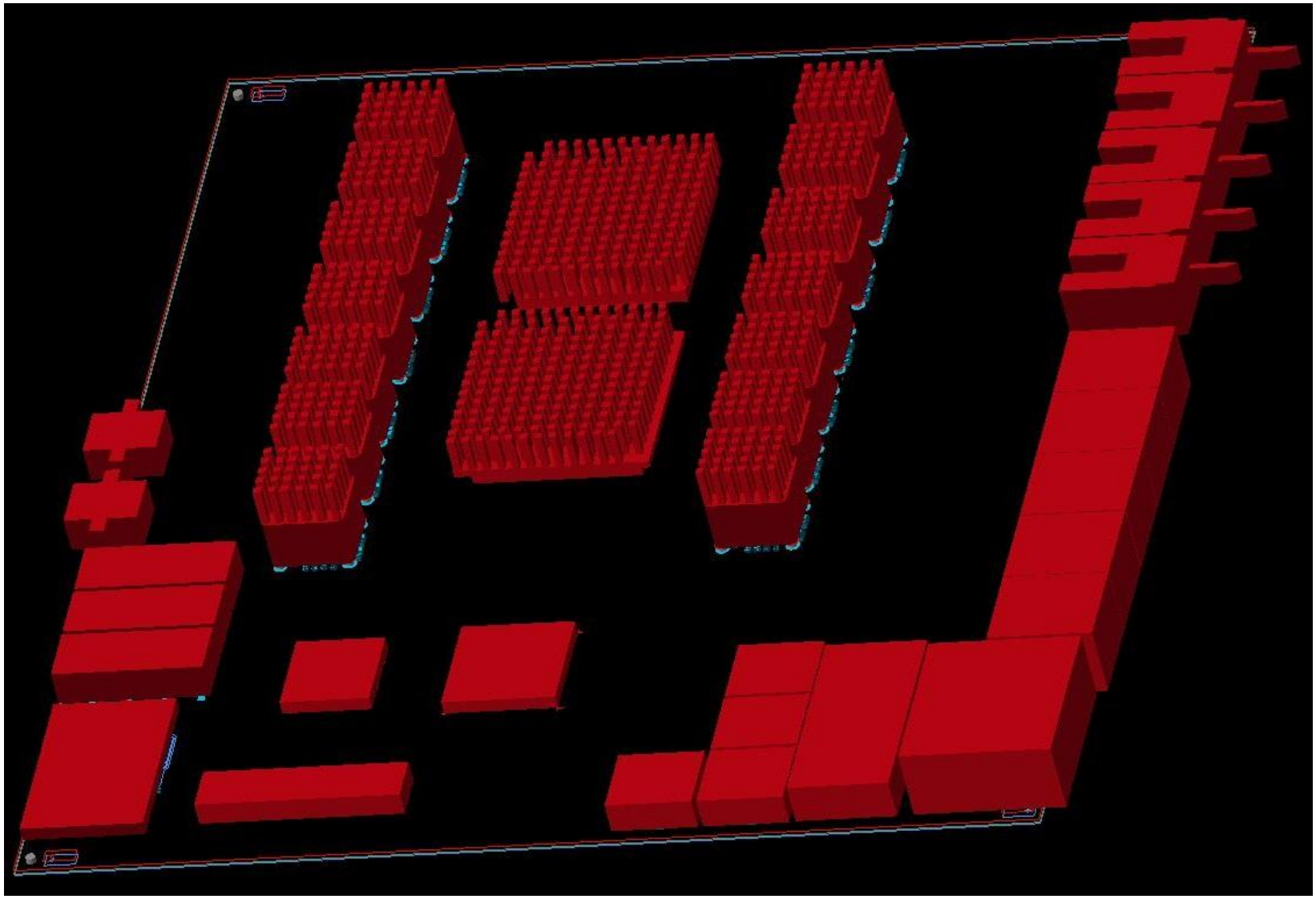
- Real-time input links: maximum bandwidth available on market: 160 *13Gb/s links per two FPGAs
- All links supplied from fibres, with 48-way connectors that fits 4 connectors
- Processor-to-processor bandwidth maximised (230 Gb/s)
- Real-time output optical 24 * 6.4 Gb/s +
- Electrical real-time path: 44 diff pairs total (1 bank per FPGA)
- Minimum 1 DAQ and ROI link each. Optional 12 fibres miniPod (?)

- Link count on prototype to be decided now: 112 v. 180

Floor plan, so far…



… and in 3-d



PCB status and components

- Detailed design under way
- FPGAs (production silicon) available end 2012 / early 2013
- Initial module(s) using engineering samples
- Opto transceivers to be ordered *now*
- Samples of fibre assemblies (48-way) to be ordered *now*
- Lead times seem reasonable

Opto modules : single manufacturer, NDA on docs

- Choice of device types
  - Round ribbon vs. bare (flat) fibre ribbon
  - No heat sink vs. heat sink

Fibre assemblies : probably several manufacturers, documents on the web

- Choice of # fibres per POD connector 48
  - Choice of Round ribbon vs. bare (flat) fibre ribbon

Need to make sure fibre assemblies actually fit the modules

MPO/MTP connector - define gender : male connector on processor side

(not so) randomly picked comments

Assignment of fibre links, if prototype device is smaller than production

- smaller number of PODs, all fully populated
- Use 690T-ES devices rather than 485T production silicon
  - Initial prototype is 485T ES anyway
  - Engineering silicon performance not guaranteed
  - Lead time expected similar
  - Can afford only one such 160-channel prototype module (or 2 485T based). All other money is CORE

RTDP line rate

- Make sure all links are able to operate at 6.4 and 10 Gb/s. 13 Gb/s optional. Depends on maximum miniPOD rate.
- Line rate gap for 485T. 9.6Gb/s impossible !

Electrical real-time I/O

- Define required bandwidth: sum of chip-to-chip and module-to-module I/O is a constant ! So far 44 external lanes envisaged.

ROI/DAQ bandwidth

- Decide **now** what's required
- Ready to add miniPOD (12 channels)
- All V7 compatible rates acceptable

comments

Configuration schemes

- Use multiple schemes: legacy ACE, one or several alternatives
- Flash write cycle (20 minutes), device density, configuration speed

Module control – decision to be taken now

- Initially VME extender
- Later whatever L1/L1Calo favour
- MGT/separate crystal to allow for any format/rate
- # channels ?
- Front panel optical/electrical and/or backplane ?
- Open for processor based Ethernet. On Mezzanine. Zynq ?

ATCA/IPMC etc.

- Need to start looking into documentation available now.
- Put h/w on mezzanine and hope that someone in the community can provide scheme/software
- Not required initially for operation on the bench.

Module count/ duplication

- No backplane links
- no far end PMA loopback

Need to stop here…