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| Report of the Specification & Preliminary Design Review |
| TDAQ Forward Feature Extractor |
| Summary |
| The specification and preliminary design review of the TDAQ fFEX was held on September 26th, 2022 with Zoom connection. This report summarizes it and gives some recommendations.  |
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# Members of the Review Committee

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| Review Committee | fFEX Team |
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# Agenda and available documentation

The agenda and documentation are available at: <https://indico.cern.ch/event/1184786/>

# Review outcomes (O: observations; R: recommendations; A: actions; CA: critical actions)The actions are requested to be implemented, whereas the team may – after careful consideration – decide to implement or not implement each of the recommendations. The team is asked to take note of the observations. The action labeled CA – Critical Action – must be addressed and closed before the review can be considered passed. All the other recommendations and actions shall be followed up and addressed by the team before the next review, and are to be discussed in presentations at that meeting.

The fFEX (forward Feature EXtractor) is part of the L0Calo trigger system in the TDAQ Phase-II upgrade, to extend the ATLAS trigger performance for electrons (|η|>2.5) and jets (|η|>3.2) being produced in the forward region. The fFEX receives cell level energies from the LAr LASP and identifies jets and electromagnetic clusters. The identified objects and some global quantities are reported to the Global Trigger. The fFEX is in the ATCA form factor. A total of 4 fFEX blades will be installed in an ATCA shelf in USA15.

A fFEX document which describes the user requirements, specifications and preliminary design, and review presentations have been made available before the combined SPR & PDR.

***fFEX specification***

**R:** Each fFEX blade is a double width ATCA module which carries 2 processing FPGAs. Power consumption of fFEX is specified to be no more than 350 W for front blade and 50 W for RTM. The team should check the power and cooling allowance for the double width ATCA module, which could be beneficial to ease the overall fFEX power and thermal management.

The numbers provided by the fFEX as the power consumption specification come directly from the allowance of the double width ATCA module.

No, we do not have information for a double width module. TC ?

**O:** The team is planning to perform simulations to study the fFEX performance with better statistics beyond studies described in the TDAQ Phase-II Upgrade TDR, to compare trigger efficiency with offline selection as a reference.

To be done in the future.

**O:** Each fFEX processing FPGA has 88 fiber optical links to receive data from LASP, and 24 links to send data to Global Trigger. All links in the real-time path use 25.78125 Gb/s crystal-referenced transmission in Interlaken (“core1990”) protocol.

* The suitability of the Interlaken protocol for low latency data transmission from LASP to fFEX needs to be demonstrated. Due to latency concerns, a different scheme of LHC-clock synchronized transmission at 25.65 Gb/s with 8B/10B encoded data is considered.
* The FELIX team has released an updated Interlaken protocol in the firmware specification document, which includes some more information on the different latency contributions measured in tests. The fFEX team may use that as reference for latency study. Please see section 8.4.19.4 of: (<https://atlas-project-felix.web.cern.ch/atlas-project-felix/user/docs/FELIX_Phase2_firmware_specs.pdf>).
* The LASP team is concerned that a protocol based on 8B/10B encoding at 25.65 Gb/s will require more development work than currently assumed, considering the link stability, additional error correction and control etc.

The latency concerns regarding the Interlaken protocol have disappeared, since we now realize the additional latency was already considered in the budget. We will keep the double scheme at least for the prototype, but in principle we would remove the LHC-clock synchronous option moving forward and keep the asynchronous option, which provides better link stability. For us, internally: we should not forget resource use until test implementation done…

**R:** The team should discuss with the LASP team to finalize the choice of link, either at 25.78125 Gb/s asynchronous to LHC clock, or at 25.65 Gb/s synchronous to LHC clock. Necessary tests should be carried out to facilitate the decision making as soon as possible. Until this is agreed upon, the design needs to have the clock scheme to support both options.

Both in terms of latency and in terms of resources the asynchronous option seems viable and it would therefore be out preferred choice, as the one we thought originally because of its better link stability. The prototype will still include both options, however.

**O:** Each processing FPGA uses 2 central SLRs in Xilinx FPGA VU13P to receive LASP data for the core region of 1 φ quadrant (or 2 φ octants), and 2 outer SLRs to receive LASP data for 2 neighboring octants in φ. A 100% duplication of all input data will be provided by LASP.

Correct.

**R:** The fFEX to FELIX interface has 25.78125 Gb/s TX link for readout and 2.56 Gb/s (in presentation) or 4.8 Gb/s (in document) RX link for timing channel. The team should discuss with the FELIX team to finalize the link interface, and confirm if 2.56 Gb/s lpGBT RX link is an option, or 4.8 Gb/s GBT RX link and 9.6 Gb/s 8B/10B RX link should be used.

At the moment the FELIX readout link speed is not set, but this is not something that would change our design.

**CA:** The specification of the fFEX interfaces is quite advanced. The team shall continue to work with LAr LASP, Global Trigger and FELIX systems to finalize external interface documents, which should have the number of optical links, link speed, link protocol, data format and latency clearly spelled out, with the understanding these are live documents and will evolve along the development process.

The external interface documents are at the moment just starting and mostly empty.

**O:** The fFEX firmware has 3 main components: infrastructure, readout and algorithms.

* The infrastructure firmware can reuse some design in the Phase-I jFEX/L1Topo infrastructure firmware, taking into account the migration from VU9P to VU13P.
* Preliminary studies of different algorithms have been carried out and used to make the first estimate on FPGA resource utilization.

 Correct.

**R:** The firmware specification should be further updated to include a release plan. In addition, the specification document should cover the control FPGA as well, which is currently planned to be put on the RTM, including aspects of firmware, software and operating system.

This is work that is still to be done.

**R:** The team plans to use GbE with implementation of IPbus for interface to DAQ run-control and DCS through a private network similar to Phase-I upgrade. The team should follow up with the CERN SoC interest group and explore if a SoC based interface for the fFEX unit is a better option, with DAQ run-control applications running directly on the ARM processor. Some of the SoC interest group solutions will likely be supported by ATLAS system administrators and therefore one can profit from long-term support.

This possibility could be explored, but the Phase-I approach is our current baseline.

**A:** The team shall address the comments posted by reviewers on the CDS page of fFEX document (<https://cds.cern.ch/record/2827376/comments?ln=en>), and additional comments below:

* Line 230 – input energy encoding: the energy encoding scheme will depend on the range of energies that are delivered by the LASP system; the classic optimal filter may contain negative energies; newly developed neural network approaches aim at producing only positive energies by stronger suppression/correction of out-of-time pile-up.
* Line 235 – DCS data path: the specification should make a more clear statement about the transmission of DCS data that is not sent by IPMC/shelf manager. It should be clarified if DCS data and board/run control data can be handled by the same GbE link, and if there will be an OPC-UA server which is required in Phase-II upgrade. This also requires a clarification of the network integration of the fFEX modules in the ATCN at Point 1. The team should evaluate if a second GbE could be useful considering redundancy and separability of DCS and run-control traffic.
* Figure 4.3 – clock distribution: it should be clarified if the clock lines from/to the RTM fulfill the clock quality requirements, e.g. jitter, etc.
* Line 1025 – LAr “energy saturation”: it should be added that this “saturation” is a saturation of the encoding range, not a saturation of the LAr analog or digital readout.

 The responses to these comments are written in a separate document that was also provided.

***fFEX preliminary design***

**A:** The Xilinx FPGA VU13P is used in the current fFEX front blade prototype design as the baseline, while Versal Premium FPGA is also being considered. The team shall make the FPGA selection, ideally this should already be done by PDR.

We stick to VU13P for the prototype.

**O:** The FPGA resource estimate is still preliminary, with extrapolation from algorithm firmware studies, and has ~60% of usage in LUT and DSP for algorithm firmware. The estimate is missing infrastructure and readout firmware, necessary interfaces across 4 SLRs in the floorplan, and clock utilization. This implies there is a risk the firmware may run into the FPGA resource limit.

We are exploring a few possibilities here to reduce the resource use. One of them would be to use a 6 times faster clock (240 MHz)- that’s already been accounted for !!!, which would reduce the resource use by a factor 6 (real value to be checked, probably smaller). Another possibility we are considering would be to double the amount of FPGAs that are used to process the same quadrant, doubling the amount of boards as well.

**R:** The team should justify that usage of the algorithm firmware can be sufficiently reduced by operating at a multiple of the base clock.

This is still to be checked.

**R:** The team should make more progress in the firmware development, aiming to make a realistic estimate on both FPGA resource usage and power consumption with Xilinx tools, which is also important to devise a proper thermal management scheme. In addition, the estimate will provide important inputs to confirm the baseline choice of the FPGA, would VU13P be OK or Versal Premium FPGA needs to be used?

We will use the Xilinx tool for power estimation once we know how much resources the fFEX will require.

**O:** The fFEX preliminary design includes a front blade and an RTM. The power dissipation of the front blade is estimated to be about 300 W with main contribution from 2 processing FPGAs, based on experience from the Phase-I upgrade.

Correct.

**O:** The fFEX preliminary design has a modular construction with high-speed circuitry on the main board, and mezzanines for power supply, IPMC, JTAG and I2C interfaces.

* Both JTAG mezzanine and I2C mezzanine designs are under way.
* The team confirmed the form factor of the front blade will be standard ATCA, not the modified L1Calo form factor with an extension around the Zone 3 area for other FEX modules developed in Phase-I upgrade.
* The fFEX preliminary design supports the FELIX interface on processing FPGAs on the main blade and/or control FPGA on the RTM.
* Preliminary design of RTM has not been presented, the interface between the front blade and RTM is to be worked out, given the originally planned MTP-CPI connector becomes obsolete.

 Correct.

**R:** The front blade design is ready for the P&R in PCB layout, with the stack-up used in the Phase-I upgrade. The team should discuss with the PCB manufacturer to get an updated stack-up with halogen free material.

This will be done.

**R:** The fFEX team plans to use an UltraZed module mounted on RTM to handle the module control and FELIX interface. The team should check if UltraZed can handle 25.78125 Gb/s links, the proposed one with ZU7EV doesn't have GTY transceivers to support 25 Gb/s links.

This is one important point to consider, but we do not have a decision about it yet. Current baseline: use per processor FELIX and low speed link controller

**CA:** The RTM in the fFEX design is not well specified and the motivation is not really justified, since this makes the overall system more complex, in terms of power management, mating connectors, control interface, readout and TTC interface, signal integrity of long traces, necessity of MMC for intelligent RTM etc. Given the estimate of power consumption is < 350 W (300 W for front blade and 50 W for RTM) plus double width configuration, the team shall revisit the design choice and optimize the prototype design accordingly.

* The team should consider simply moving the SoC mezzanine from the RTM to the front blade, possibly taking advantage of the additional area in Zone 3.
* A follow-up review should be planned once the team makes progress in finalizing the preliminary design of the fFEX, including the front blade design, JTAG and I2C mezzanines, and RTM if the team decides to keep it. This review could be held before the layout design is completed allowing comments to be addressed before the prototype fabrication.

No decision yet, but the possibility of having the controller FPGA on the mainboard is being considered.

**R:** The team should consider whether staggering 2 processing FPGAs on the main blade, so that they are not aligned vertically, could help improve the airflow to the upper FPGA. Otherwise, mounting holes should be placed on the board, to allow the option of fitting a baffle to redirect the airflow.

Board design is being revised, one of these options will be included.

**O:** It was reported that interoperability tests of optical links between Samtec FireFly on fFEX and Finisar BOA on Global Trigger need to be performed. The optical modules used on the Global Trigger is still to be determined, on the other hand, the early development of FELIX and GCM demonstrators have already verified the interoperability for optical modules from different vendors.

Correct.

**R:** The team would like to finish the main blade design then send it out for fabrication due to personpower constraints. Rushing to send out the fFEX main blade may not be the best strategy in the long term, particularly if the design needs to be significantly revised. Nevertheless, the team should spend time to organize the fFEX development with different design cycles and long term support in mind.

This is, of course, reasonable.

**R:** The team should consider putting all monitoring parameters which go to IPMC also on SoC if reasonably possible (e.g. sensor duplication, separate I2C interfaces if data is from FPGA).

There will be sensor duplication, not I2C switch.

**R:** The validity of DCS data should be verified at the firmware level on the main blade processing FPGA or SRTM SoC, e.g. by using timestamps or toggling bits.

Ok, we take note of that.

**R:** For network integration, DCS links should be routed to ATCN directly, i.e. if routing via ATCA backplane and ATCA switch, compliance with ATCN requirements should be ensured.

We are not going via ATCA backplane. Direct cable connection from the blade to whatever switch will be provided to us by ATLAS IT.

# Conclusions and Recommendations

The review panel appreciates the work that went into the preparation of the document and review presentations, which were comprehensive with good coverage on both hardware and firmware aspects prepared by a knowledgeable team with Phase-I experience. The panel considers the review as **conditionally passed with follow-up actions**. The team shall finalize the interface documents with the LAr LASP, TDAQ Global Trigger and FELIX systems. The team shall further develop the preliminary design, in both hardware and firmware, before green light is given to launch the prototype fabrication. Other actions and recommendations should be addressed by the PDR follow-up review.