Level-1 Trigger updates for Phase 1

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For ATLAS TDAQ

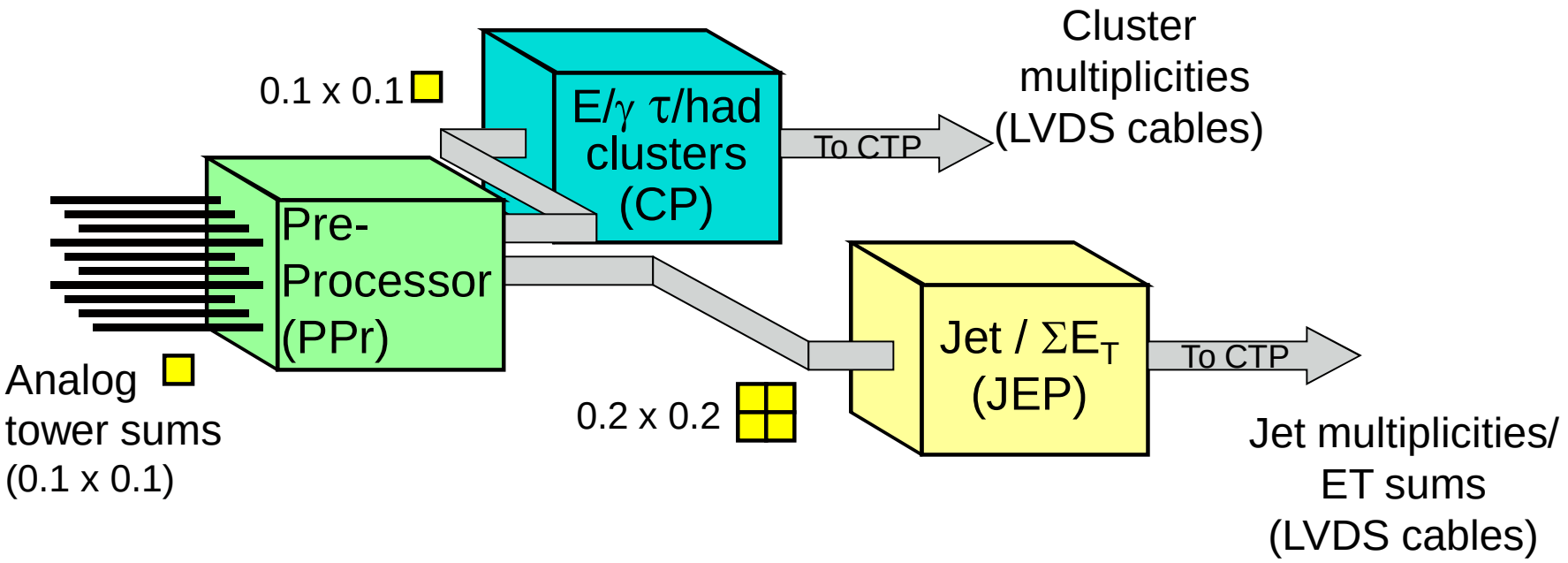
Phase-1 upgrade strategy

- Keep much of current infrastructure
  - Trigger front ends
  - Identification of Jet/em/hadron/muon objects (ROIs)
  - Continue using current multiplicity-based algorithms, $\sum E_T$ triggers.
- Add topological trigger algorithms
  - Use coordinates of ROIs seen in Level-1
  - Combine ROI maps from L1Calo cluster, Jet (and muon) subsystems in a global topological algorithm processor

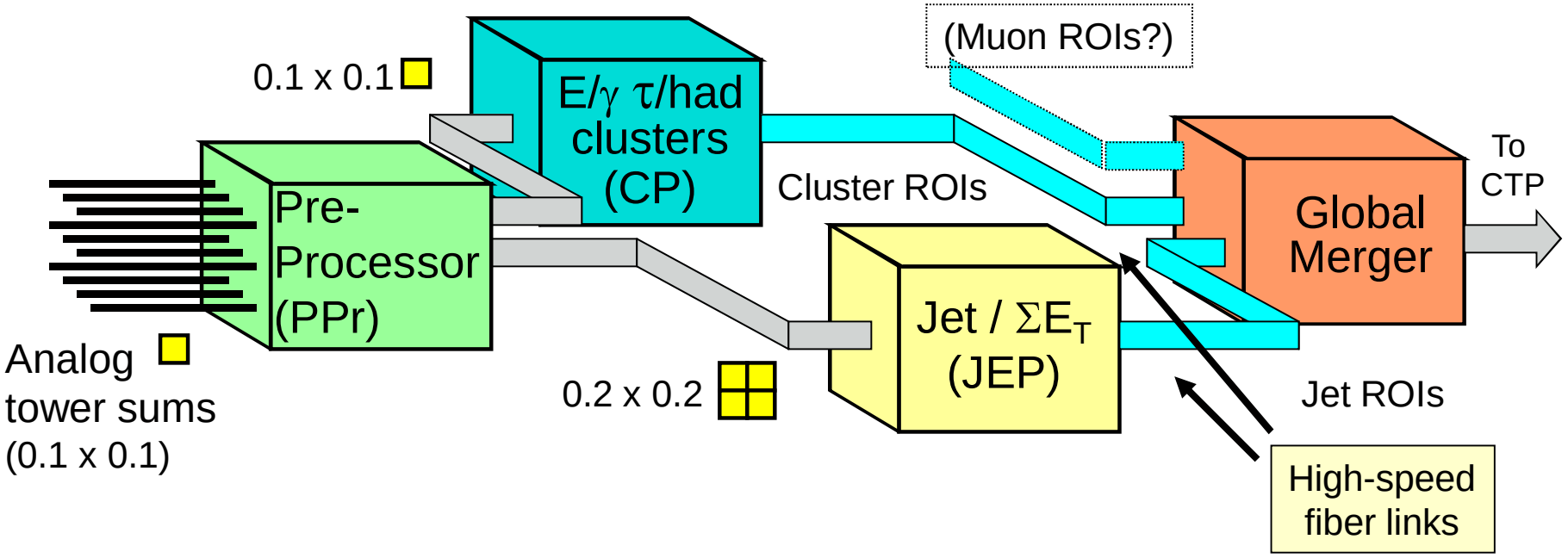
L1Calo Upgrade

- Upgrade processor module firmware to report ROI bits and coordinates on real-time data path
- Collect and transmit ROI maps to a global topological processor crate
  - Can we include muon ROIs?
- Report multiplicity-based and topological trigger results to CTP

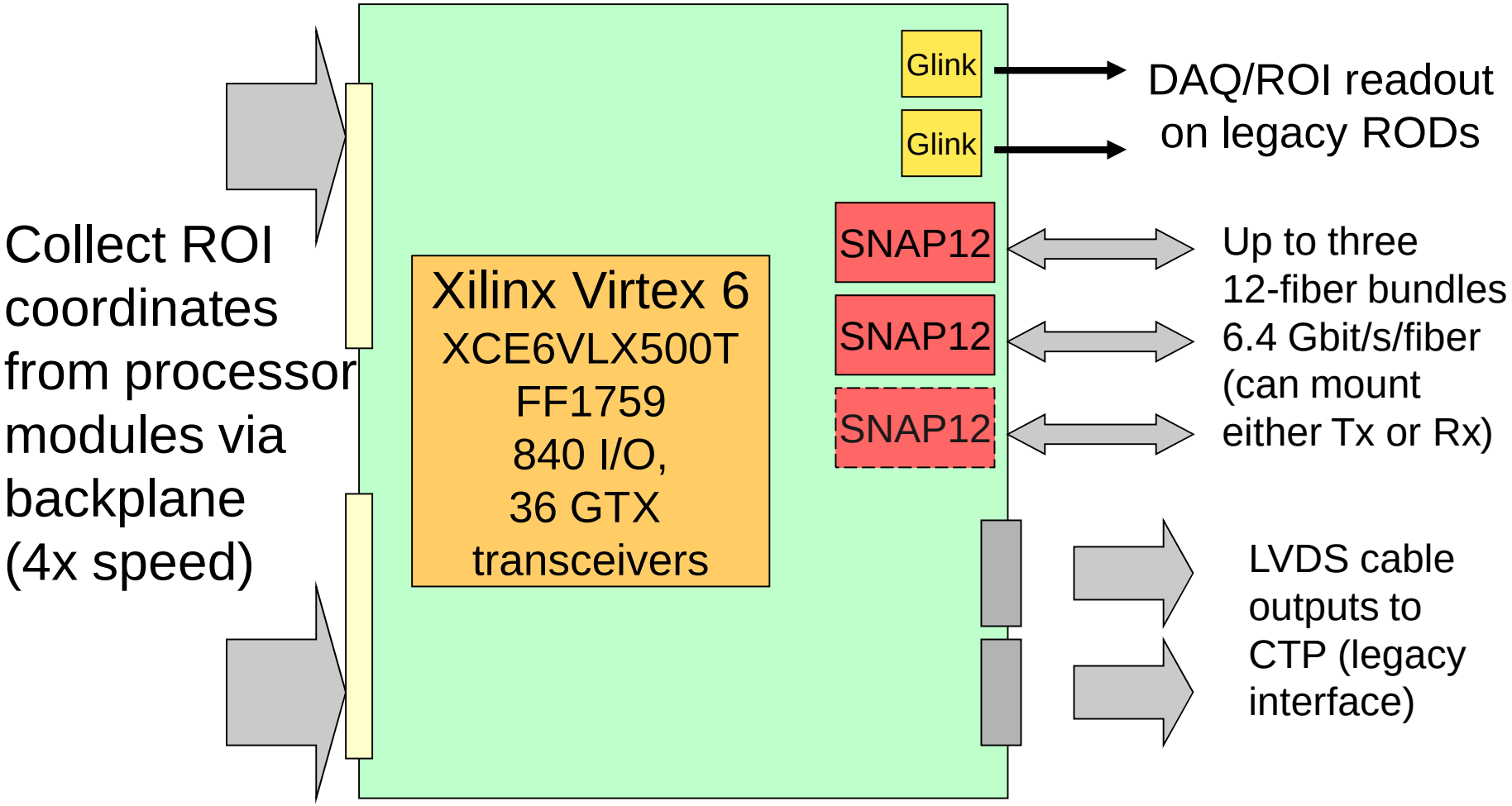
Current L1Calo system



Phase-1 upgrade

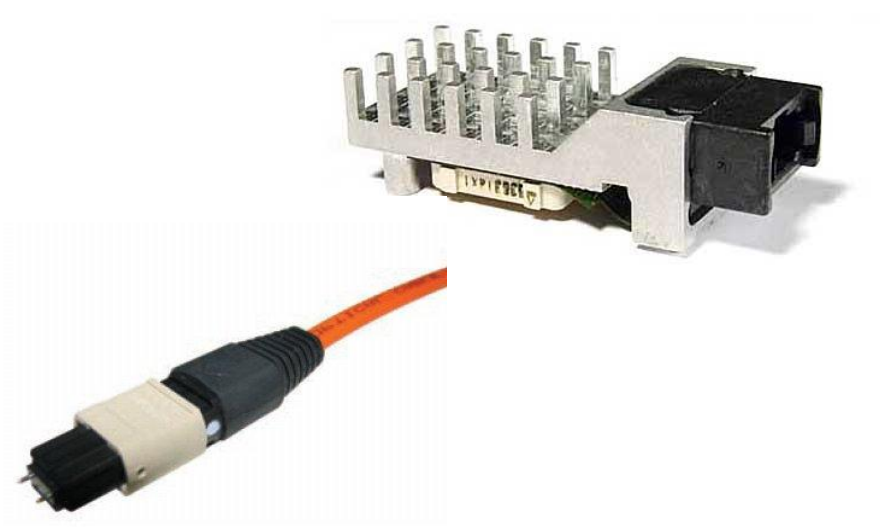


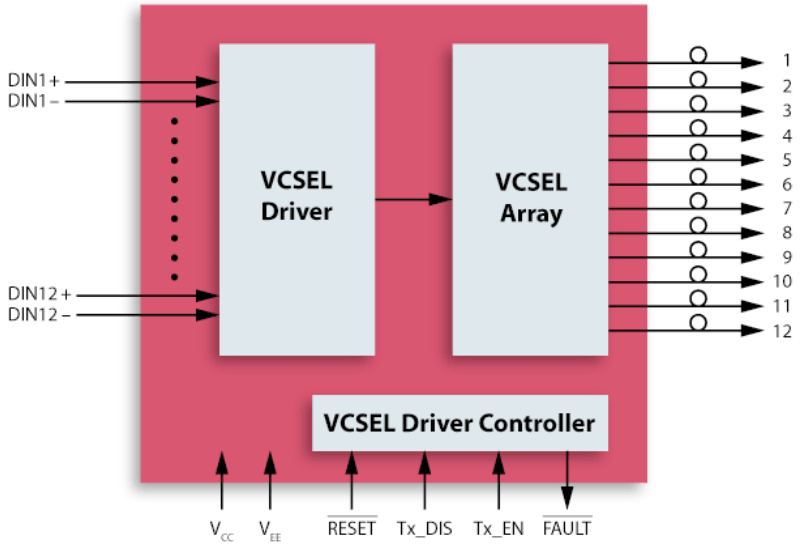
CMM++ design concept



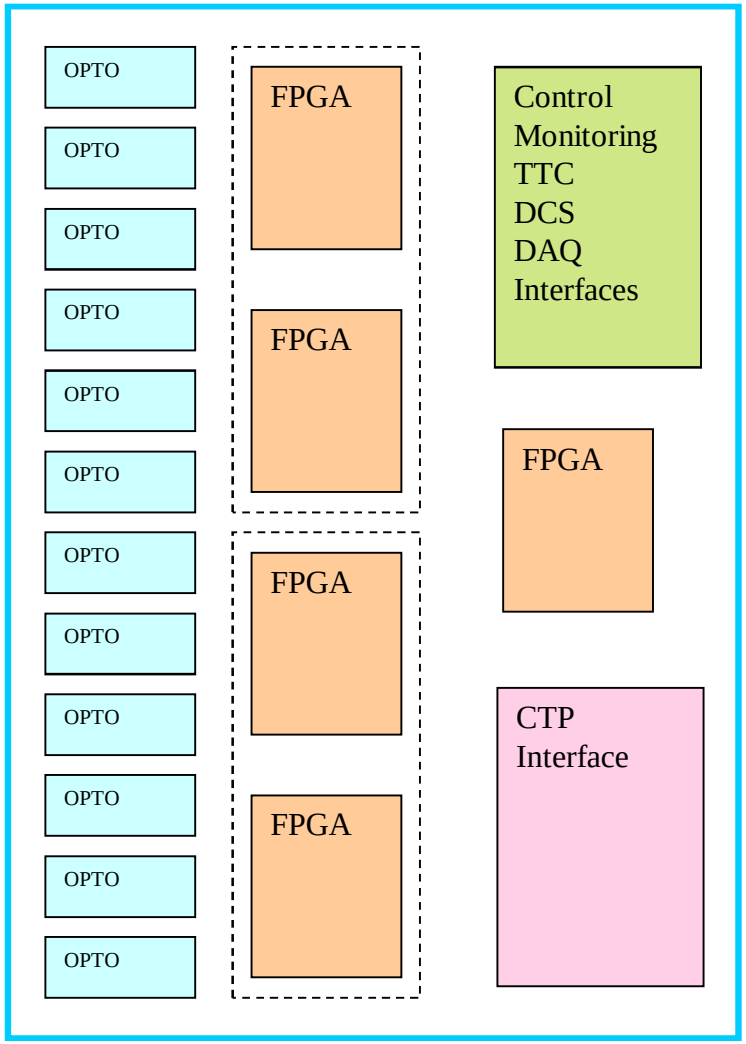
Ribbon Fiber

- Simple transmitter/receiver pair
- 12 parallel channels at up to 6.4 Gb/s each.
- Low added latency





Topological processor module



- Optical ribbon links bring all L1 ROI data to each TP module
- Four FPGAs receive and pre-process one quadrant of data each. Global processing of selected data on additional FPGA(s)
- Scalability: use upstream replication of input signals → multiple modules can run in parallel, each with access to full data.

Topol. algorithm candidates

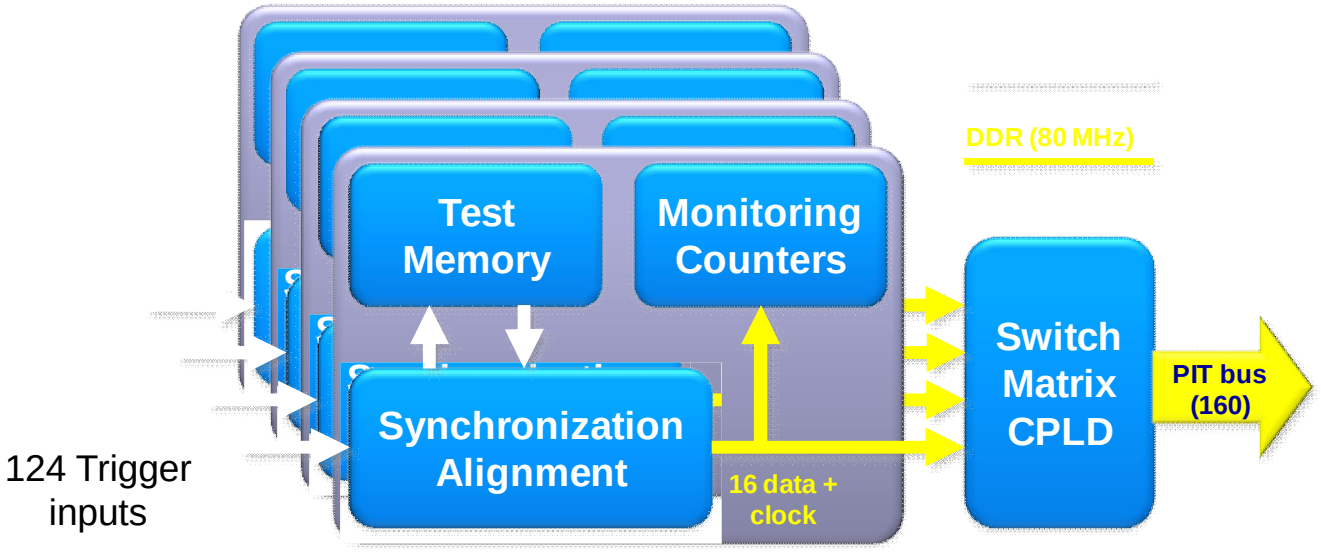
- Overlapping features
  - Identify electrons/hadrons also seen as jets..."clean up" double counting
- Rapidity gaps
  - delta-phi, delta eta
- Back-to-back features
- Etc....

CTP upgrade

- Additional algorithms will require more inputs to CTP
- CTP can modify firmware to run at higher speed, multiplex inputs to accomodate more bits
- Possibility to extract ROI information from MUCTPI to include muons in topological triggers
- Described in TDAQ week talk by Stefan Haas

CTP upgrade Status (S. Haas)

- Modified firmware tested successfully on one of the CTP reference systems
  - Inject arbitrary data patterns from the CTPIN test memories
  - Check monitoring buffers and counters on CTPIN, CTPMON and CTPCORE
- Clock phase scan shows good timing margins
  - Valid data window 65-70% (8-9 ns) of the bit period (12.5 ns)



CTP upgrade Status (S. Haas)

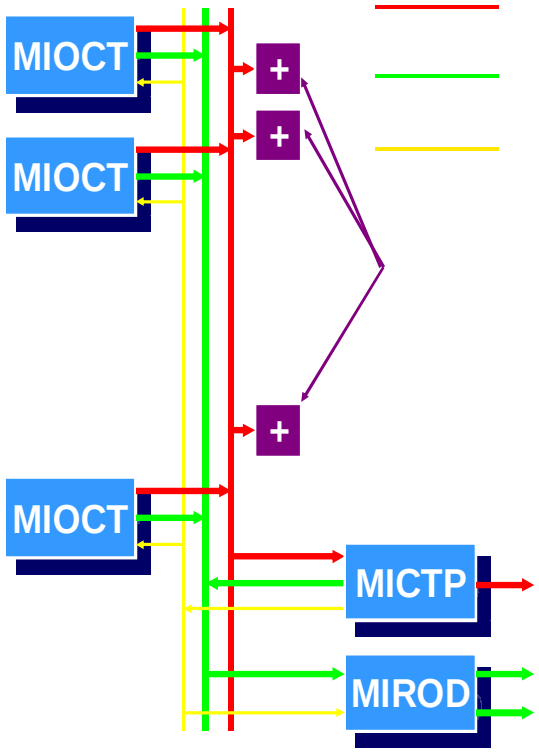
- Basic CTP functionality maintained with a few limitations:
  - Bunch-by bunch monitoring only for 160 PIT signals
    - Limited FPGA memory resources on the CTPMON module
  - Reduced flexibility in mapping trigger signals to LUT inputs
    - Trigger signals always allocated in pairs
  - Latency increased from 4 to 7 BC (6 BC probably feasible)
- Most of the software development still to be done
  - This is the limit of what can be done without changing the current CTP hardware
    - Any other significant modifications will require (partial) redesign

Muon upgrade

- No plans to upgrade muon detector hardware for additional Phase-1 trigger functionality
- Discussion to add third TileCal layer to muon trigger, but don't believe this will improve p_T resolution (limiting factor in trigger).
- Possibility to modify MUCTPI to include some ROI topological information to L1 data path

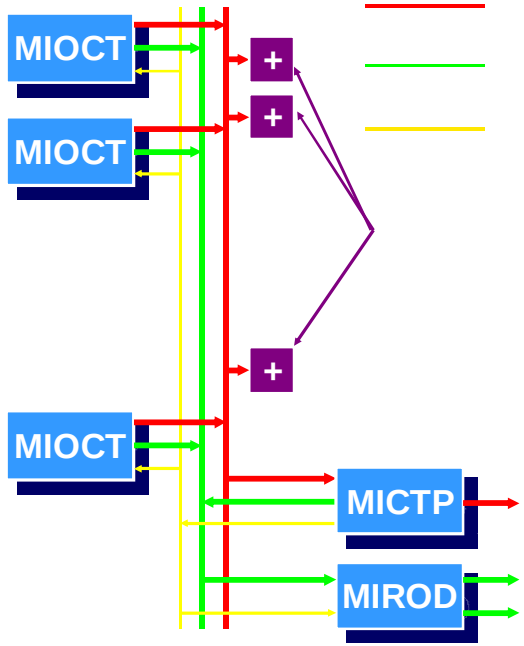
MUCTPI (S. Haas)

- MUCPTI receives muon candidates from 208 trigger sectors
  - Up to 2 muon candidates/sector/BC
  - Muon candidate data consists of p_T and location information (RoI)
  - MUCTPI calculates and sends multiplicity per p_T to the CTP
  - Sends detailed muon candidate data to LVL2 and DAQ at L1A rate
- Topological trigger processing could potentially profit from detailed muon candidate information

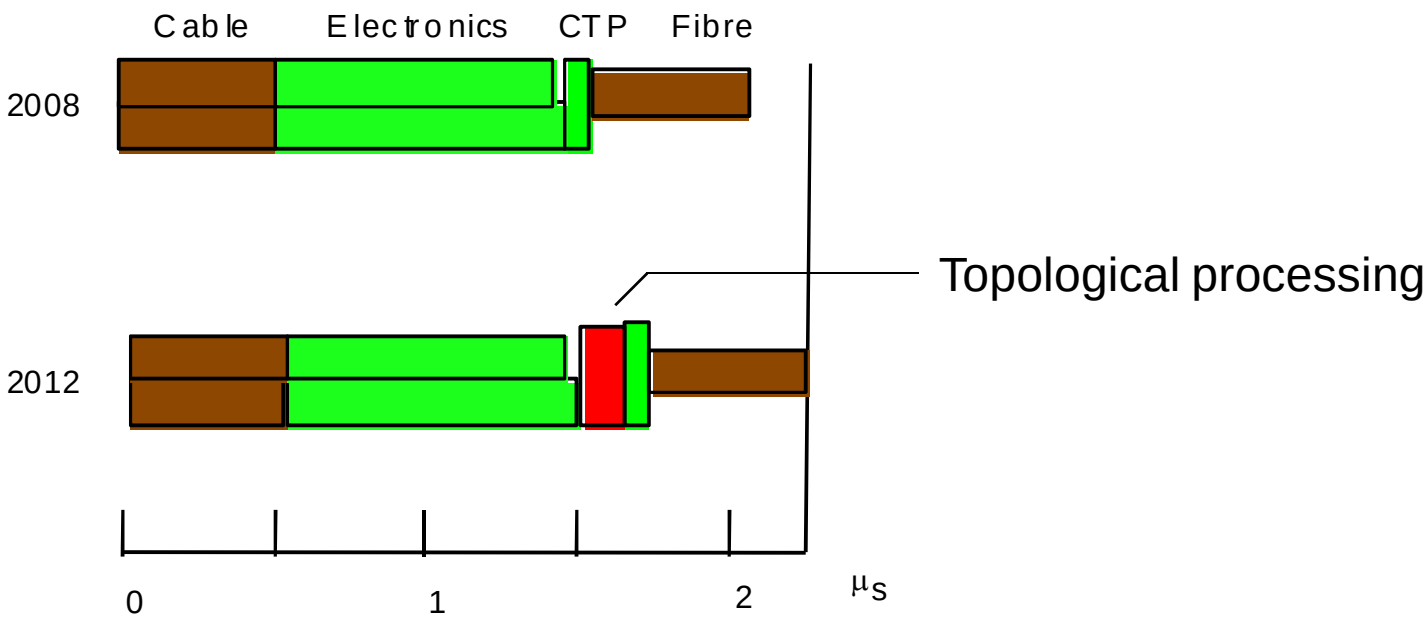


MUCTPI (S. Haas)

- MIOCT modules have 2 local trigger outputs
  - Could only be used for very coarse topological information (~4 bit per octant)
  - Extracting full p_T and RoI information for a subset of muon candidates at 40 MHz requires redesign of the system
  - Feasible for phase-I if required
- May have to modify MIOCTs for additional RPC chambers in the ATLAS feet region
  - Requires 14 inputs per octant



Latency implications



- What is our latency budget?

Current latency budget

- L1Calo latency in USA15 and CERN test rig measured, with good agreement between them.
- We are only slightly over original 2 μs budget
  - perhaps 0.45 μs available for phase-1 upgrade without impacting LAr dead time
  - Corresponds to about 18 BCs in L1Calo

Sources of added latency for L1Calo Phase-1 upgrade

- ROI data transfer from processor modules to CMM++ over backplane
  - ca. 1 BCs
- Fiber optic transfer of ROI data to algorithm processor
  - ca. 5 BCs
- Latency of the topological algorithms
  - ???
- But it's not all bad news....

Potential latency savings in L1Calo Phase-1 upgrade

- Skip multiplicity summation in processor modules
  - ca. 0.5 BCs
- Data merging now takes 8-9 BCs in current CMMs
  - Can skip crate-to-crate merging of data in system
    - ca 1 BC
  - Virtex-E ⇒ Virtex 6 FPGAs: much faster!
  - Topological algorithms can run in parallel with multiplicity based, "day-1" algorithms
    - Can start before end of current latency envelope
- Savings may balance much or all of the additional latency costs

Current activities

- L1Calo:
  - simulation and prototype VHDL designs for Phase-1 topological algorithms
  - Various hardware/firmware prototyping and feasibility studies
- CTP
  - Studies of firmware upgrades/modifications to accomodate topological algorithms
  - Discussions with L1Calo on providing Muon ROIs to topological processor