Hardware status GOLD

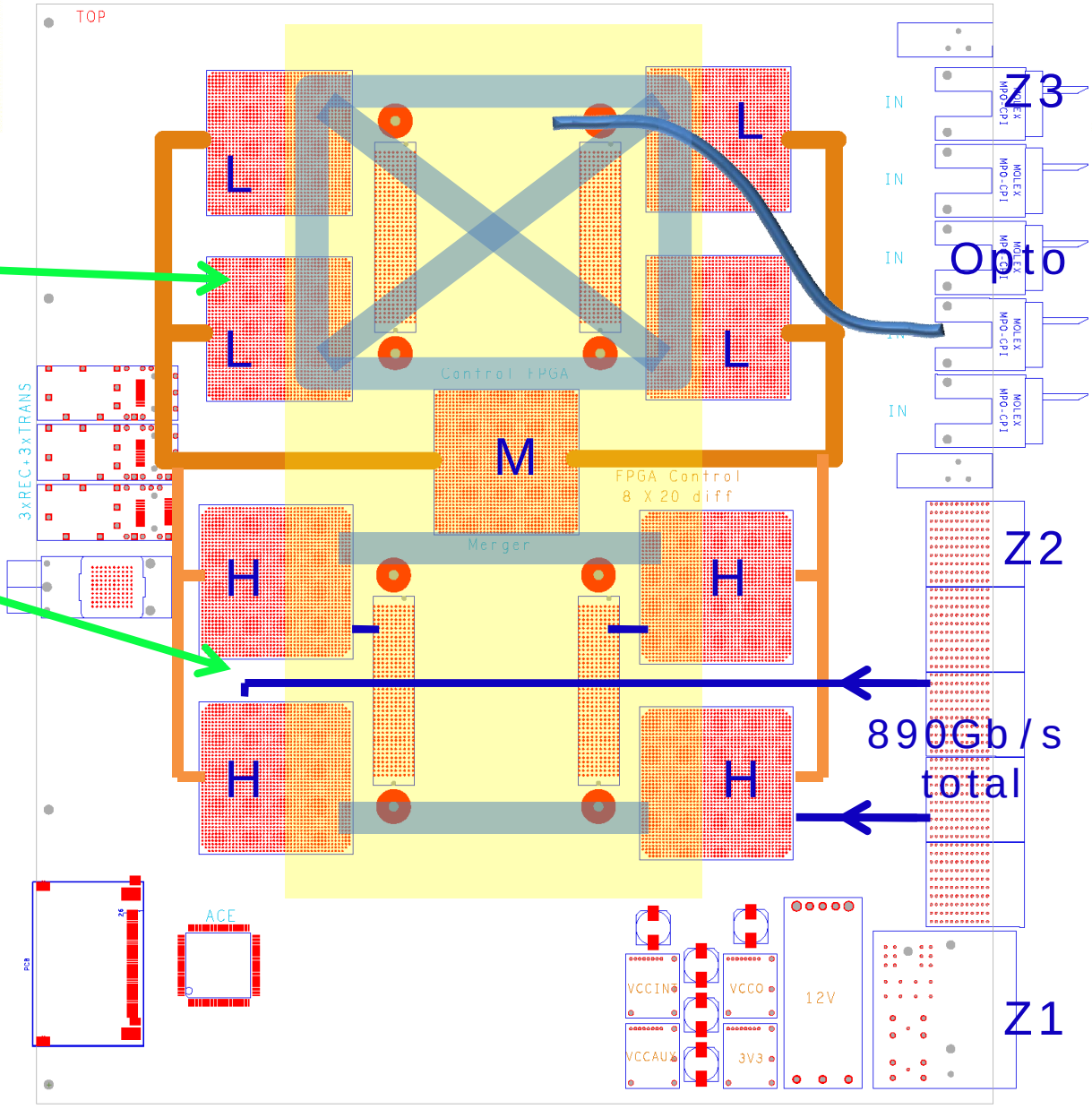
Update 03 Mar. 2010

GOLD floor plan (approximate)

5 * XC6VLX (L,M)

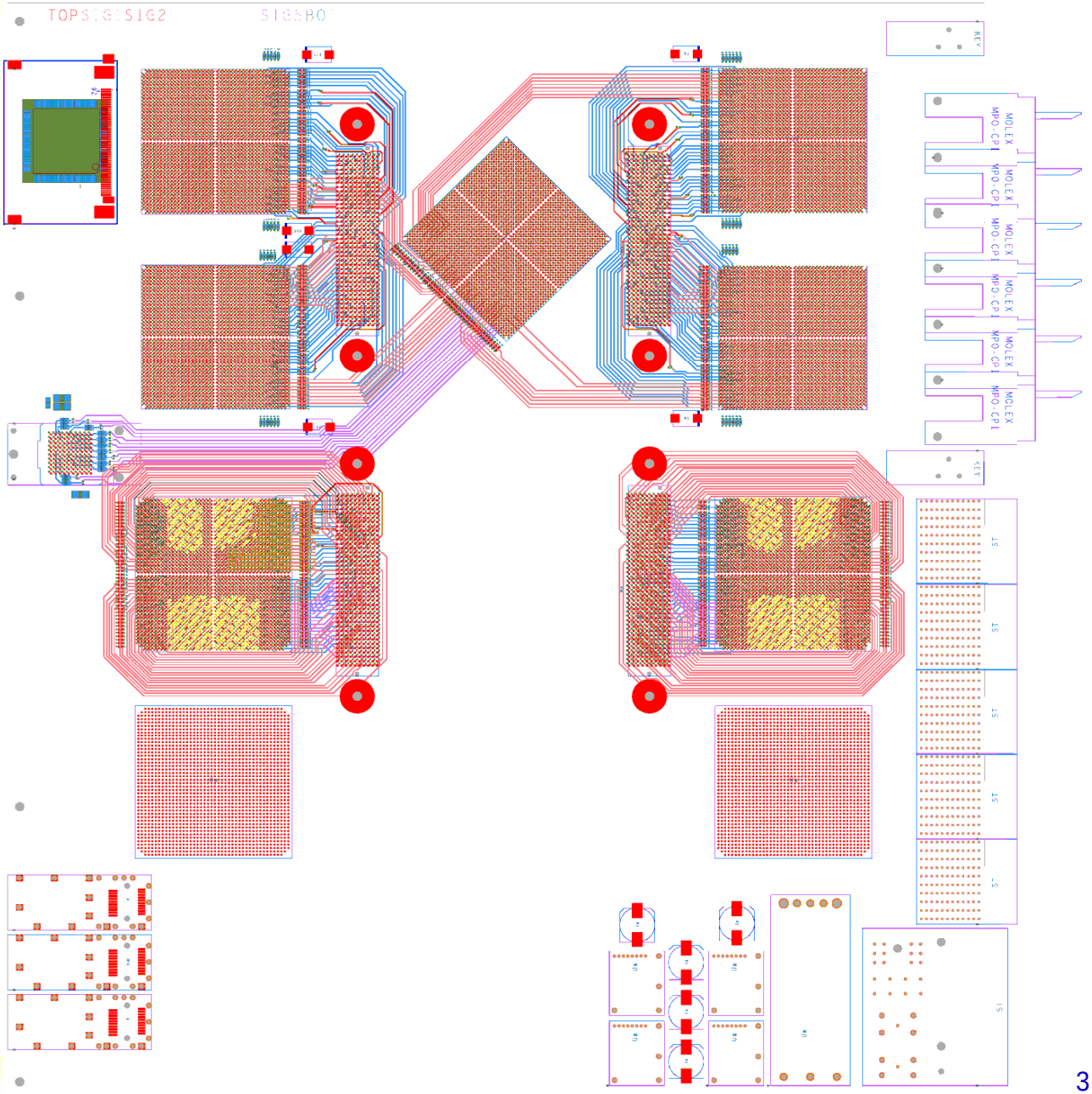
4* XC6VHX (H)

144 multigigabit links in zone 2 (equiv. 22300 bit / BC)



GOLD – current status

- Schematics partially done
- Routing as shown:
  - xGb/s links hand routed →
- ‘Low’ speed links (1Gb/s) to be auto routed



GOLD status

- Schematics and layout under way
- Components ordered. Lead time:
  - AVAGO (2*T, 2*R) : arrived
  - SNAP12 : mid April
  - Xilinx XCVLXT: 8-10 weeks
- Production of Xilinx HXT devices delayed

Firmware activities:

Currently working on extension of VME bus from 9U processor crates, via BLT module, optically into GOLD