* L1Topo Production v1.0
* **L1Topo design modifications**[**http://www.staff.uni-mainz.de/baussh/TOPO/L1Topo\_REF1/L1Topo\_REV1\_Sheets.pdf**](http://www.staff.uni-mainz.de/baussh/TOPO/L1Topo_REF1/L1Topo_REV1_Sheets.pdf)
* **MGT termination calibration resistors: Mount all instances -> SHEET 28,29**
* **Differential routing of spare lines between processor FPGAs and extension mezzanine -> SHEET 7, 13**
* **(check for cc’able pairs). Use same connectivity as jFEX on mezzanine end. Route cc’able pins first. Symmetric between FPGAs. Check if differential routing works for jFEX as well.**
* **The plan is to run same configuration of control FPGA on Topo and jFEX. -> SHEET 24**
* **Add one (as yet unused pin on mezzanine connector) and ground it on Topo. Open on jFEX.**
* **Add one (as yet unused pin on mezzanine connector) and ground it on new design. Open on old design.**
* **IPMC Changes** <http://www.staff.unimainz.de/baussh/TOPO/L1Topo_REF1/CERN-IPMC%20-%20hardware%20guide.pdf>
* **Address lines HA 0..7 should be made identical between L1Topo and jFEX (update L1Topo to jFEX) -> SHEET 49**
* **Connect (if possible 8 , but at least correct original 4) IPMC ‘user’ lines to the mezzanine. -> SHEET 49**
* **The problem with the USER\_IO lines is that we got wrong the IPMC pin mapping for them. (you can find the correct one on this link:** <https://espace.cern.ch/ph-dep-ESE-BE-ATCAEvaluationProject/PP_IPMC/Public%20documents/CERN-IPMC%20-%20Pinout%20and%20mapping.pdf>**).**
* **We used pins 63, 64, 66 and 67 but they are IPM IO, but we want to use pins 75, 76, 197 and 198. Update IPMC symbol to correct pin mapping.**
* **Remove RES logic -> SHEET 49**
* **Remove GB\_C\_P/N, GB\_D\_P/N -> SHEET 49**
* **Remove UART CTS, RTS -> SHEET 49**
* **Change LED colors -> SHEET 49**
* **Add 8 more USER I/O to mezzanine -> SHEET 49**
* **Change JTAG header for MICROSEMI interface -> SHEET 50, CERN-IPMC Hardware guide SHEET5**
* **Connect EXT\_RES to JTAG header -> SHEET 50**
* **Change BASE ETHERNET INTERFACE -> SHEET 51, CERN-IPMC Hardware guide SHEET6**
* **Remove BASE ETHERNET connection to mezzanine -> SHEET 51**
* **Remove I2C (IPMC\_SENS\_SDA/SCL) pullups U30 (pullups on U31)->Sheet 50**
* **IPMC temp sensors move to bottom side**
* **Change Different REFCLK INPUTs QUAD232 U1 and U2 -> SHEET 21, 38**
* **Change Clock Fanout AC coupling capacistors from 100nF -> SHEET 46**
* **Connect Mainboard JTAG chain to mezzanine -> SHEET 57**
* **Change Config CCLK, Config D0 – D3, JTAG to 50R single ended impedance -> SHEET 53,54**
* **Config CCLK serial resistor 39 R -> SHEET 53,54**
* **Check JTAG GÖPEL Interface for M-lines without config resistors**
* **Set config M0-2 pullup/-Down to NA -> SHEET 53,54**
* **Drillsize Zone 1 +2 connector check**
* **ZD24 HM-Zd Plus Drill 0.46mm**
* **J5 Drill 1.6mm + 1.0 mm**
* **Update Mezzanine connector pins spreadsheet**
* **PUDC 1k to GND on mainboard**
* **JTAG TCK buffered (SN74AVC4T774) for each device in chain ( U1,U2,Mezz)**
* **JTAG Leveltranslator (2x SN74AVC4T774) OE\* pullup to 3V3 and pulldown with transistor to gnd, base over resistor to 1V8\_FPGA. Output enables with 1V8\_FPGA rail.**