REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

UNIVERSITY OF MAINZ

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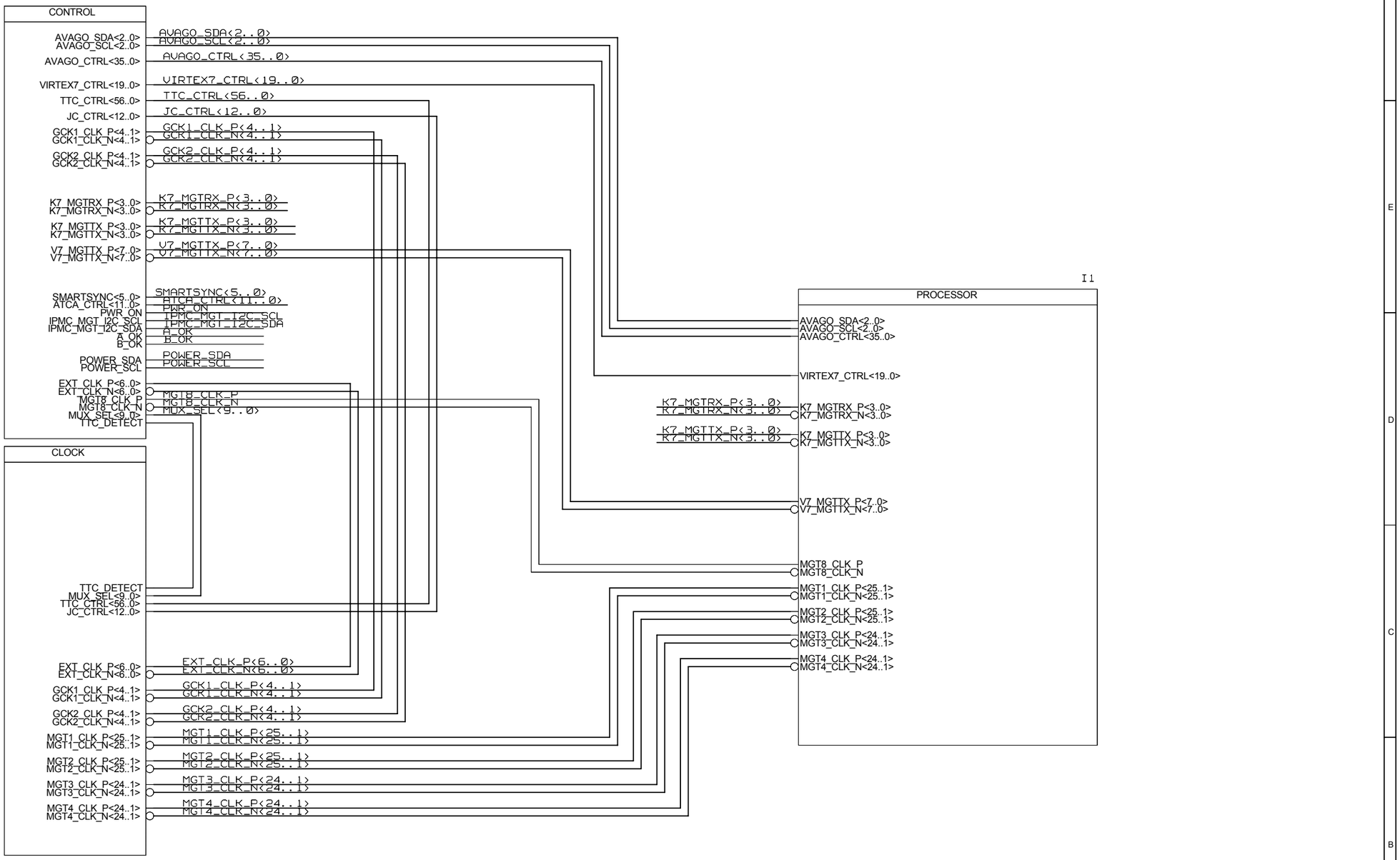
C		

SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



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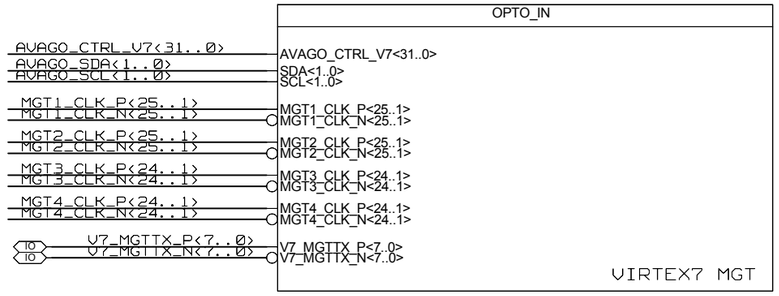
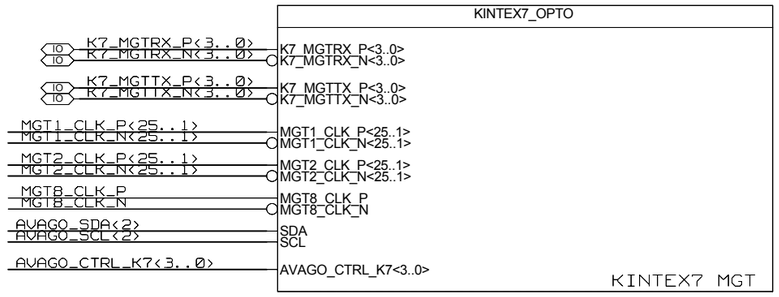
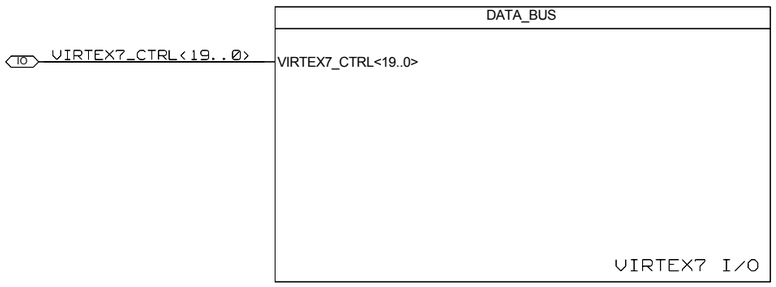
ZONE	LTR	DESCRIPTION	DATE	APPR.







MGT1_CLK_P<25..1>
MGT1_CLK_N<25..1>
MGT2_CLK_P<25..1>
MGT2_CLK_N<25..1>
MGT3_CLK_P<24..1>
MGT3_CLK_N<24..1>
MGT4_CLK_P<24..1>
MGT4_CLK_N<24..1>
MGT8_CLK_P
MGT8_CLK_N

AVAGO_SDA<2..0> → AVAGO_SDA<1..0>, AVAGO_SDA<2>

AVAGO_SCL<2..0> → AVAGO_SCL<1..0>, AVAGO_SCL<2>

AVAGO_CTRL<35..0> → AVAGO_CTRL_V7<31..0>, AVAGO_CTRL_K7<3..0>

UNIVERSITY OF MAINZ		DRAWING TITLE: OPTO INPUT AND DATA	
BLOCK: PROCESSOR		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

U1_AV1

AVAGO_MINIPOD_REC

SUBDESIGN_SUFFIX=AV1

U1_AV2

AVAGO_MINIPOD_REC

SUBDESIGN_SUFFIX=AV2

U1_AV15

AVAGO_MINIPOD_TRAN

SUBDESIGN_SUFFIX=AV15

NC VX485

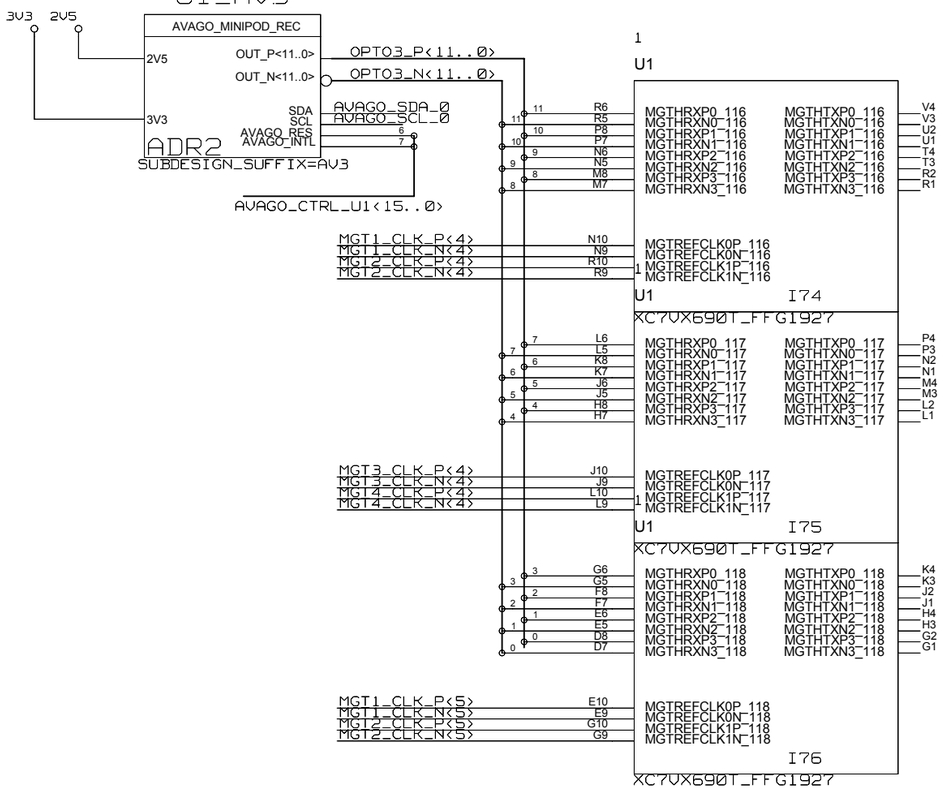
NC VX485

XC7VX690T_FFG1927

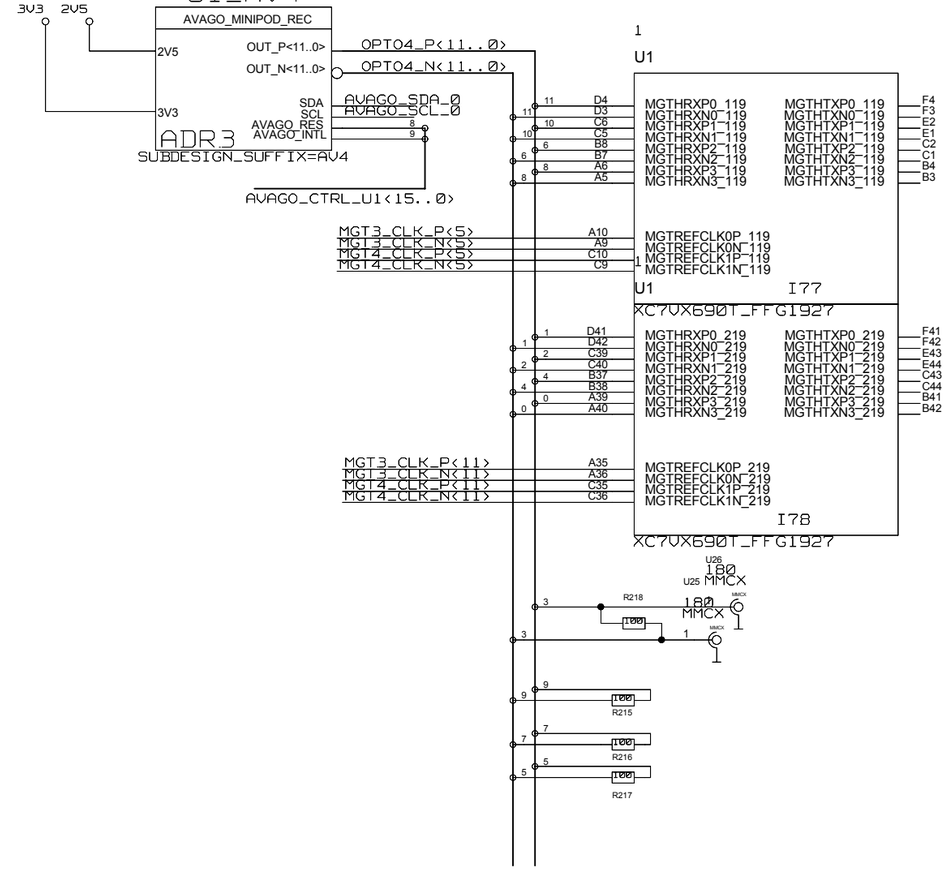
UNIVERSITY OF MAINZ	DRAWING TITLE: OPTO INPUT / OPTO OUTPUT
BLOCK: PROCESSOR OPTO_IN	SIZE C; REV.; DRAWING NO.; SCALE; SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

U1_AV3



U1_AV4



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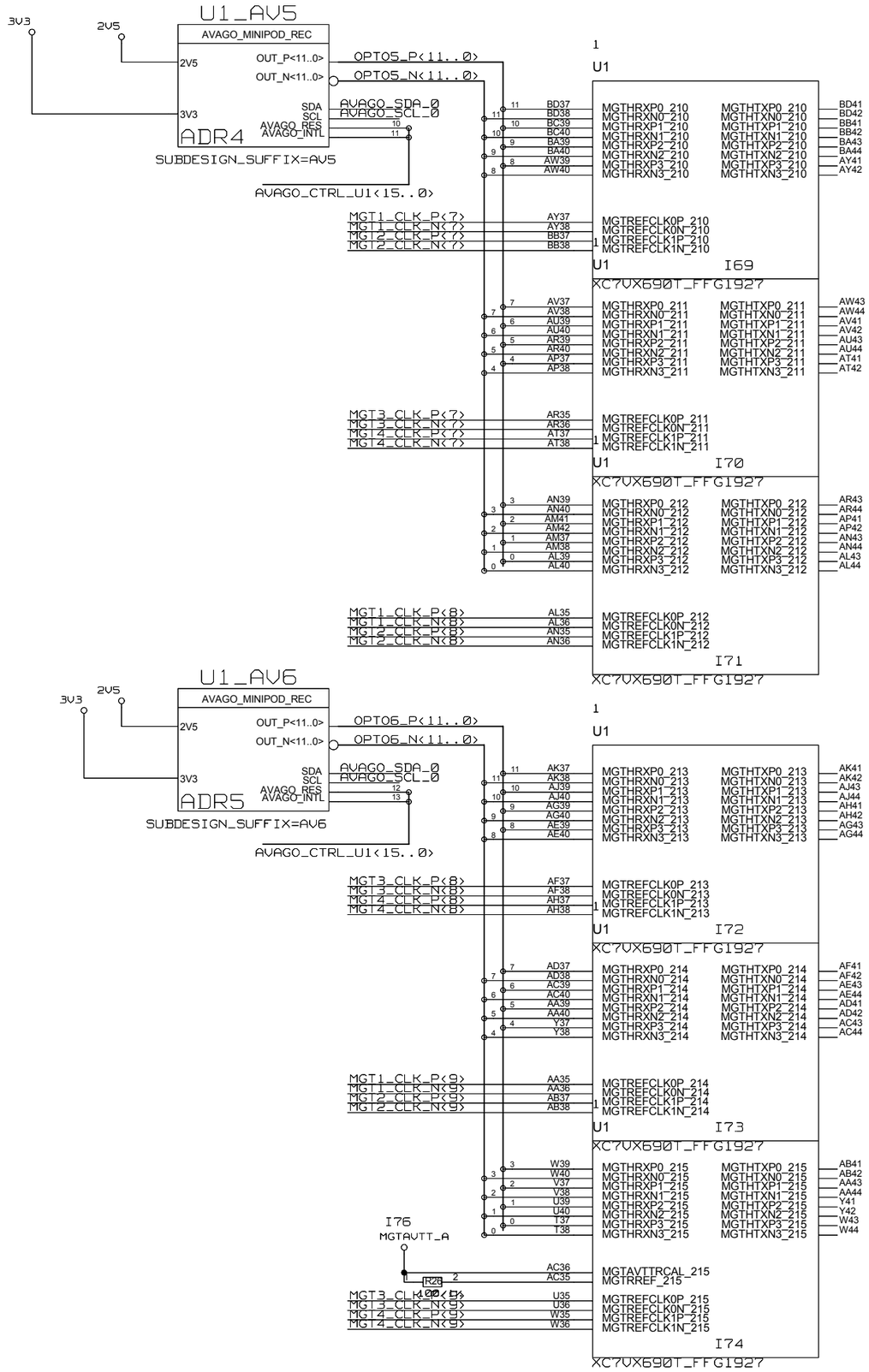

UNIVERSITY OF MAINZ	DRAWING TITLE: OPTO INPUT	
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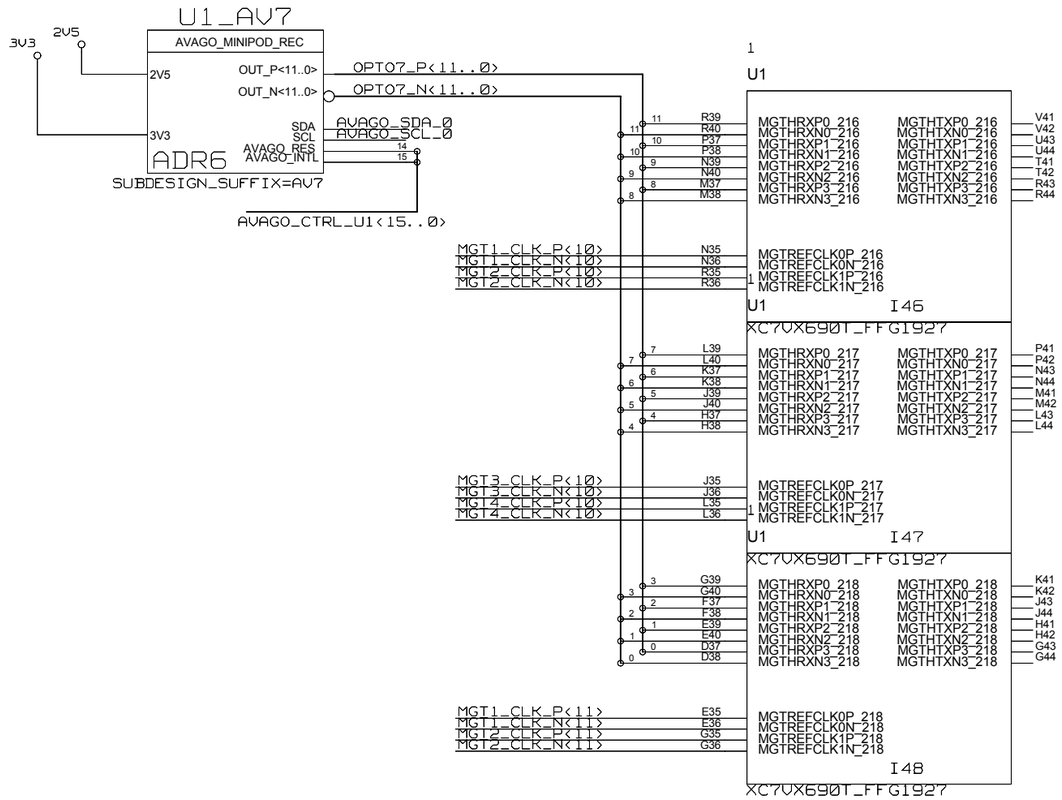
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ		DRAWING TITLE: OPTO INPUT	
BLOCK: PROCESSOR OPTO_IN		SIZE: C	REV.
		DRAWING NO.	
SCALE		SHEET OF	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

U2_AV8

AVAGO_MINIPOD_REC

3V3 2V5 2V5 3V3 SDA SCL AVAGO_RES AVAGO_INTL

OUT_P<11..0> OPTO8_P<11..0>

OUT_N<11..0> OPTO8_N<11..0>

AVAGO_SDA_1 AVAGO_SCL_1

ADR0

SUBDESIGN_SUFFIX=AV8

AVAGO_CTRL_U2<15..0>

U2

BD8	MGTHRXP0_110	MGTHTXP0_110	BD4
BD7	MGTHRXN0_110	MGTHTXN0_110	BD3
BC8	MGTHRXP1_110	MGTHTXP1_110	BB4
BC5	MGTHRXN1_110	MGTHTXN1_110	BB3
BA6	MGTHRXP2_110	MGTHTXP2_110	BA2
BA5	MGTHRXN2_110	MGTHTXN2_110	BA1
AW6	MGTHRXP3_110	MGTHTXP3_110	AY4
AW5	MGTHRXN3_110	MGTHTXN3_110	AY3
AY8	MGTREFCLK0P_110		
AY7	MGTREFCLK0N_110		
BB8	MGTREFCLK1P_110		
BB7	MGTREFCLK1N_110		

U2 I33 XC7VX690T_FFG1927

NC VX485

AV8	MGTHRXP0_111	MGTHTXP0_111	AW2
AV7	MGTHRXN0_111	MGTHTXN0_111	AW1
AU6	MGTHRXP1_111	MGTHTXP1_111	AV4
AU5	MGTHRXN1_111	MGTHTXN1_111	AV3
AR6	MGTHRXP2_111	MGTHTXP2_111	AU2
AR5	MGTHRXN2_111	MGTHTXN2_111	AU1
AP8	MGTHRXP3_111	MGTHTXP3_111	AT4
AP7	MGTHRXN3_111	MGTHTXN3_111	AT3
AR10	MGTREFCLK0P_111		
AR9	MGTREFCLK0N_111		
AT8	MGTREFCLK1P_111		
AT7	MGTREFCLK1N_111		

U2 I28 XC7VX690T_FFG1927

AN6	MGTHRXP0_112	MGTHTXP0_112	AR2
AN5	MGTHRXN0_112	MGTHTXN0_112	AR1
AM4	MGTHRXP1_112	MGTHTXP1_112	AP4
AM3	MGTHRXN1_112	MGTHTXN1_112	AP3
AM8	MGTHRXP2_112	MGTHTXP2_112	AN2
AM7	MGTHRXN2_112	MGTHTXN2_112	AN1
AL6	MGTHRXP3_112	MGTHTXP3_112	AL2
AL5	MGTHRXN3_112	MGTHTXN3_112	AL1
AL10	MGTREFCLK0P_112		
AL9	MGTREFCLK0N_112		
AN10	MGTREFCLK1P_112		
AN9	MGTREFCLK1N_112		

I27 XC7VX690T_FFG1927

V7_MGTTX_P<7..0>

V7_MGTTX_N<7..0>

U2_AV9

AVAGO_MINIPOD_REC

3V3 2V5 2V5 3V3 SDA SCL AVAGO_RES AVAGO_INTL

OUT_P<11..0> OPTO9_P<11..0>

OUT_N<11..0> OPTO9_N<11..0>

AVAGO_SDA_1 AVAGO_SCL_1

ADR1

SUBDESIGN_SUFFIX=AV9

AVAGO_CTRL_U2<15..0>

U2

AK8	MGTHRXP0_113	MGTHTXP0_113	AK4
AK7	MGTHRXN0_113	MGTHTXN0_113	AK3
AJ6	MGTHRXP1_113	MGTHTXP1_113	AJ2
AJ5	MGTHRXN1_113	MGTHTXN1_113	AJ1
AG6	MGTHRXP2_113	MGTHTXP2_113	AH4
AG5	MGTHRXN2_113	MGTHTXN2_113	AH3
AE6	MGTHRXP3_113	MGTHTXP3_113	AG2
AE5	MGTHRXN3_113	MGTHTXN3_113	AG1
AF8	MGTREFCLK0P_113		
AF7	MGTREFCLK0N_113		
AH8	MGTREFCLK1P_113		
AH7	MGTREFCLK1N_113		

U2 I70 XC7VX690T_FFG1927

AD8	MGTHRXP0_114	MGTHTXP0_114	AF4
AD7	MGTHRXN0_114	MGTHTXN0_114	AF3
AC6	MGTHRXP1_114	MGTHTXP1_114	AE2
AC5	MGTHRXN1_114	MGTHTXN1_114	AE1
AA6	MGTHRXP2_114	MGTHTXP2_114	AD4
AA5	MGTHRXN2_114	MGTHTXN2_114	AD3
Y8	MGTHRXP3_114	MGTHTXP3_114	AC2
Y7	MGTHRXN3_114	MGTHTXN3_114	AC1
AA10	MGTREFCLK0P_114		
AA9	MGTREFCLK0N_114		
AB8	MGTREFCLK1P_114		
AB7	MGTREFCLK1N_114		

U2 I69 XC7VX690T_FFG1927

W6	MGTHRXP0_115	MGTHTXP0_115	AB4
W5	MGTHRXN0_115	MGTHTXN0_115	AB3
V8	MGTHRXP1_115	MGTHTXP1_115	AA2
V7	MGTHRXN1_115	MGTHTXN1_115	AA1
U6	MGTHRXP2_115	MGTHTXP2_115	Y4
U5	MGTHRXN2_115	MGTHTXN2_115	Y3
T8	MGTHRXP3_115	MGTHTXP3_115	W2
T7	MGTHRXN3_115	MGTHTXN3_115	W1
AC10	MGTAVTTRCAL_115		
AC9	MGTRREF_115		
U10	MGTREFCLK0P_115		
U9	MGTREFCLK0N_115		
W10	MGTREFCLK1P_115		
W9	MGTREFCLK1N_115		

MGTAVTT_B

R27 200 1%

I68 XC7VX690T_FFG1927

U1_AV16

AVAGO_MINIPOD_TRAN

2V5 3V3 SDA SCL AVAGO_RES AVAGO_INTL

IN_P<11..0> OPTO_T2_P<11..0>

IN_N<11..0> OPTO_T2_N<11..0>

AVAGO_SDA_1 AVAGO_SCL_1

ADR7

SUBDESIGN_SUFFIX=AV16

AVAGO_CTRL_U2<15..0>

3V3 2V5

MGT1_CLK_P<13>	AY8		
MGT1_CLK_N<13>	AY7		
MGT2_CLK_P<13>	BB8		
MGT2_CLK_N<13>	BB7		
MGT3_CLK_P<13>	AR10		
MGT3_CLK_N<13>	AR9		
MGT4_CLK_P<13>	AT8		
MGT4_CLK_N<13>	AT7		
MGT1_CLK_P<14>	AL10		
MGT1_CLK_N<14>	AL9		
MGT2_CLK_P<14>	AN10		
MGT2_CLK_N<14>	AN9		
MGT3_CLK_P<14>	AF8		
MGT3_CLK_N<14>	AF7		
MGT4_CLK_P<14>	AH8		
MGT4_CLK_N<14>	AH7		
MGT1_CLK_P<15>	AA10		
MGT1_CLK_N<15>	AA9		
MGT2_CLK_P<15>	AB8		
MGT2_CLK_N<15>	AB7		
MGT3_CLK_P<15>	U10		
MGT3_CLK_N<15>	U9		
MGT4_CLK_P<15>	W10		
MGT4_CLK_N<15>	W9		

UNIVERSITY OF MAINZ		DRAWING TITLE: OPTO INPUT B OPTO OUTPUT	
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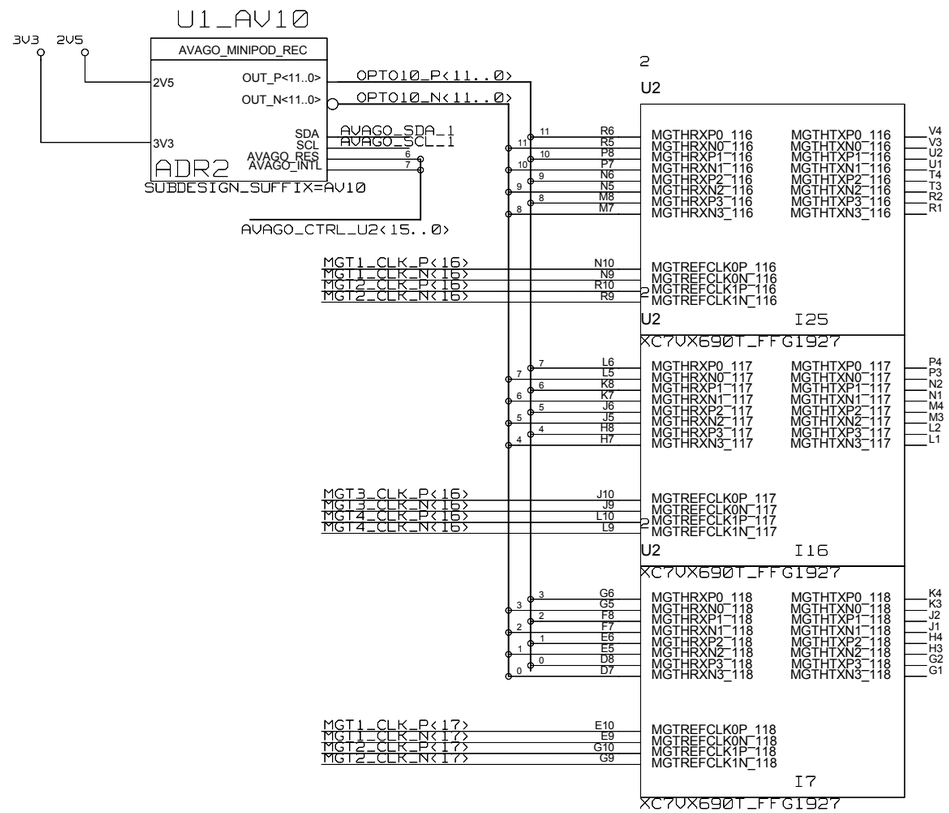
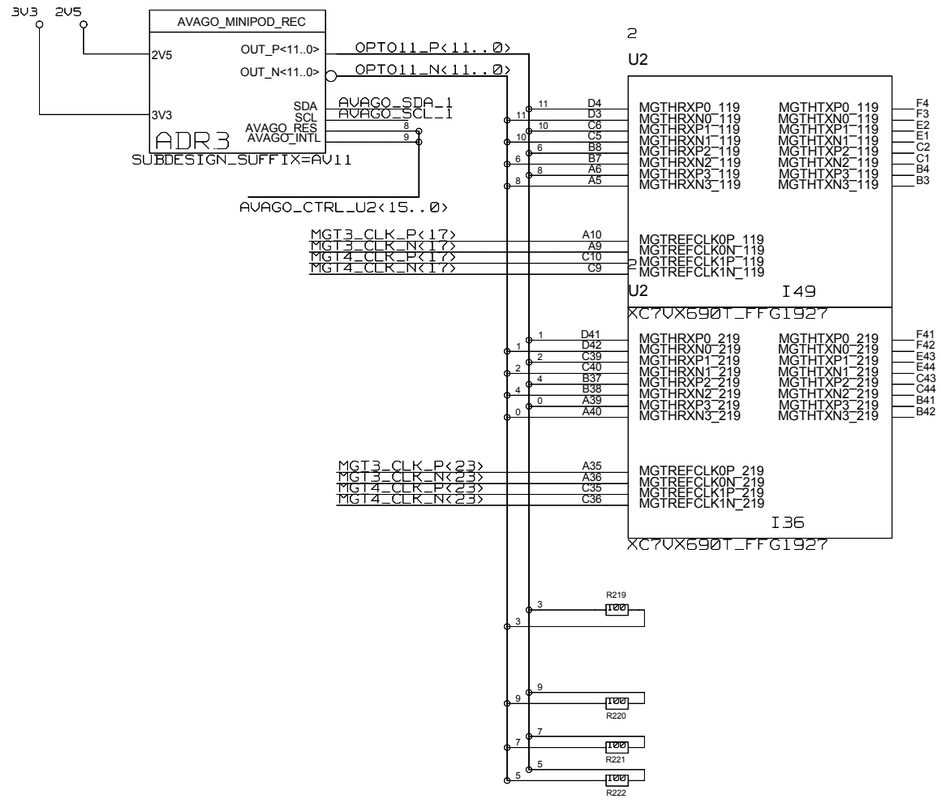
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





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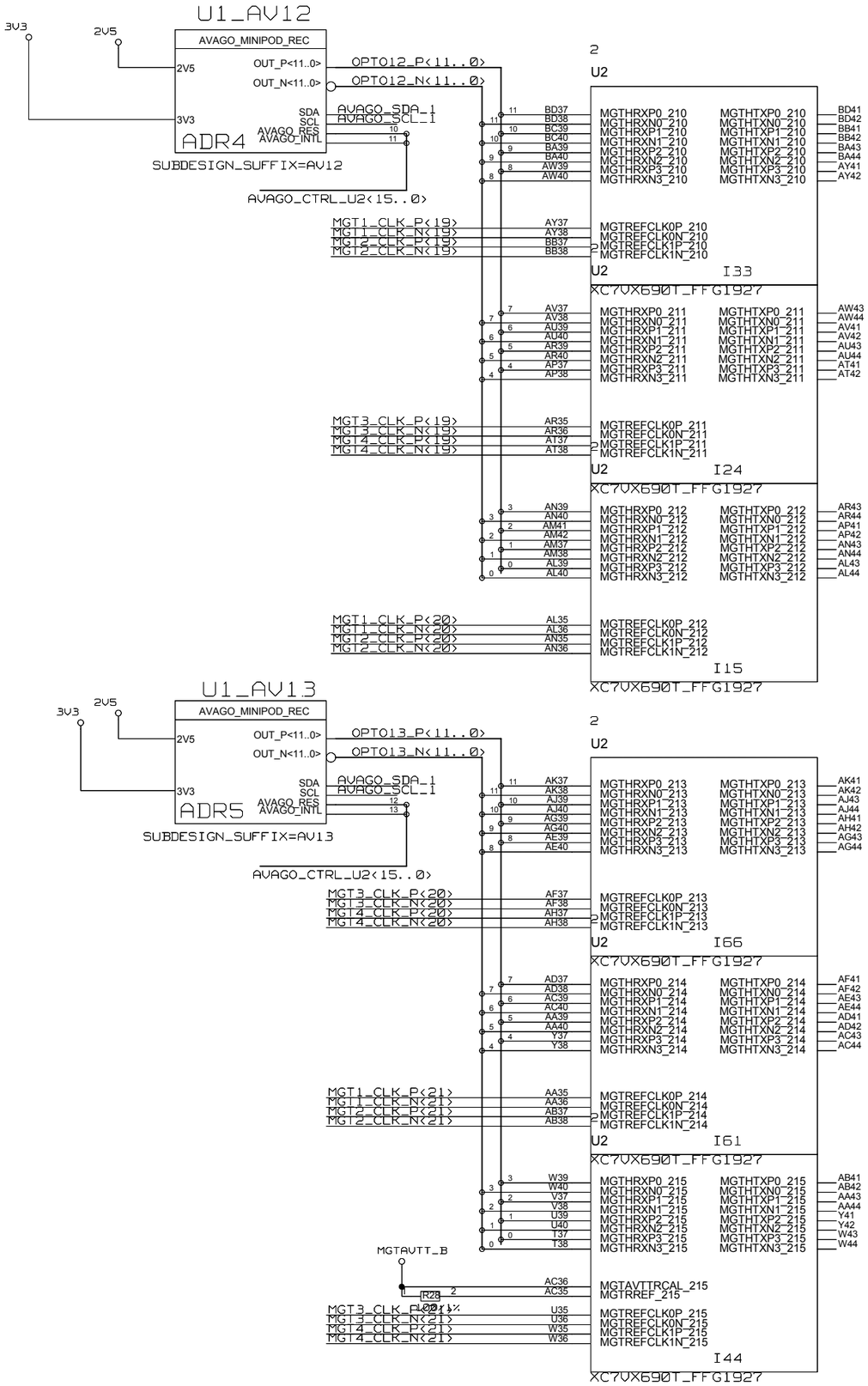
ZONE	LTR	DESCRIPTION	DATE	APPR.



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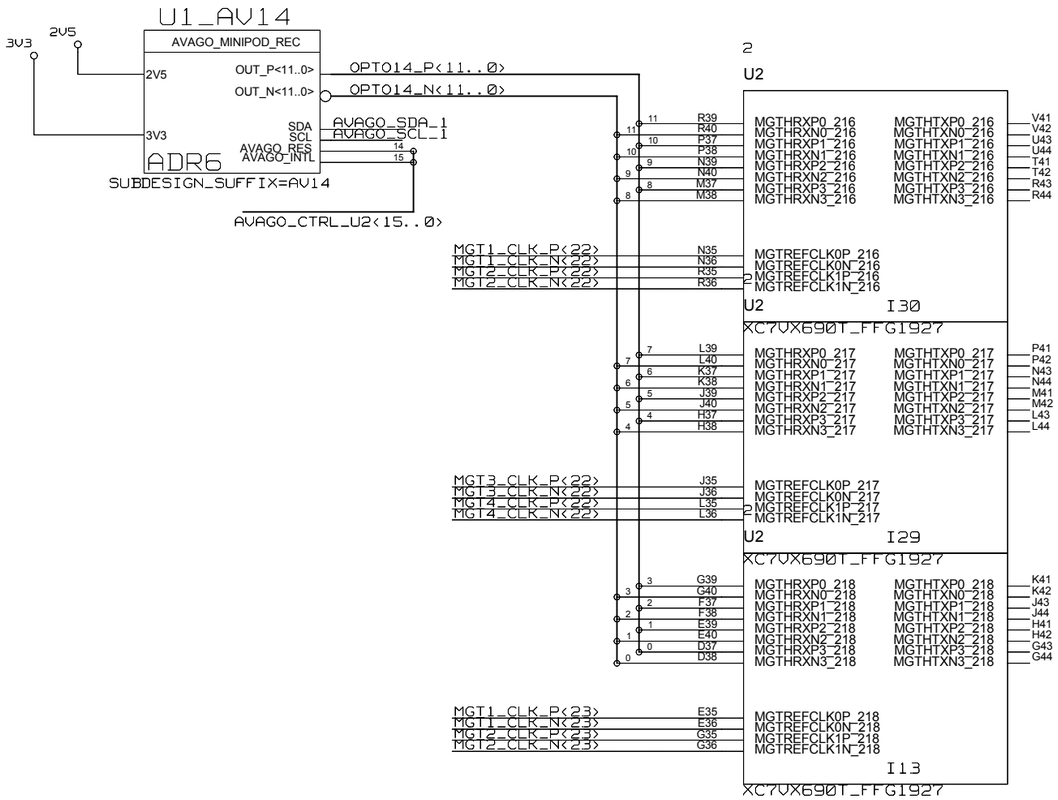
ZONE	LTR	DESCRIPTION	DATE	APPR.



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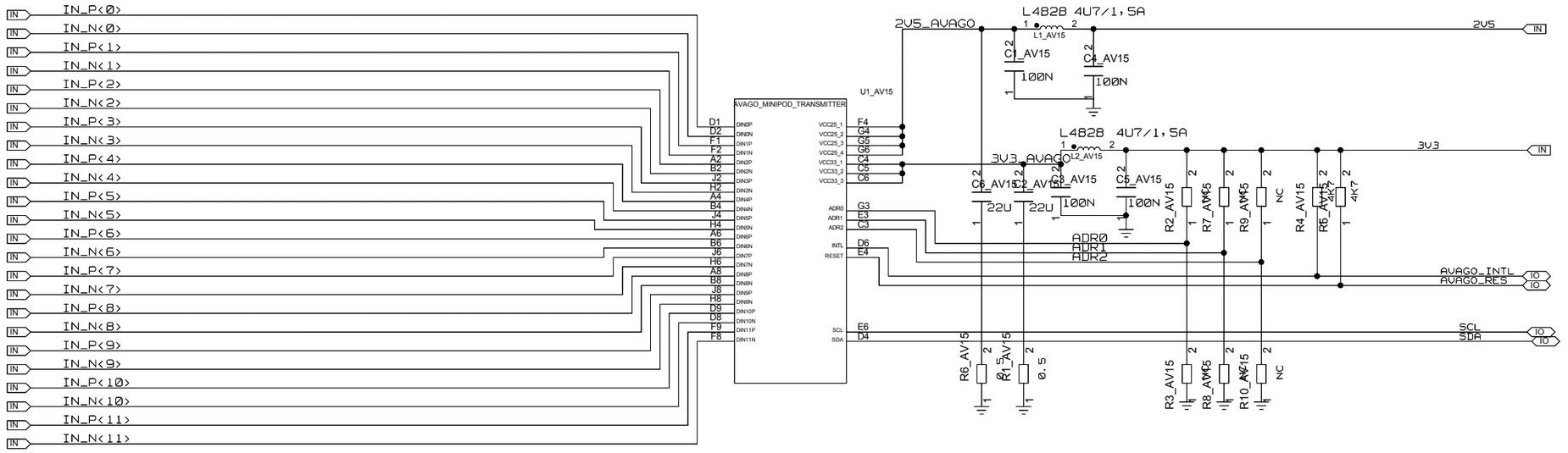

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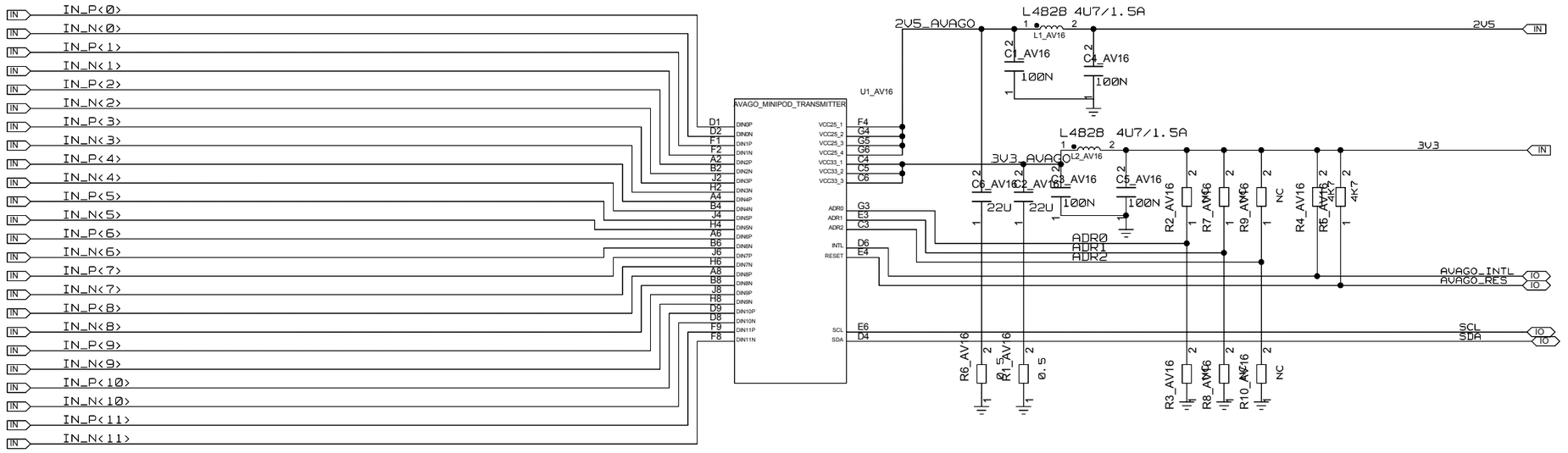

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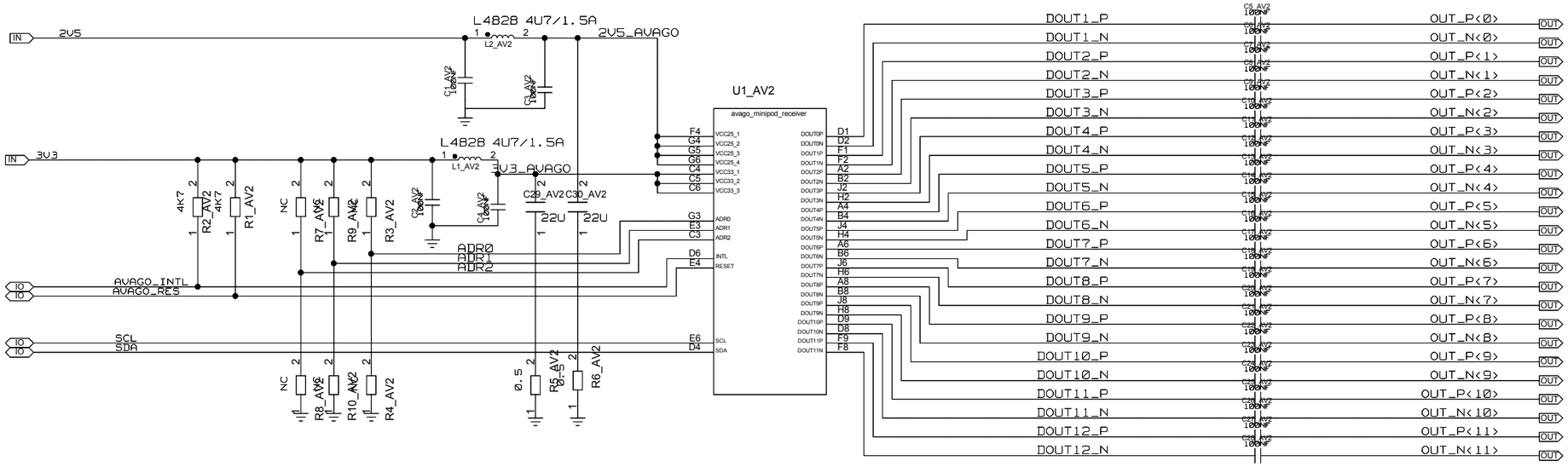
ZONE	LTR	DESCRIPTION	DATE	APPR.



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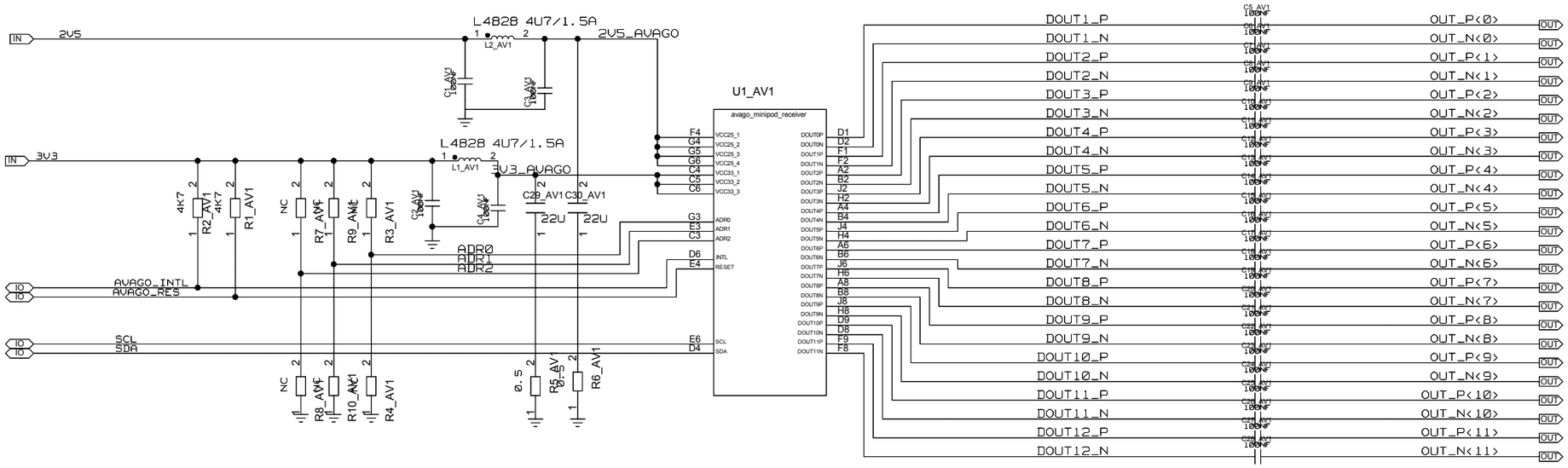

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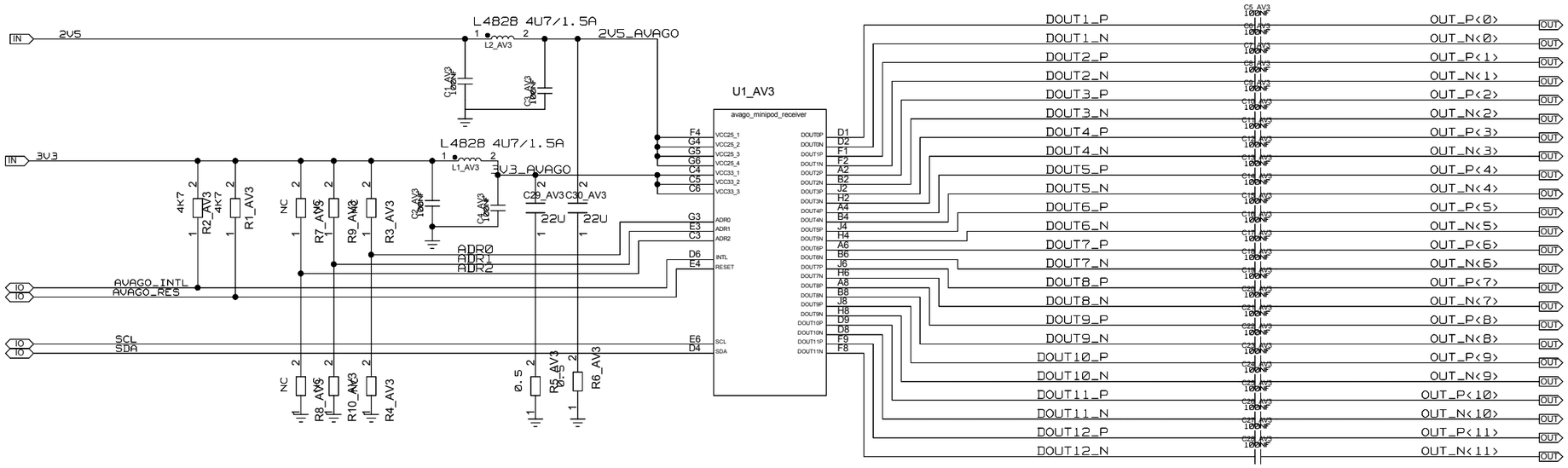

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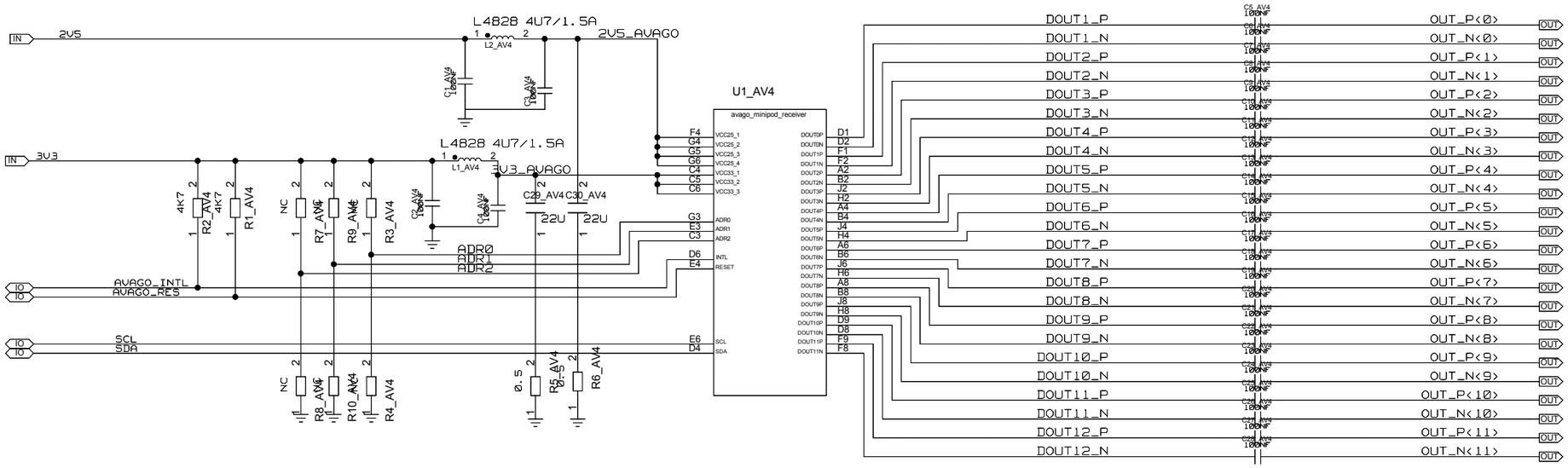

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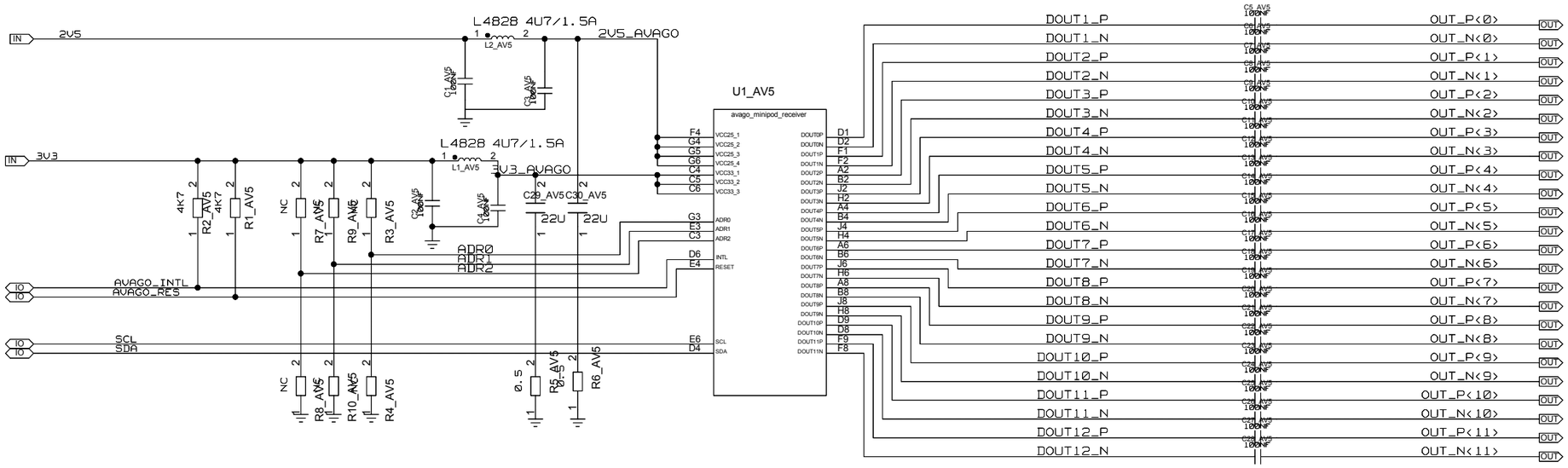

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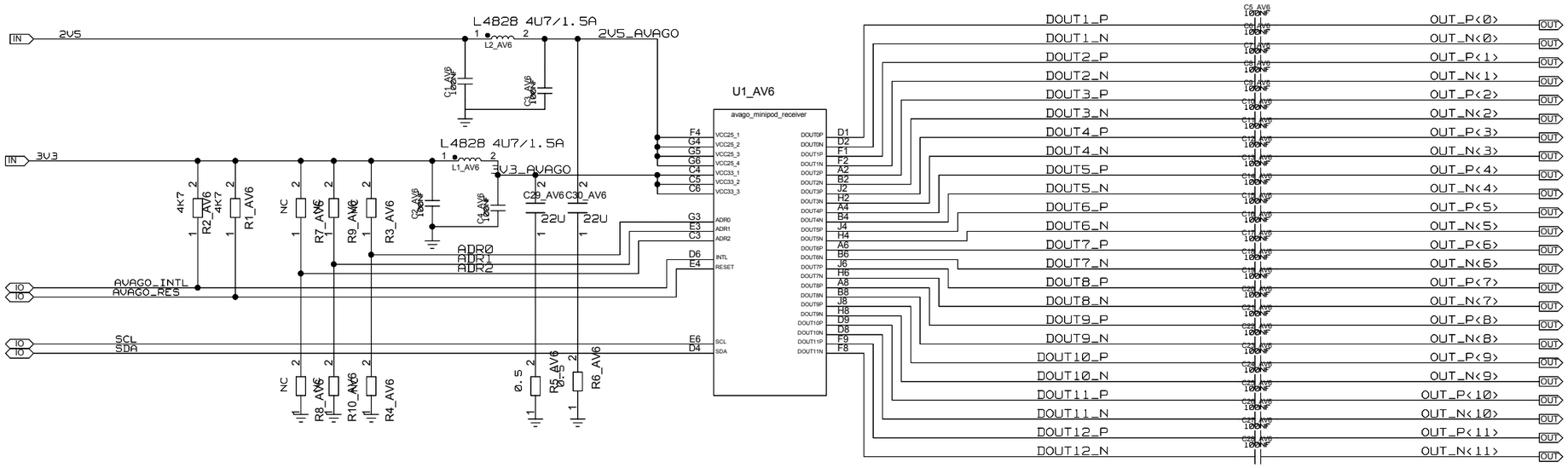

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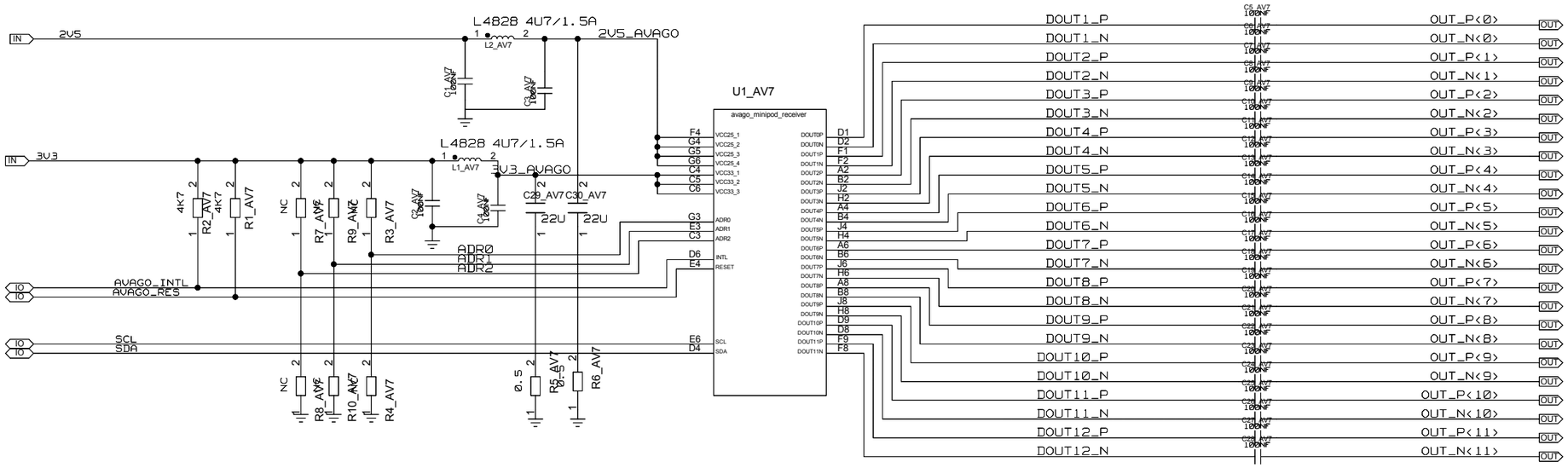

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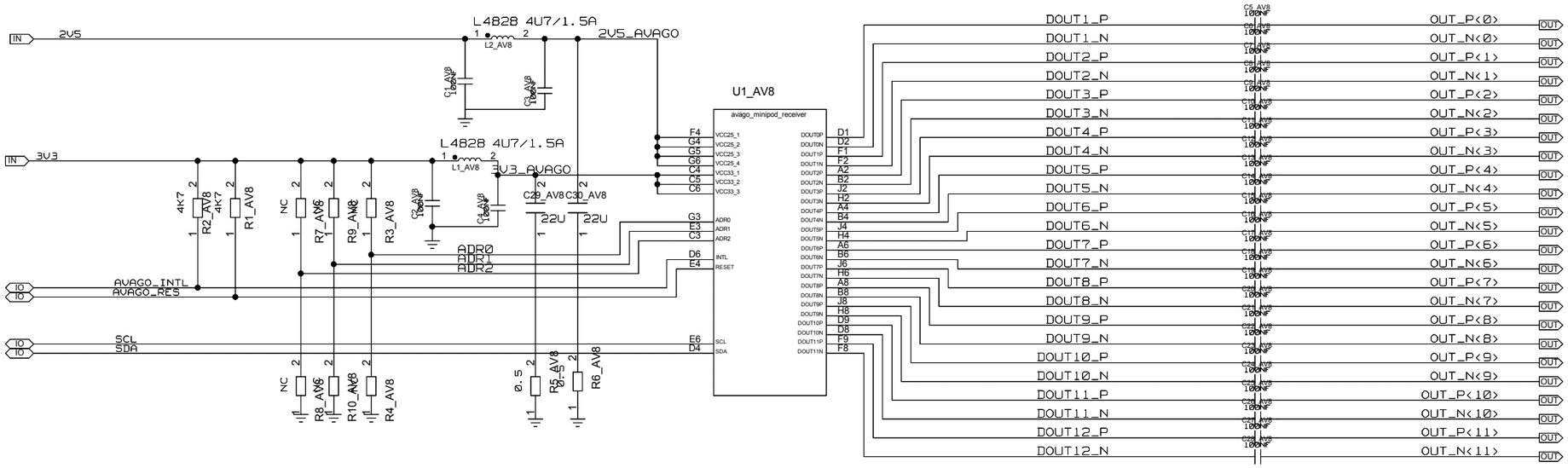

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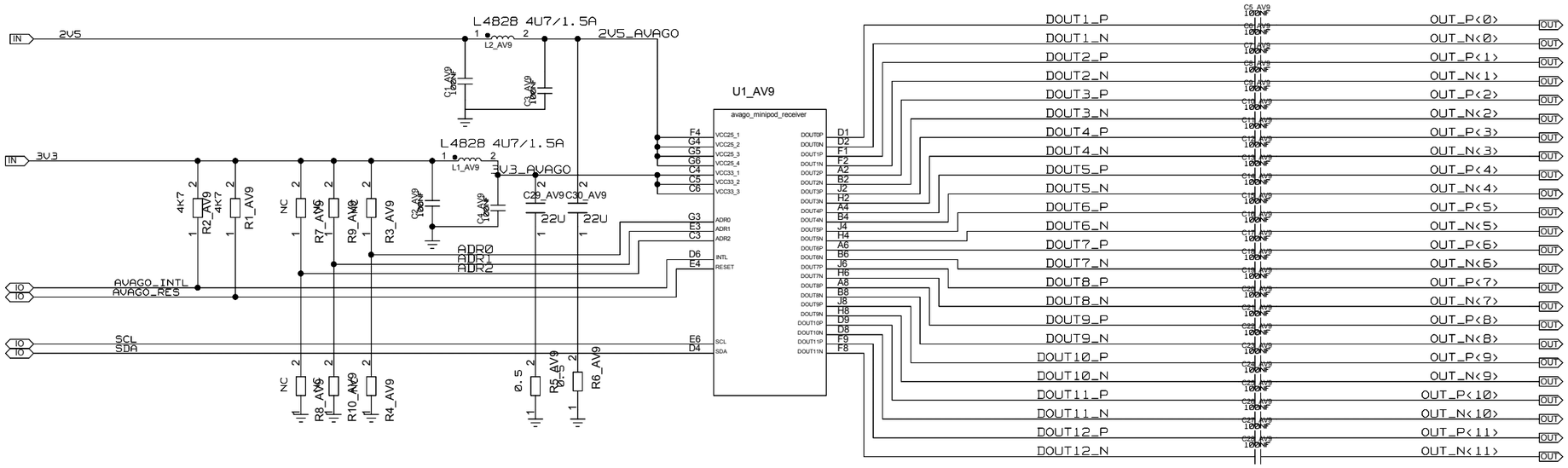

UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO RECEIVER	
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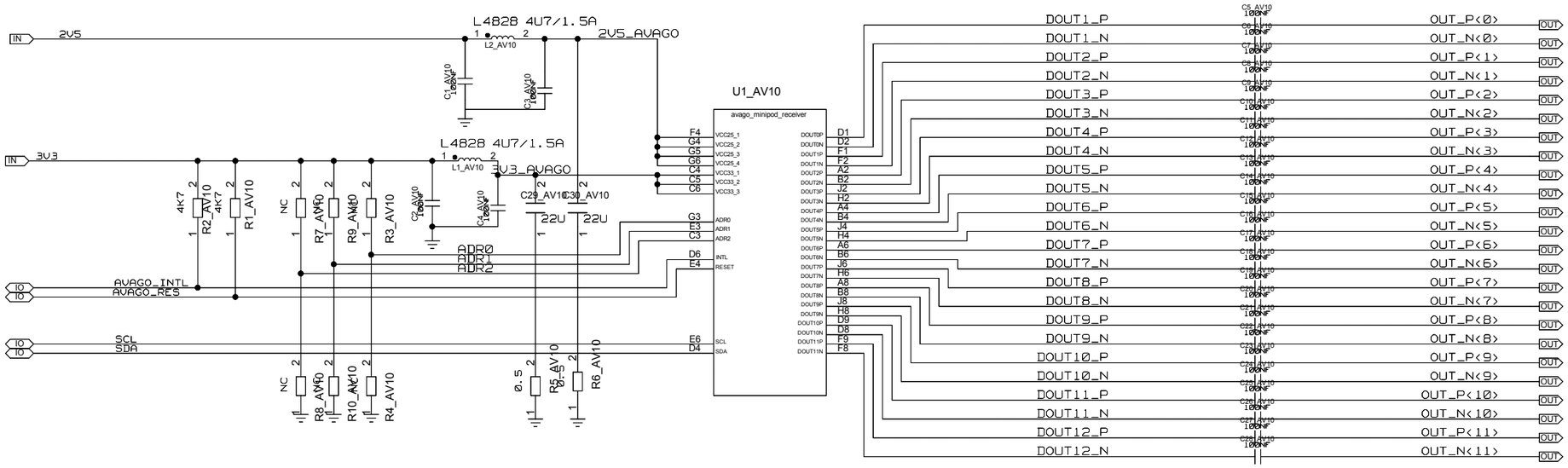

UNIVERSITY OF MAINZ

DRAWING TITLE: AVAGO RECEIVER

SIZE	REV.	DRAWING NO.
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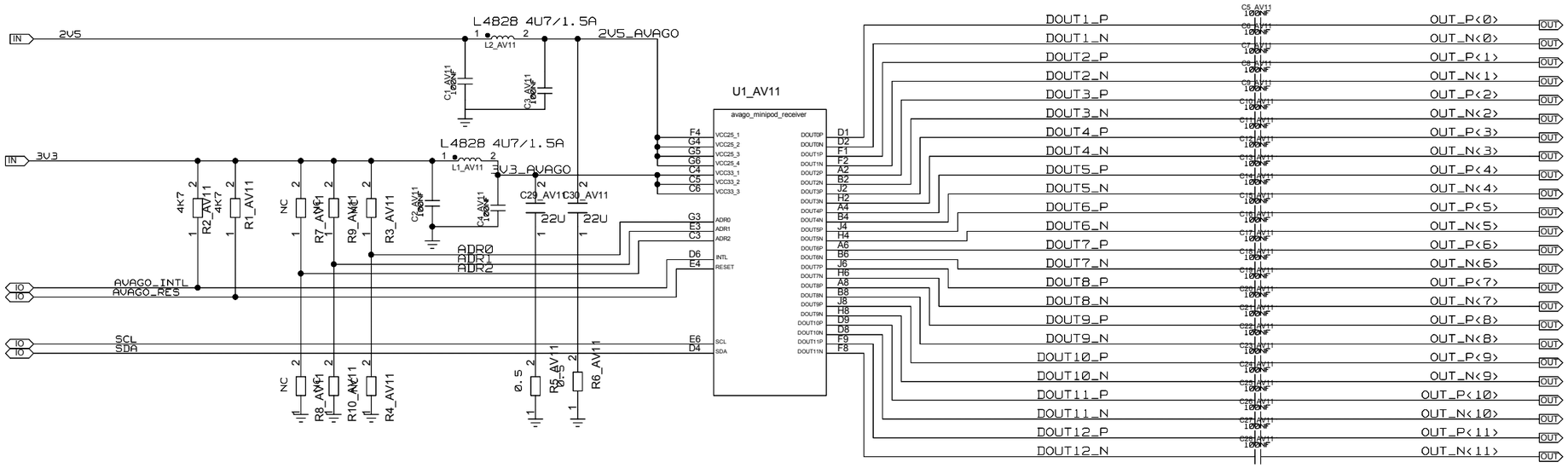
SCALE | SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



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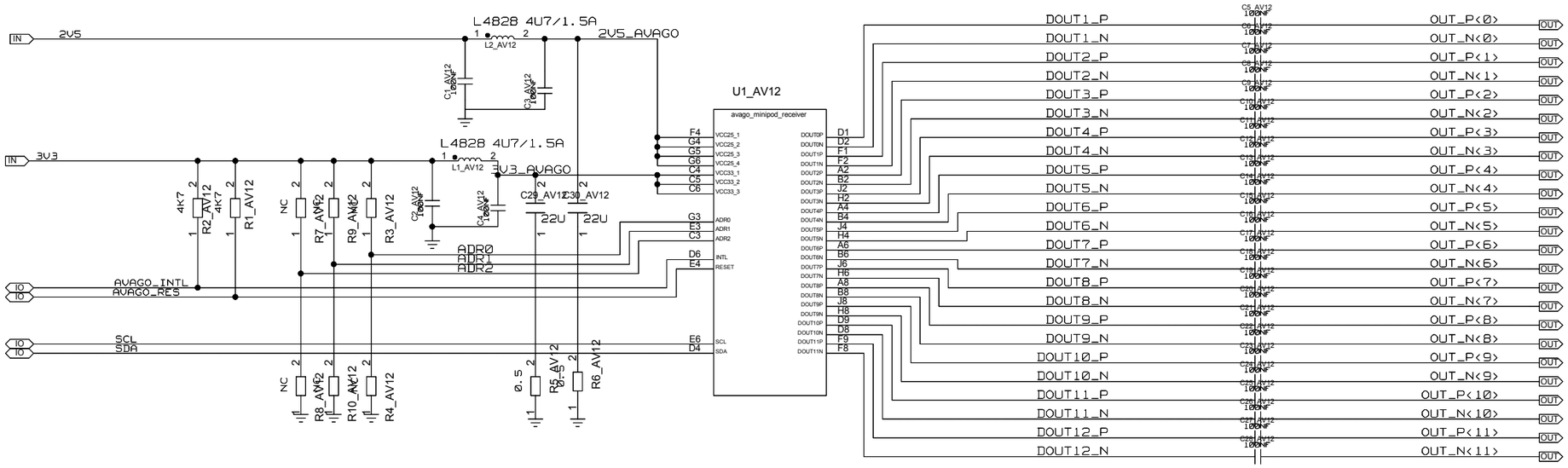

UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO RECEIVER	
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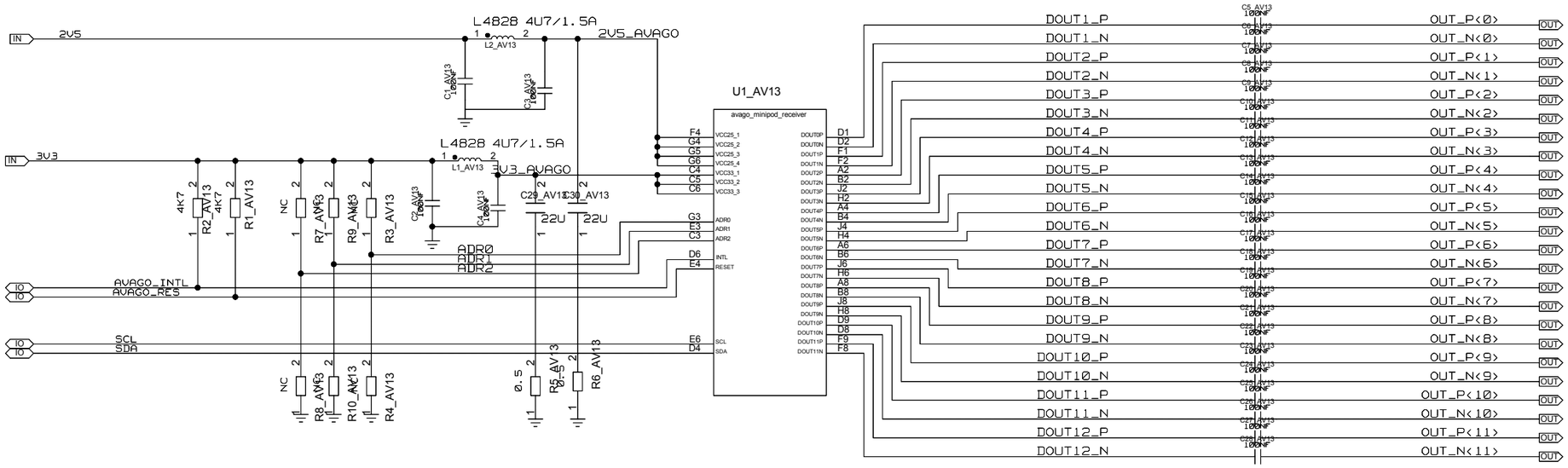
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO RECEIVER		
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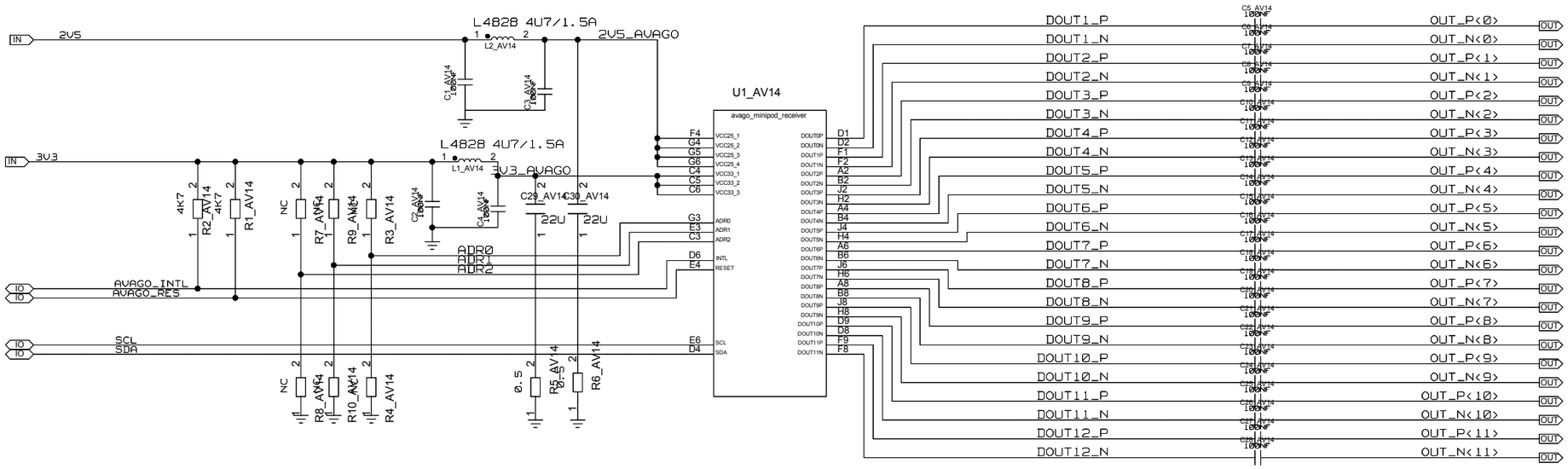
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO RECEIVER		
	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

U1_KR1

AVAGO_MINIPOD_REC

SUBDESIGN_SUFFIX=KR1

U1_KT1

AVAGO_MINIPOD_TRAN

SUBDESIGN_SUFFIX=KT1

U3 — XC7K1325T_FBG900?

CLOCK_LVPECL_SI591_AC — 100MHZ — S-LINK

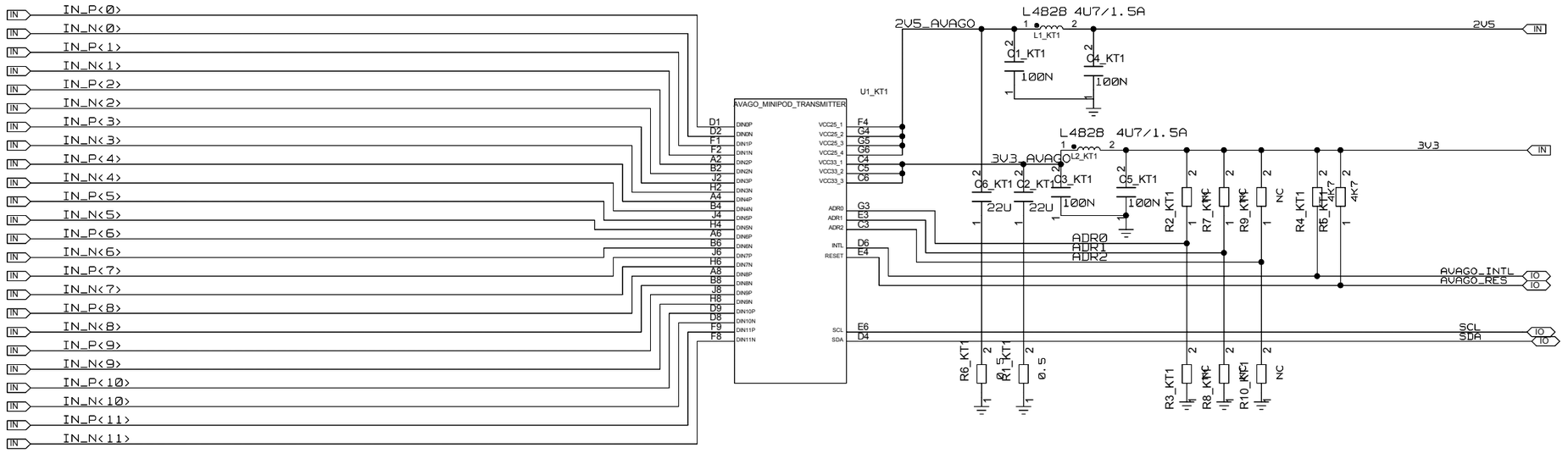
CLOCK_LVPECL_SI591_AC — XXXMHZ

CLOCK_LVPECL_SI591_AC — 125MHZ — VME

TO EXT MODUL

DRAWING TITLE			
UNIVERSITY OF MAINZ	DAQ AND ROI VME		
BLOCK: PROCESSOR KINTEX7_OPTO	SIZE C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO TRANSMITTER		
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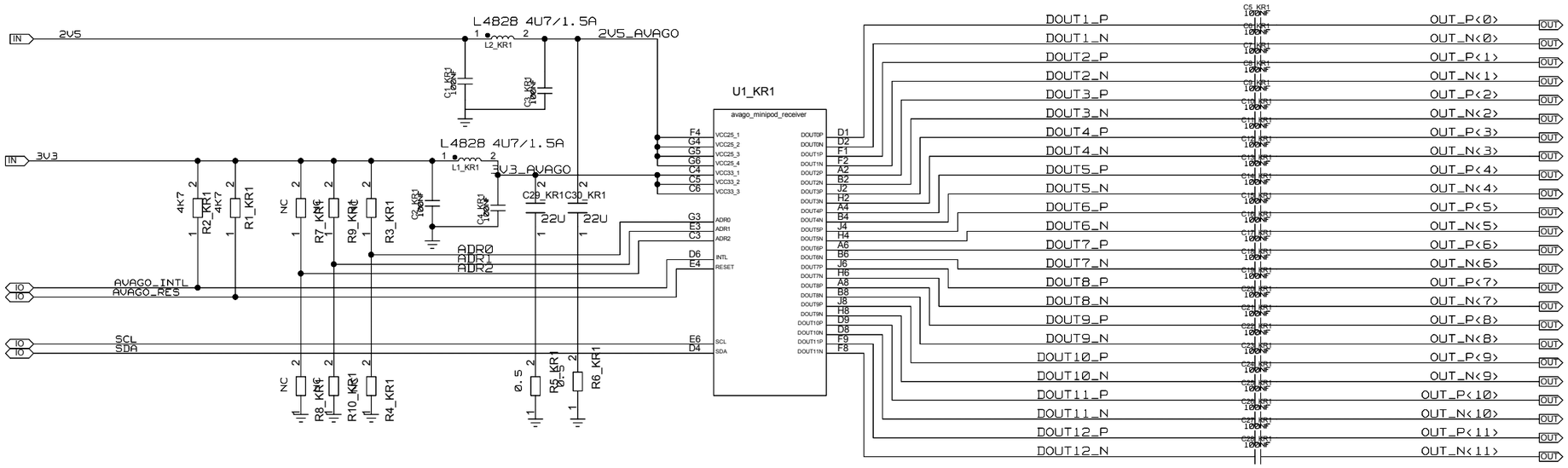
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: AVAGO RECEIVER		
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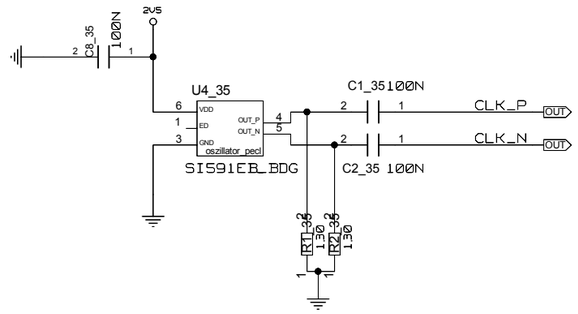
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC	
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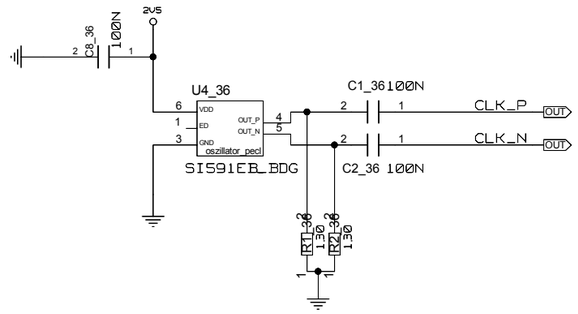
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC	
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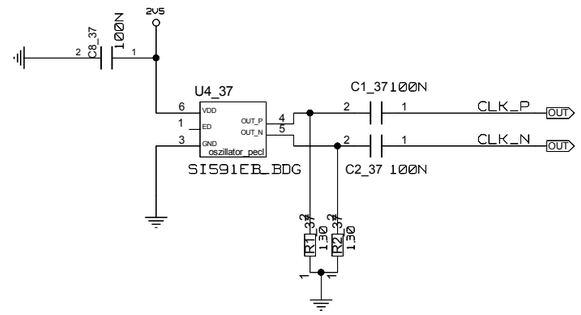
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC	
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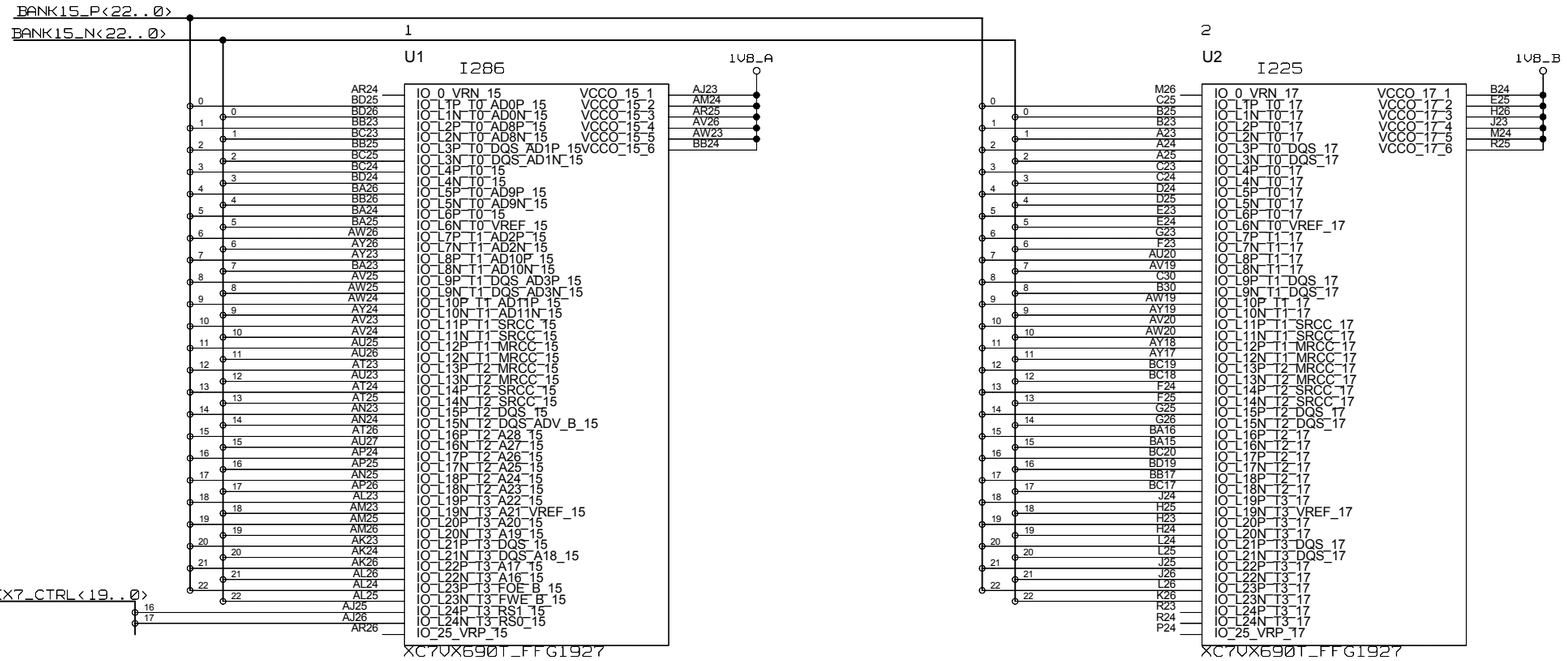
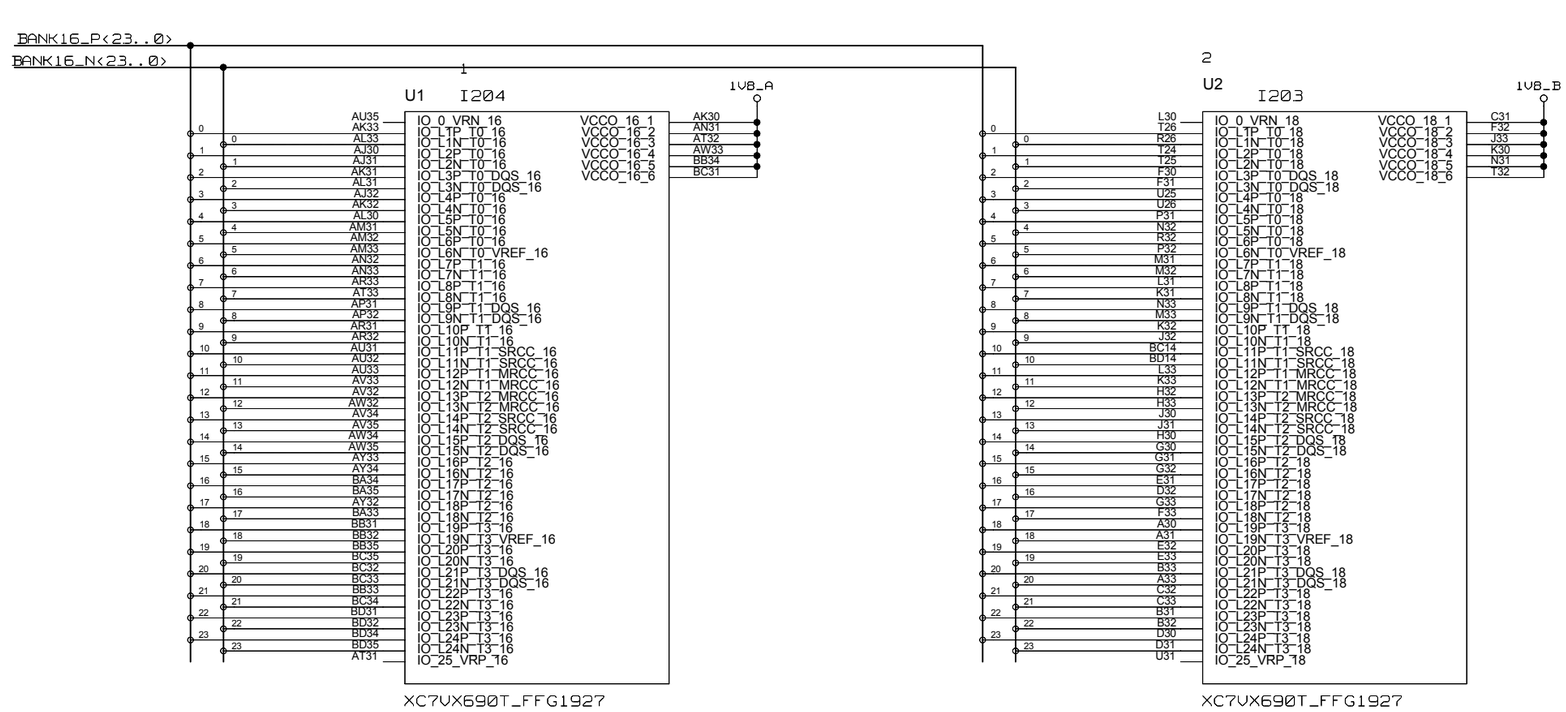
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





UNIVERSITY OF MAINZ		DRAWING TITLE: DATABUS	
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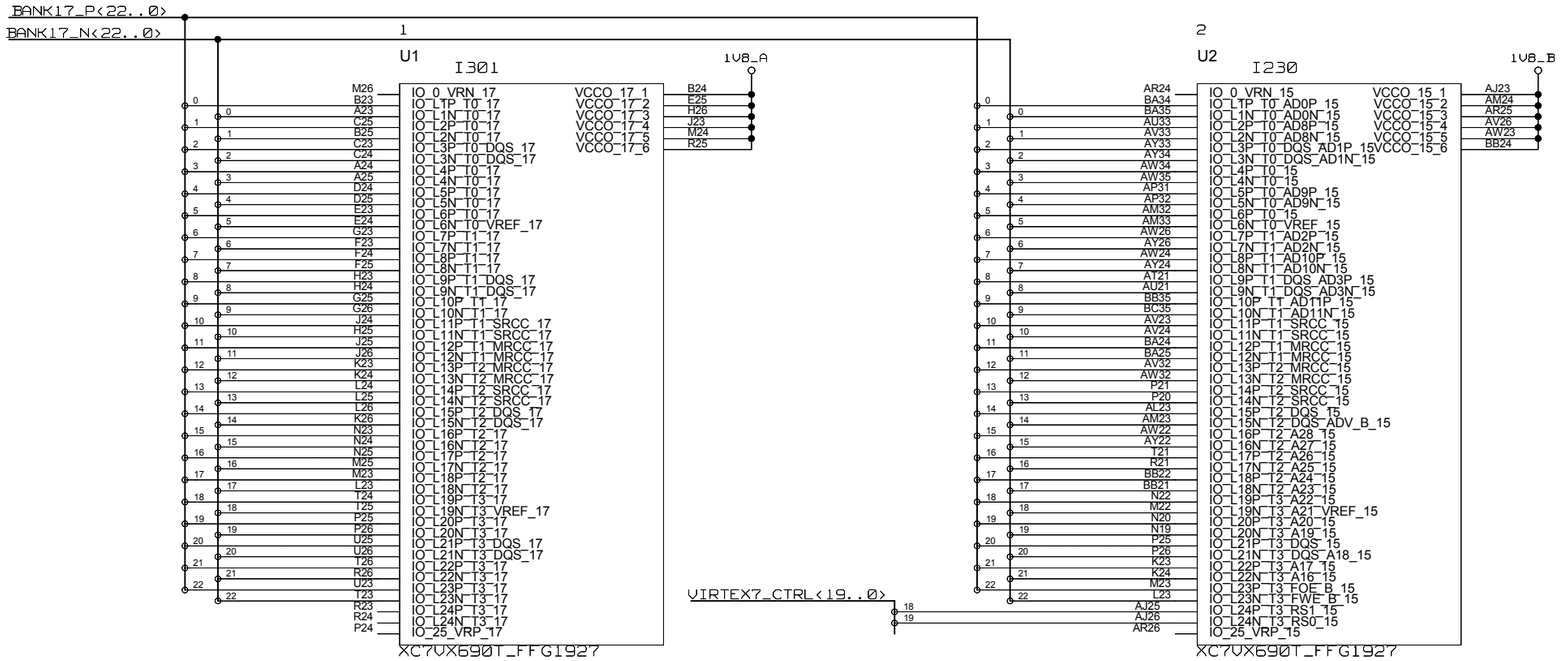
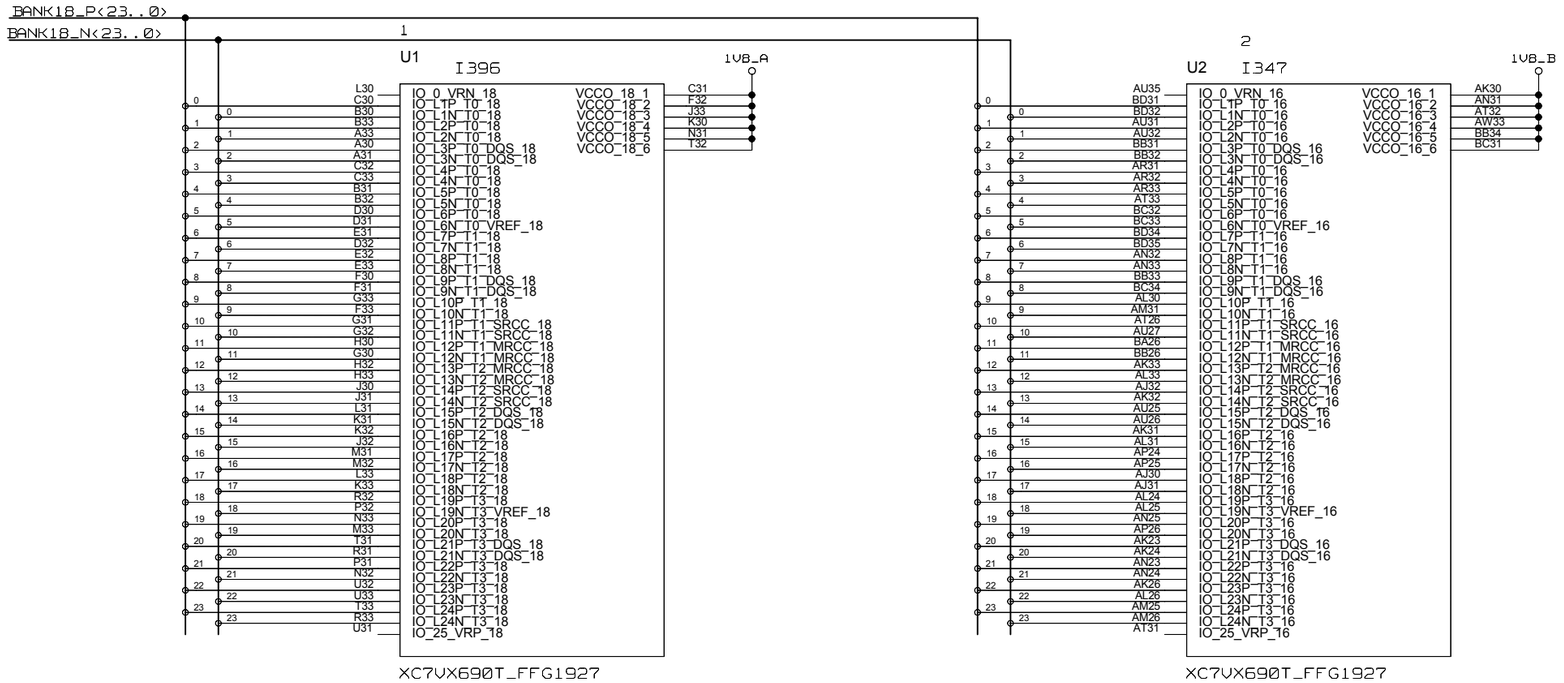
		DRAWING NO.	
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





UNIVERSITY OF MAINZ

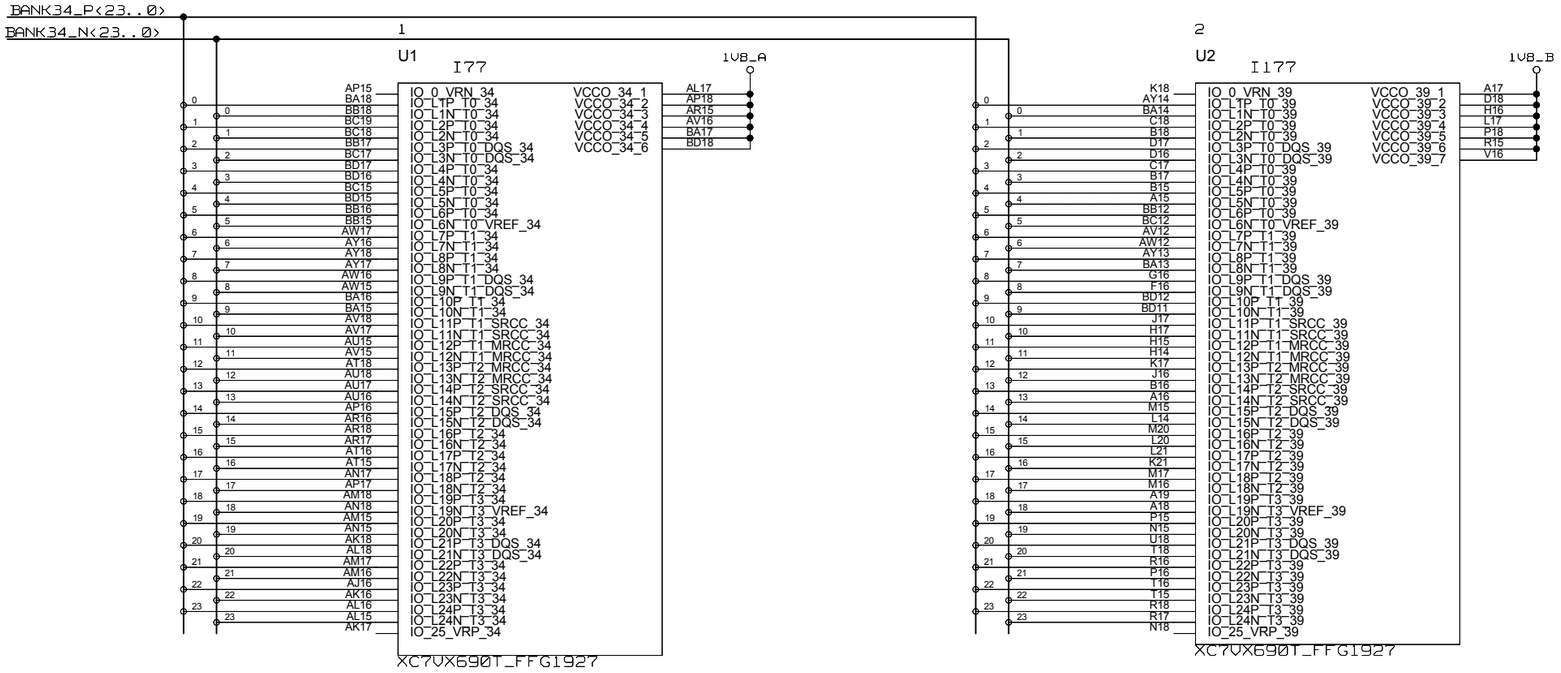
BLOCK: PROCESSOR
DATA_BUS

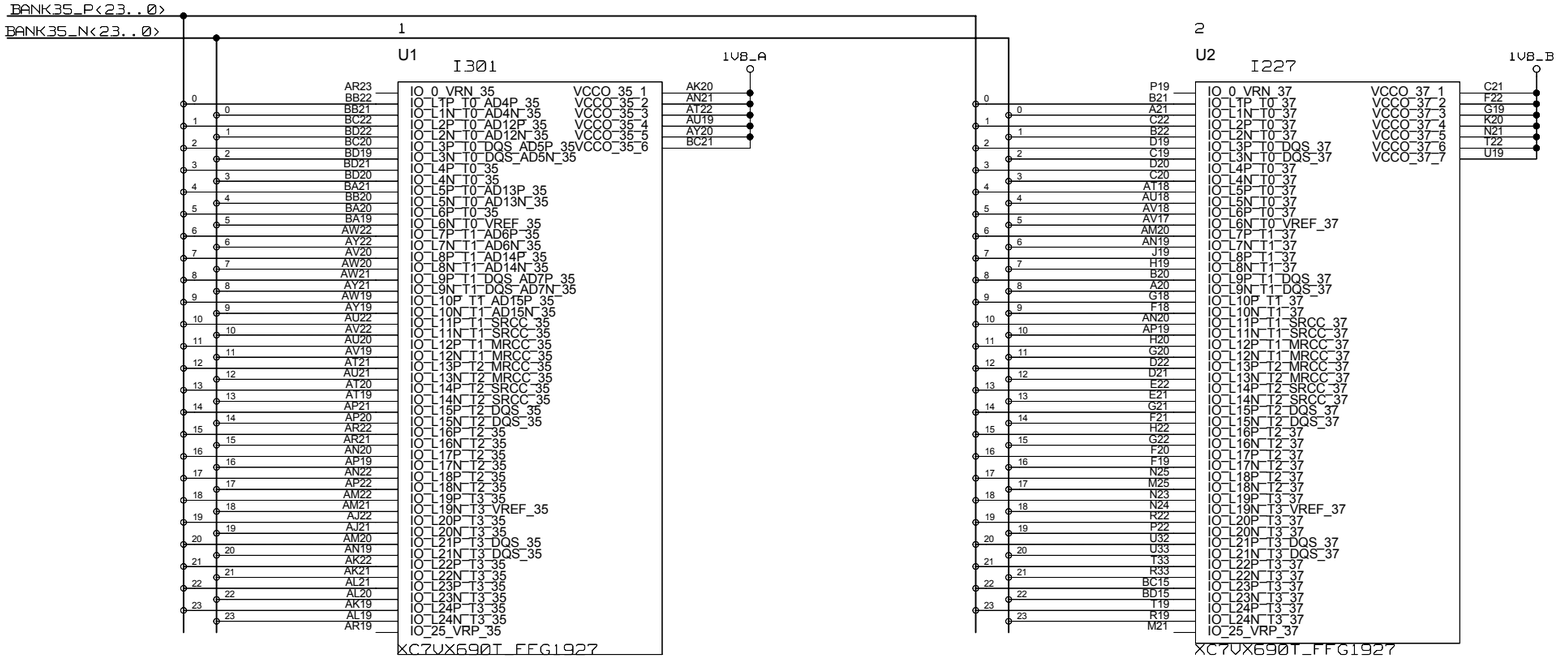
DRAWING TITLE: DATABUS

SIZE: C | REV. | DRAWING NO.

SCALE | SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





UNIVERSITY OF MAINZ		DRAWING TITLE: DATABUS	
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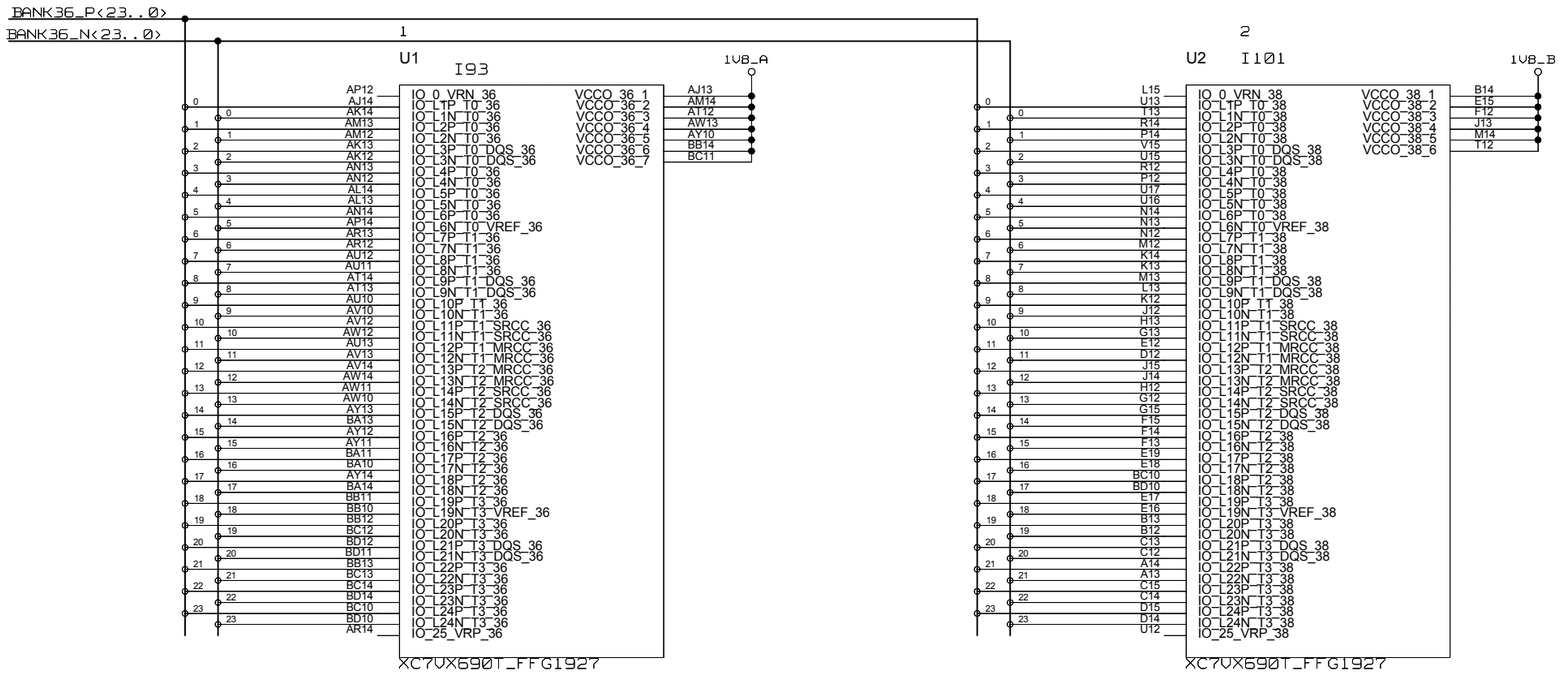
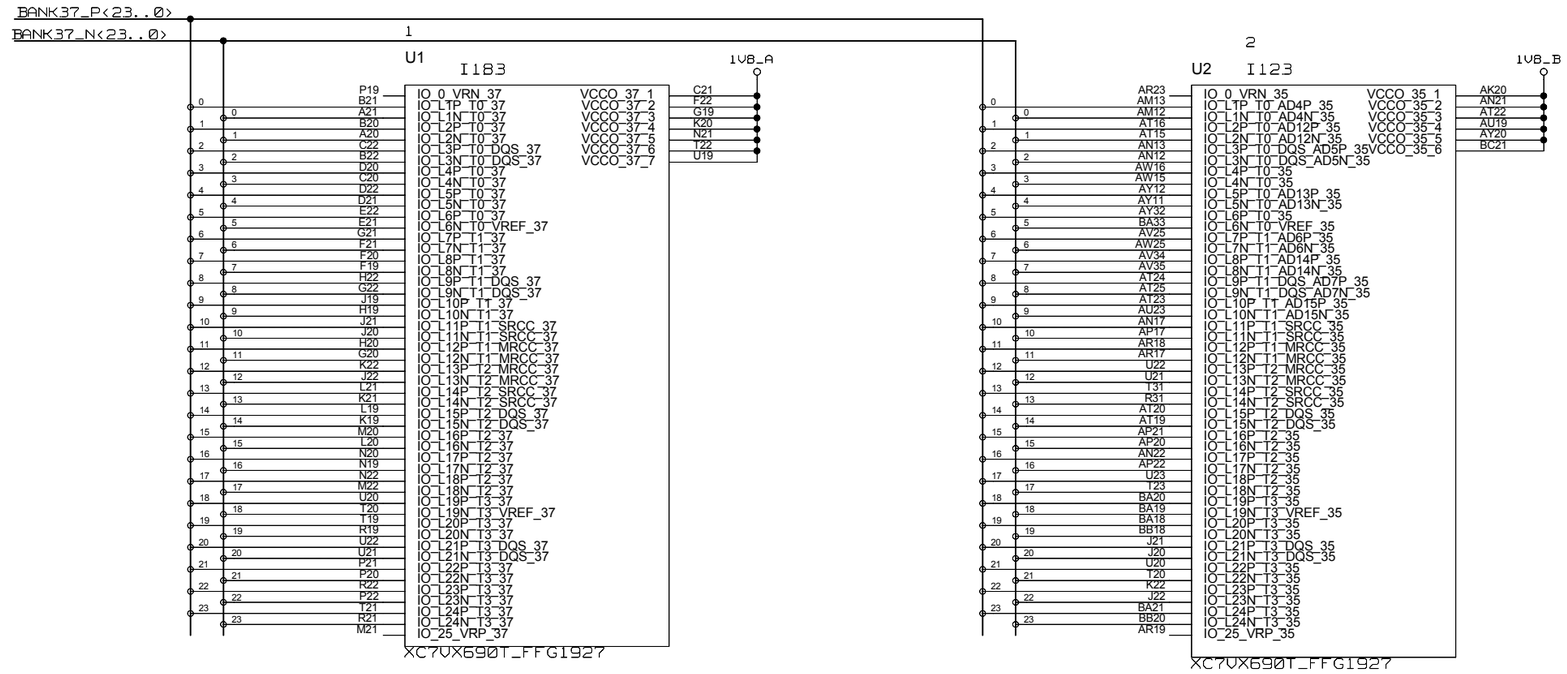
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





UNIVERSITY OF MAINZ		DRAWING TITLE: DATABUS	
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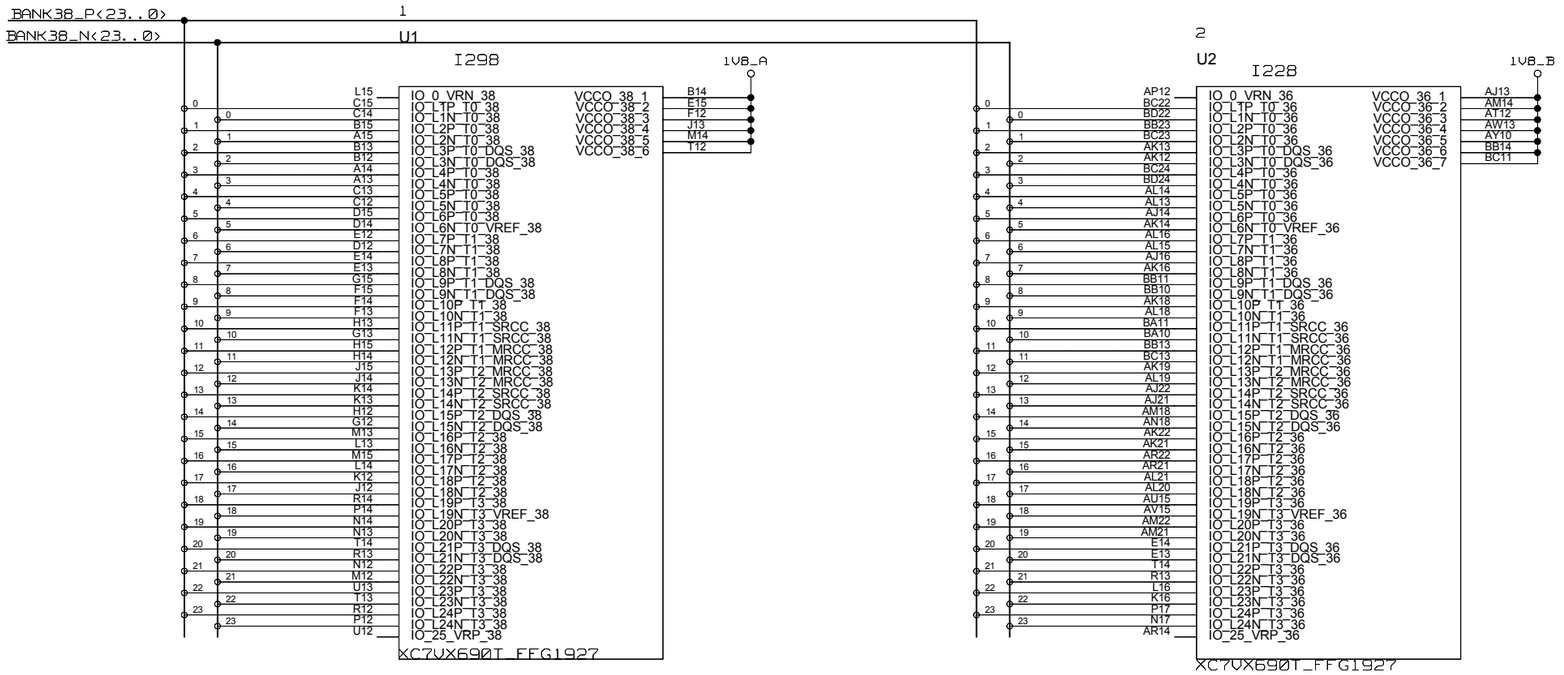
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ		DRAWING TITLE: DATABUS	
BLOCK: PROCESSOR DATA_BUS		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

PTH08T220W	3V3	1K21
PTH08T220W	2V5	2K37
PTH08T220W	1V0	20K5
PTH08T240W	1V0	20K5
PTH08T240W	1V2	12K1
SIL20C2	1V0	2K87
SIL20C2	1V8	976R
LDO06C	1V0	2K87
LDO06C	1V2	1K96
LDO06C	3V3	436R
LDO06C	5V0	270R
TPS74401	1V8	3K57/2K87

ATCA POWER IN & CTRL

3V3_UP

J1

FUSE1

POLYFUSE 300MA

JTAG_USB (VREF, TDI, TDO, TMS, TCK, CONNECTOR)

CABLE LOOP TO IPMC JTAG CONNECTOR

J2

TDI, TDO, TMS, TCK

HA0, HA1, HA2, HA3, HA4, HA5, HA6, HA7/P

SCL_A, SDA_A, SCL_B, SDA_B

SHELF_GND, LOGIC_GND

SEGMENT3

ENABLE_B — ENB — NANO2_1A

VRTN_A — VRTN_A — NANO2_15A

VRTN_B — VRTN_B — NANO2_15A

EARLY_A, EARLY_B — R2236, R2238

ENABLE_A — ENA — NANO2_1A

-48V_A — -48V_A — NANO2_12A

-48V_B — -48V_B — NANO2_12A

100R R2512

3V3_UP

R240 R241 R242 R243 R244 R245 R246 R247 10K

ATCA_CTRL<11..0>

C715 C717 C719 C721 1N

C716 C718 C720 C722 1N

DC -48V INPUT

-48V_A, -48V_B

0.22UF/100V, 0.22UF/100V, 5.6NF/1.5KV, 5.6NF/1.5KV

C729 C731 C727 C728 C730 C732

SEGMENT3

VRTN_A, VRTN_B

5.6NF/1.5KV, 5.6NF/1.5KV

AICR250 — atca250

1 -48VA, 2 -48VB, 3 NC, 4 HOLD UP, 5 RTN A, 6 RTN B, 7 ENA, 8 ENB, 9 C-CL-, 10 HU-

REG1

12VOUT, 12VRTN, 3V3TRIM1, 3V3TRIM2, 3V3OUT1, 3V3OUT2, 3V3RTN1, 3V3RTN2, SDA, A0, SCL, A1, INTRPT, A2, A_OK, B_OK

HU+OUT, HU+IN, ON/OFF-, ON/OFF+

IPMC_MGT_I2C_SDA (TO)

IPMC_MGT_I2C_SCL (TO)

C72 C73 C74 C75 — 1000U/50V, 1000U/50V, 1000U/50V, 82U/100V?

PANASONIC EEU-FK1H102M

RUBYCON 100YXGB2MEFC12.5X16

R7 10K, R8 10K, R9 NC, R10 NC, R11 NC, R12 NC

C76 330U/25V, C712 1UF/16V, C713 1UF/16V, C714 47UF/6V

12V, 3V3_UP

3V3_UP

U8 VCC=3V3_UP — SN74AHC1G86 (=1 XOR) — SN74AHC1G86

R1 NC, R2 4K7, C71 100N

IN — PWR_ON

R3 10K, R4 10K, Q2 BSS138

MANUAL POWER-ON

TP GND, GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9, GND10

pad — SEGMENT3 — R5 10M/025W — SEGMENT2 — R6 10M/025W — SEGMENT1

3V3

U14 TPS74401RGWT (tps74401)

IN1–IN4, PG, BIAS, EN, SS, PAD, OUT1–OUT4, FB, GND

C77 4U7, C78 1U, C402

R16 3K57, R17 2K87

1V8_CPLD — C79 4U7, C80 4U7

3V3_UP

C81 100N, R19 NC

U18 VCC=3V3_UP — SN74AHC1G86 (=1 XOR) — SN74AHC1G86

A_OK — OUT

R20 4K7

3V3_UP

C82 100N, R20 NC

U19 VCC=3V3_UP — SN74AHC1G86 (=1 XOR) — SN74AHC1G86

B_OK — OUT

R21 4K7

EN_3V3_K7

12V

C194 NC, R22 0, R39 NC

U9 NC — BSS138

3V3_K7

5V, 12V

LDO06C_POWERSUPPLY (SUBDESIGN_SUFFIX=P16)

VIN, EN, VOUT, GND, MON1, MON2 — MON_5V_1, MON_5V_2

LDO06C_POWERSUPPLY (SUBDESIGN_SUFFIX=P1)

MON_3V3_K7_1, MON_3V3_K7_2

3V3, 12V

PTH08T220W_POWERSUPPLY (SUBDESIGN_SUFFIX=P2)

VIN, VOUT, MON1, MON2, GND, SMARTSYNC — C4, C6, C7 470UF/6.3V

MON_3V3_1, MON_3V3_2

2V5, 12V

PTH08T220W_POWERSUPPLY (SUBDESIGN_SUFFIX=P3)

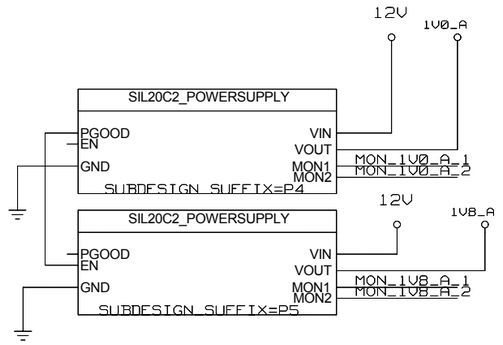
MON_2V5_1, MON_2V5_2

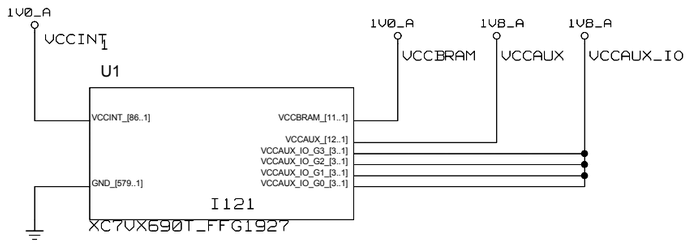
SMARTSYNC<5..0>

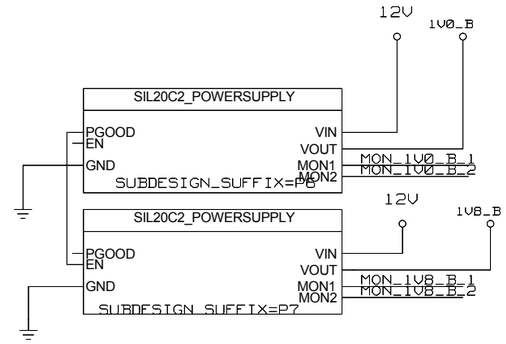
IN

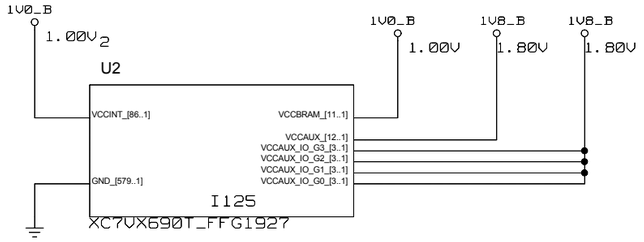
UNIVERSITY OF MAINZ	DRAWING TITLE: 12V POWERBUS		
BLOCK: POWERSUPPLY	SIZE: C	REV.: 02.06.2014	DRAWING NO.
	SCALE		SHEET OF

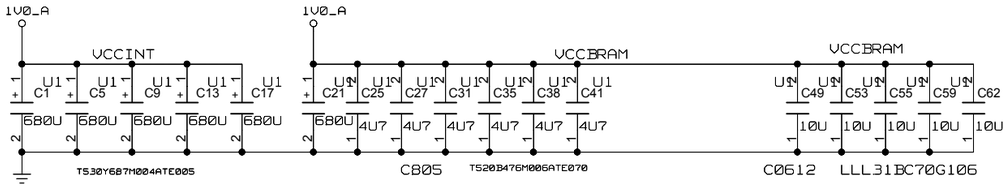
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

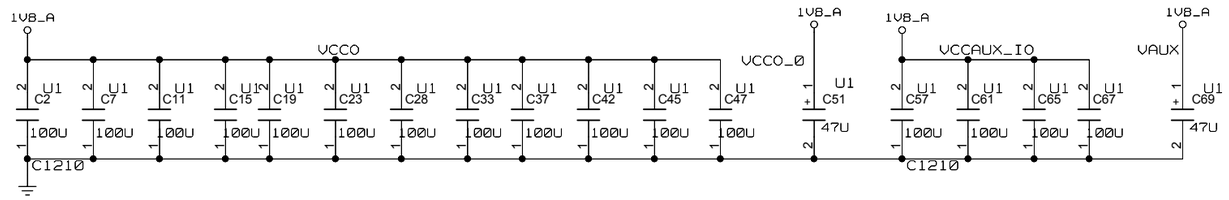


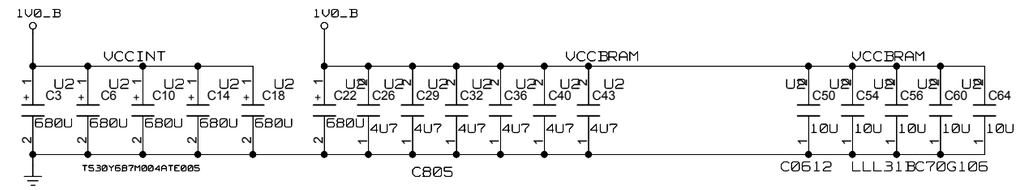


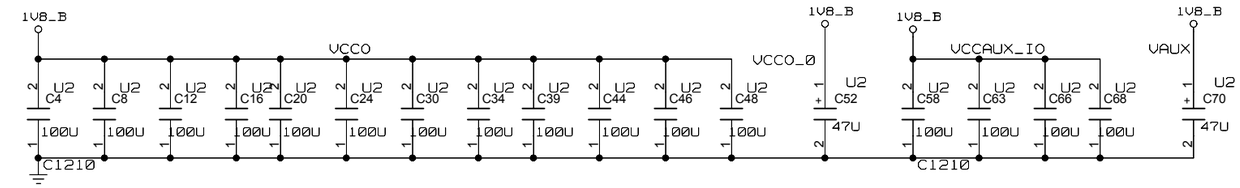






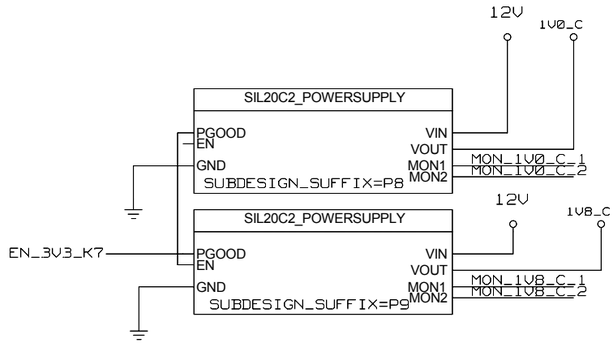


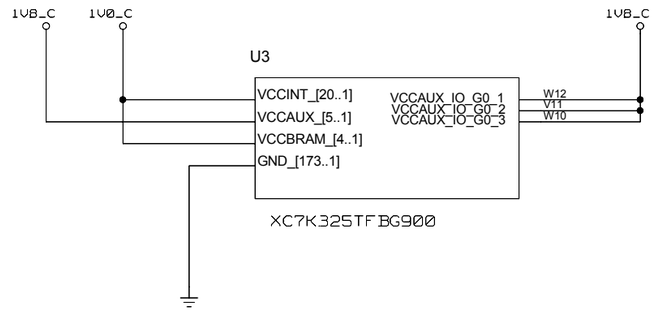


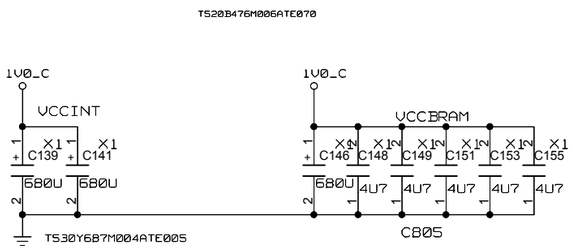


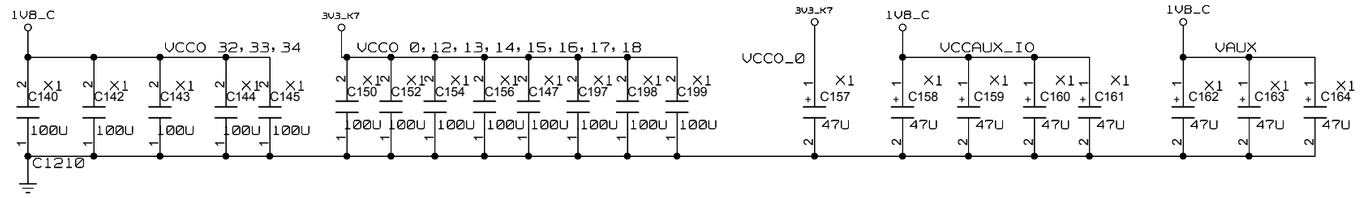
UNIVERSITY OF MAINZ		DRAWING TITLE: POWER VIRTEX7	
BLOCK: POWERSUPPLY		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.









UNIVERSITY OF MAINZ	DRAWING TITLE: POWER KINTEX7	
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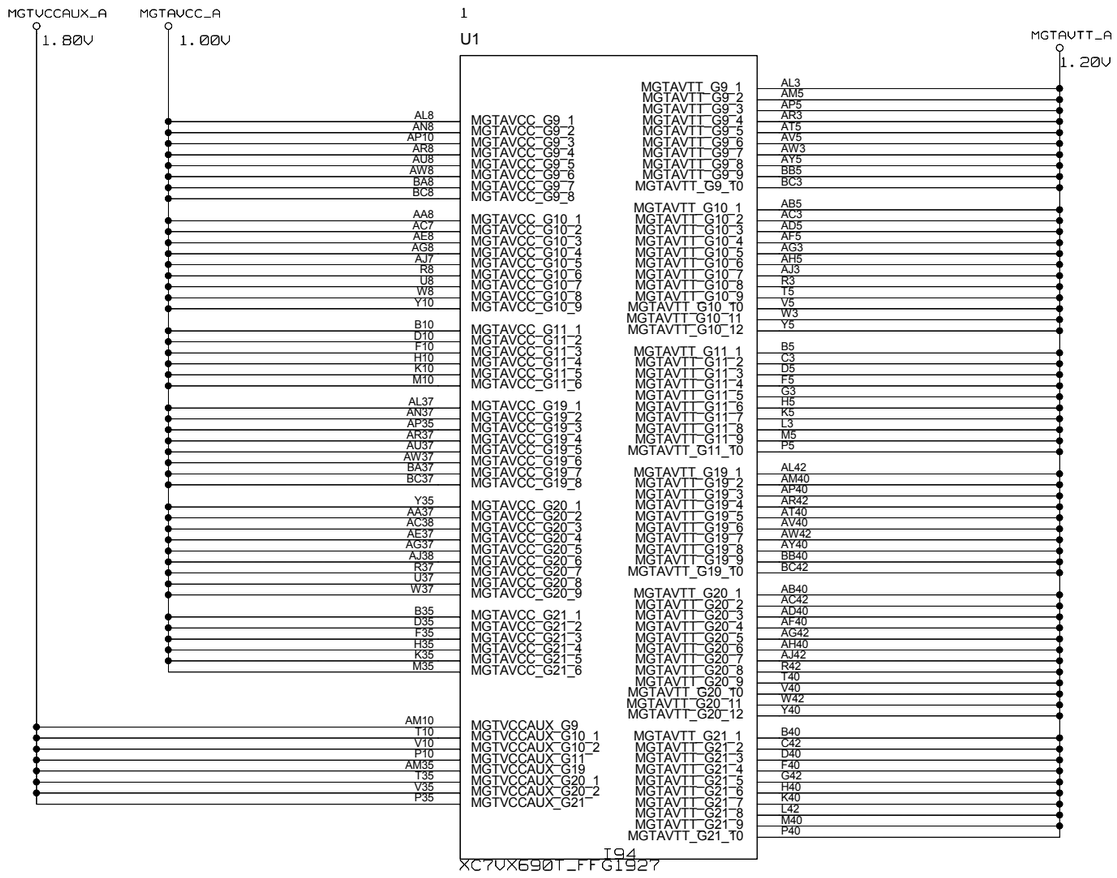
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: VIRTEX7 MGT POWER		
BLOCK: POWERSUPPLY	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

I2
MGTVCCAUX_B
1.80V

I3
MGTAVCC_B
1.00V

2
U2

I13
MGTAVTT_B
1.20V

AL8	MGTAVCC_G9_1	MGTAVTT_G9_1 AL3
AN8	MGTAVCC_G9_2	MGTAVTT_G9_2 AM5
AP10	MGTAVCC_G9_3	MGTAVTT_G9_3 AP5
AR8	MGTAVCC_G9_4	MGTAVTT_G9_4 AR3
AU8	MGTAVCC_G9_5	MGTAVTT_G9_5 AT5
AW8	MGTAVCC_G9_6	MGTAVTT_G9_6 AV5
BA8	MGTAVCC_G9_7	MGTAVTT_G9_7 AW3
BC8	MGTAVCC_G9_8	MGTAVTT_G9_8 AY5
		MGTAVTT_G9_9 BB5
		MGTAVTT_G9_T0 BC3
AA8	MGTAVCC_G10_1	MGTAVTT_G10_1 AB5
AC7	MGTAVCC_G10_2	MGTAVTT_G10_2 AC3
AE8	MGTAVCC_G10_3	MGTAVTT_G10_3 AD5
AG8	MGTAVCC_G10_4	MGTAVTT_G10_4 AF5
AJ7	MGTAVCC_G10_5	MGTAVTT_G10_5 AG3
R8	MGTAVCC_G10_6	MGTAVTT_G10_6 AH5
U8	MGTAVCC_G10_7	MGTAVTT_G10_7 AJ3
W8	MGTAVCC_G10_8	MGTAVTT_G10_8 R3
Y10	MGTAVCC_G10_9	MGTAVTT_G10_9 T5
		MGTAVTT_G10_T0 V5
		MGTAVTT_G10_11 W3
		MGTAVTT_G10_12 Y5
B10	MGTAVCC_G11_1	MGTAVTT_G11_1 B5
D10	MGTAVCC_G11_2	MGTAVTT_G11_2 C3
F10	MGTAVCC_G11_3	MGTAVTT_G11_3 D5
H10	MGTAVCC_G11_4	MGTAVTT_G11_4 F5
K10	MGTAVCC_G11_5	MGTAVTT_G11_5 G3
M10	MGTAVCC_G11_6	MGTAVTT_G11_6 H5
		MGTAVTT_G11_7 K5
		MGTAVTT_G11_8 L3
		MGTAVTT_G11_9 M5
		MGTAVTT_G11_T0 P5
AL37	MGTAVCC_G19_1	MGTAVTT_G19_1 AL42
AN37	MGTAVCC_G19_2	MGTAVTT_G19_2 AM40
AP35	MGTAVCC_G19_3	MGTAVTT_G19_3 AP40
AR37	MGTAVCC_G19_4	MGTAVTT_G19_4 AR42
AU37	MGTAVCC_G19_5	MGTAVTT_G19_5 AT40
AW37	MGTAVCC_G19_6	MGTAVTT_G19_6 AV40
BA37	MGTAVCC_G19_7	MGTAVTT_G19_7 AW42
BC37	MGTAVCC_G19_8	MGTAVTT_G19_8 AY40
		MGTAVTT_G19_9 BB40
		MGTAVTT_G19_T0 BC42
Y35	MGTAVCC_G20_1	MGTAVTT_G20_1 AB40
AA37	MGTAVCC_G20_2	MGTAVTT_G20_2 AC42
AC38	MGTAVCC_G20_3	MGTAVTT_G20_3 AD40
AE37	MGTAVCC_G20_4	MGTAVTT_G20_4 AF40
AG37	MGTAVCC_G20_5	MGTAVTT_G20_5 AG42
AJ38	MGTAVCC_G20_6	MGTAVTT_G20_6 AH40
R37	MGTAVCC_G20_7	MGTAVTT_G20_7 AJ42
U37	MGTAVCC_G20_8	MGTAVTT_G20_8 R42
W37	MGTAVCC_G20_9	MGTAVTT_G20_9 T40
		MGTAVTT_G20_T0 V40
		MGTAVTT_G20_11 W42
		MGTAVTT_G20_12 Y40
B35	MGTAVCC_G21_1	MGTAVTT_G21_1 B40
D35	MGTAVCC_G21_2	MGTAVTT_G21_2 C42
F35	MGTAVCC_G21_3	MGTAVTT_G21_3 D40
H35	MGTAVCC_G21_4	MGTAVTT_G21_4 F40
K35	MGTAVCC_G21_5	MGTAVTT_G21_5 G42
M35	MGTAVCC_G21_6	MGTAVTT_G21_6 H40
		MGTAVTT_G21_7 K40
		MGTAVTT_G21_8 L42
		MGTAVTT_G21_9 M40
		MGTAVTT_G21_T0 P40
AM10	MGTVCCAUX_G9	
T10	MGTVCCAUX_G10_1	
V10	MGTVCCAUX_G10_2	
P10	MGTVCCAUX_G11	
AM35	MGTVCCAUX_G19	
T35	MGTVCCAUX_G20_1	
V35	MGTVCCAUX_G20_2	
P35	MGTVCCAUX_G21	

I1C
XC7VX690T_FFG1927

SMARTSYNC<5..0>

1V0
MGTAVCC_B 12V

PTH08T220W_POWERSUPPLY
VIN
VOUT
MON1
MON2
GND
SMARTSYNC
SUBDESIGN_SUFFIX=P12

MON_MGTAVCC_B_1
MON_MGTAVCC_B_2

1V2
MGTAVTT_B

PTH08T240W_POWERSUPPLY
VIN
VOUT
MON1
MON2
GND
SMARTSYNC
SUBDESIGN_SUFFIX=P13

MON_MGTAVTT_B_1
MON_MGTAVTT_B_2

3V3
U108
LP38692
IN
EN
OUT
GND
1V8
1V8/0.3A
MGTVCCAUX_B
C725 10U
C726 4.7U X5R

LP38692MP_1.8NOPBCT

MGTVCCAUX_B
C101 C102 C103 C104 C105 C106
4U7
C805

MGTAVCC_B
C107 C108 C109 C110 C111 C112
4U7
C805

MGTAVTT_B
C113 C114 C115 C116 C117 C118
4U7
C805

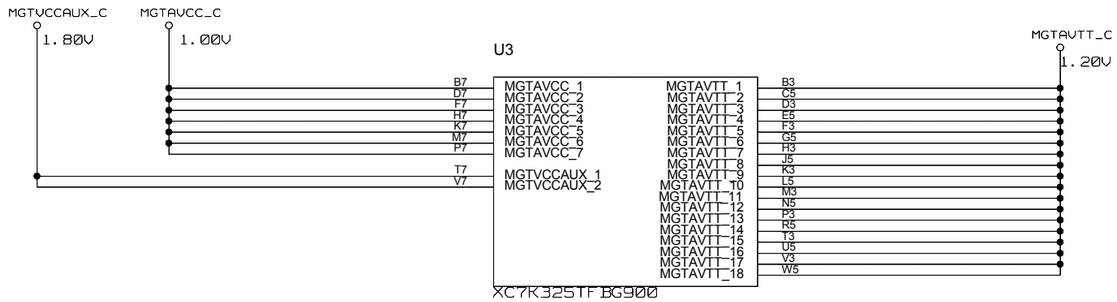
UNIVERSITY OF MAINZ

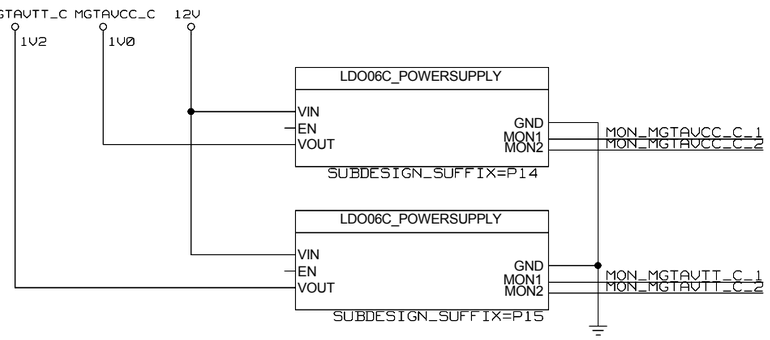
BLOCK: POWERSUPPLY

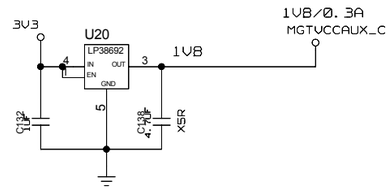
DRAWING TITLE
VIRTEX7 MGT POWER

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







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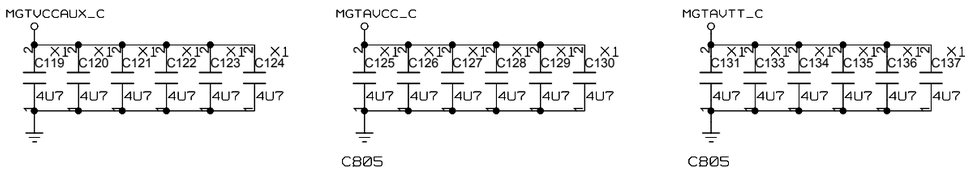
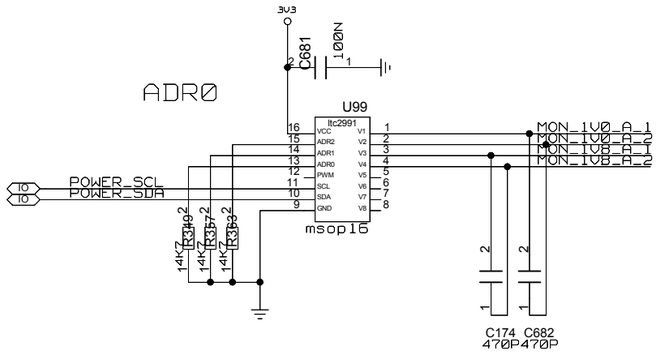


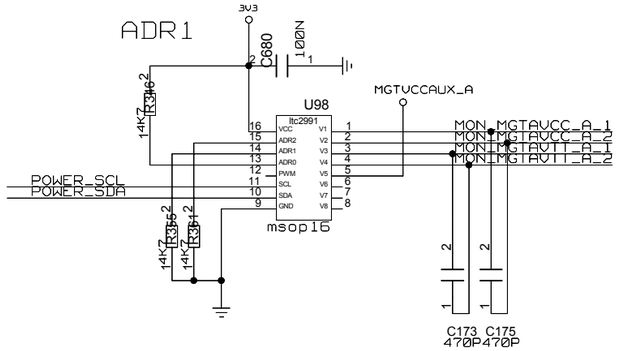
UNIVERSITY OF MAINZ	DRAWING TITLE: KINTEX7 MGT POWER	
BLOCK: POWERSUPPLY	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

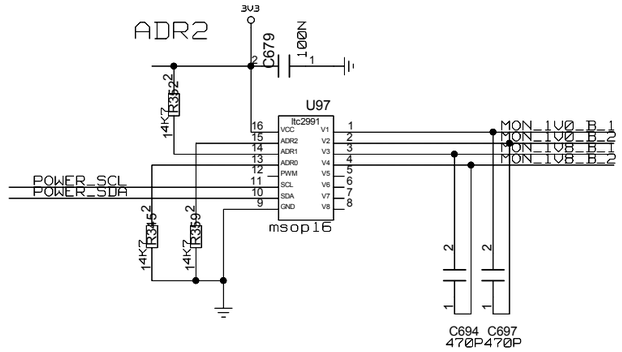
U1 CORE POWER MONITOR



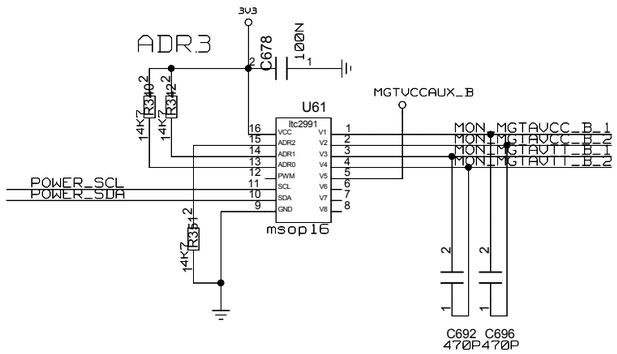
U1 MGT POWER MONITOR



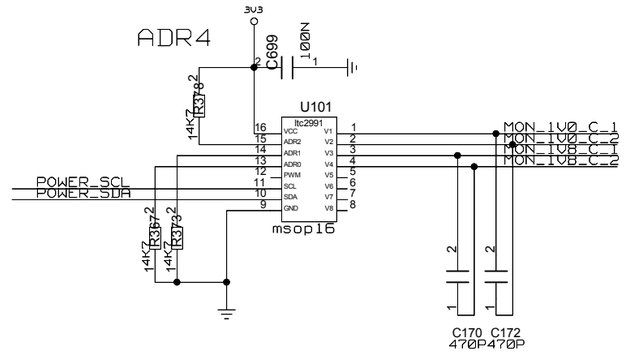
U2 CORE POWER MONITOR



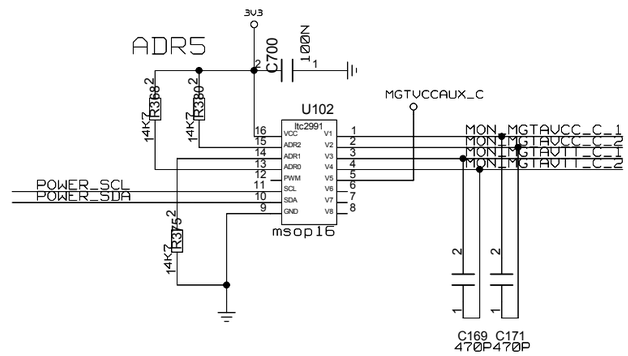
U2 MGT POWER MONITOR



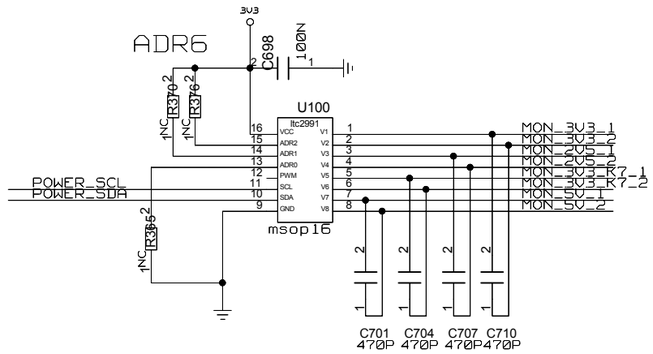
U3 CORE POWER MONITOR



U3 MGT POWER MONITOR

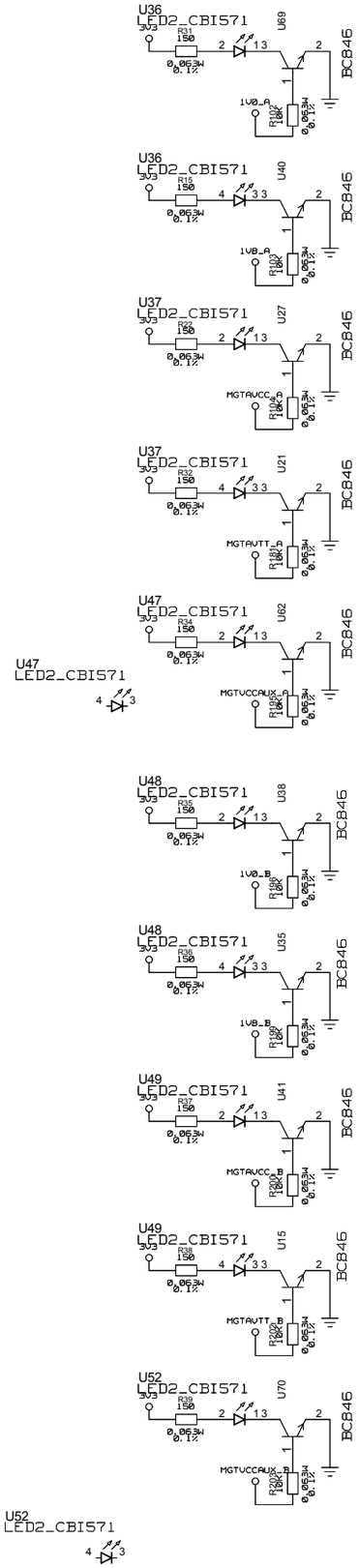


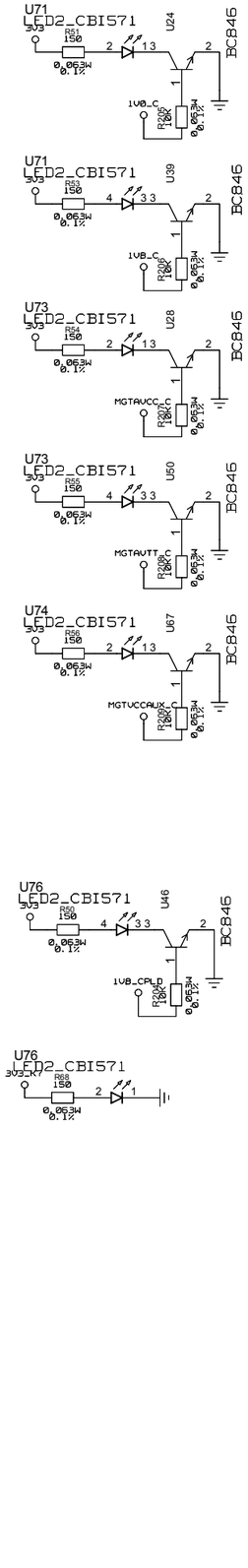
2V5, 3V3 POWER MONITOR

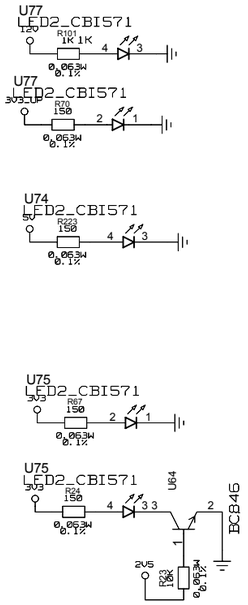


UNIVERSITY OF MAINZ	DRAWING TITLE: I2C POWERSUPPLY MONITORING	
	SIZE: C	REV.: 26.05.2014
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







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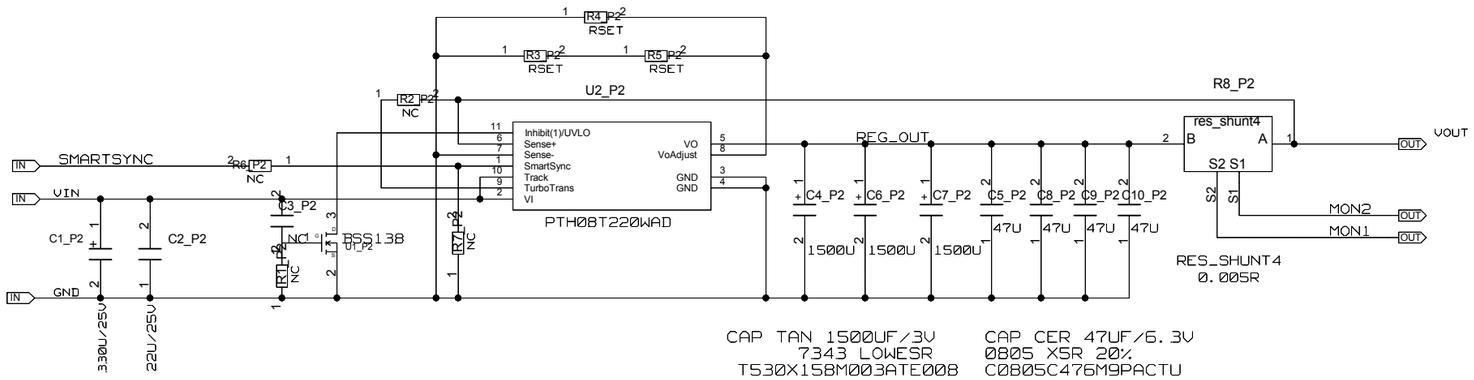
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CAP TAN 1500UF/3V
7343 LOWESR
T530X158M003ATE008

CAP CER 47UF/6.3V
0805 X5R 20%
C0805C476M9PACTU

CAP ALUM
330UF/25V 0810 SMD
EEE-HAE331UAP

CAP CER
22UF/25V 1210 Y5U
C3225Y5V1E226Z

$$R_{SET} = 10\ k\Omega \times \frac{0.69}{V_O - 0.69} - 1.43\ k\Omega$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard)	R_{SET} (Standard Value)	V_O (Actual)
5.0 V (1)	169 Ω	5.005 V
3.3 V	1.21 kΩ	3.304 V
2.5 V	2.37 kΩ	2.506 V
1.8 V	4.75 kΩ	1.807 V
1.5 V	6.98 kΩ	1.510 V
1.2 V (2)	12.1 kΩ	1.200 V
1.0 V (2)	20.5 kΩ	1.004 V
0.7 V (2)	681 kΩ	0.700 V

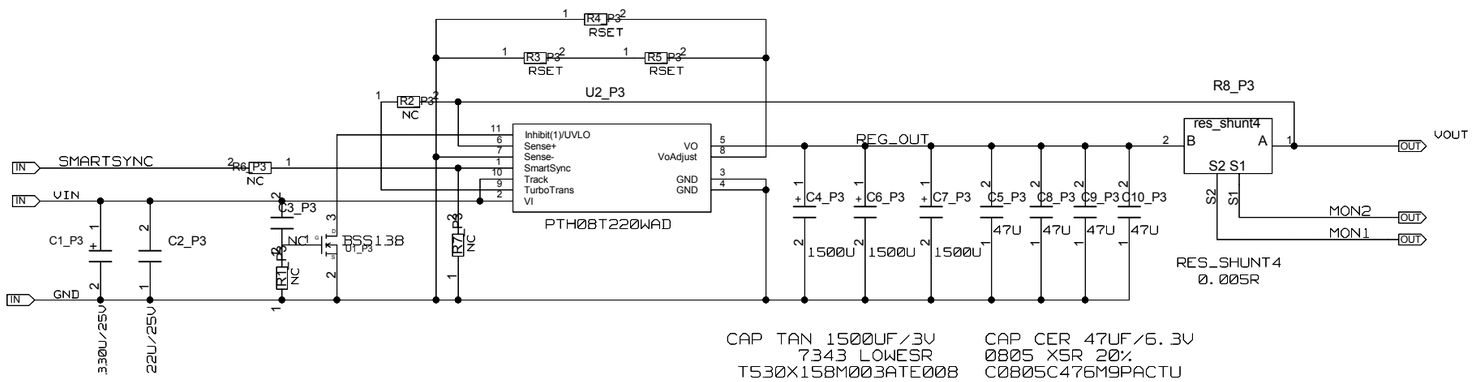
UNIVERSITY OF MAINZ

DRAWING TITLE: PTH08T220W_POWER SUPPLY

SIZE: C | REV. | DRAWING NO.

SCALE | SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CAP ALUM
330UF/25V 0810 SMD
EEE-HAE331UAP

CAP CER
22UF/25V 1210 Y5U
C3225Y5V1E226Z

CAP TAN 1500UF/3V
7343 LOWESR
T530X158M003ATE008

CAP CER 47UF/6.3V
0805 X5R 20%
C0805C476M9PACTU

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0.7 V (2)	681 kΩ	0.700 V

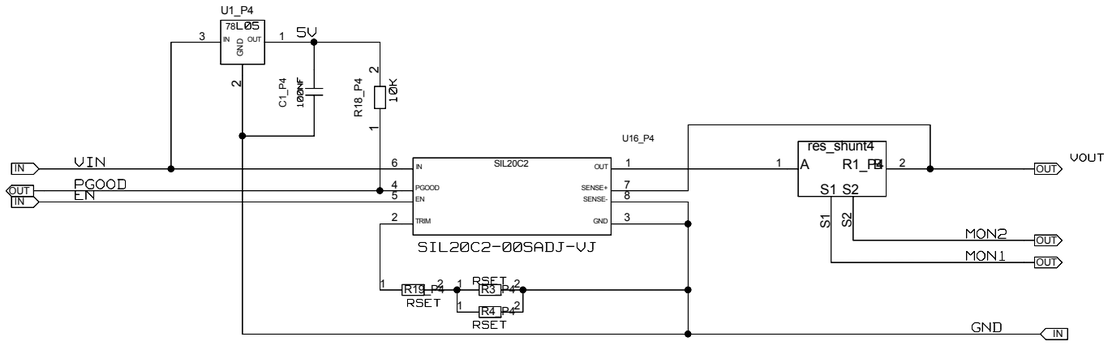
UNIVERSITY OF MAINZ

DRAWING TITLE: PTH08T220W_POWER SUPPLY

SIZE: C | REV. | DRAWING NO.

SCALE | SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

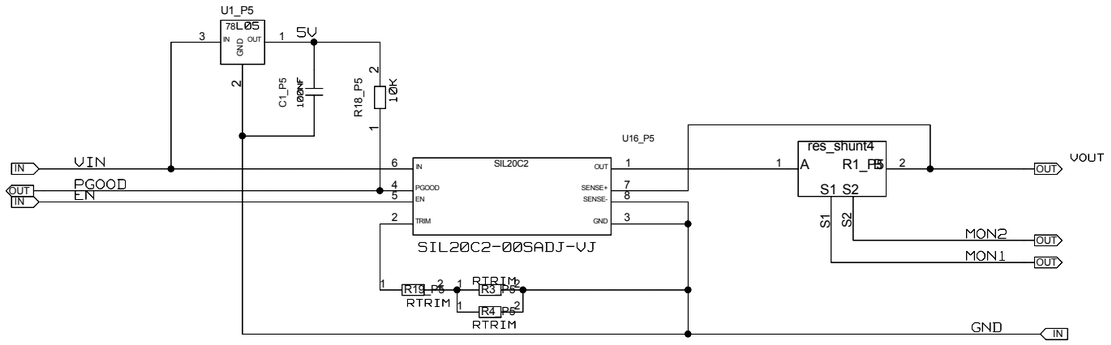


The resistor trim equation for the SIL20C2 is as follows:

$$Rtrim\ (k\Omega) = \frac{1.182}{(Vout - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



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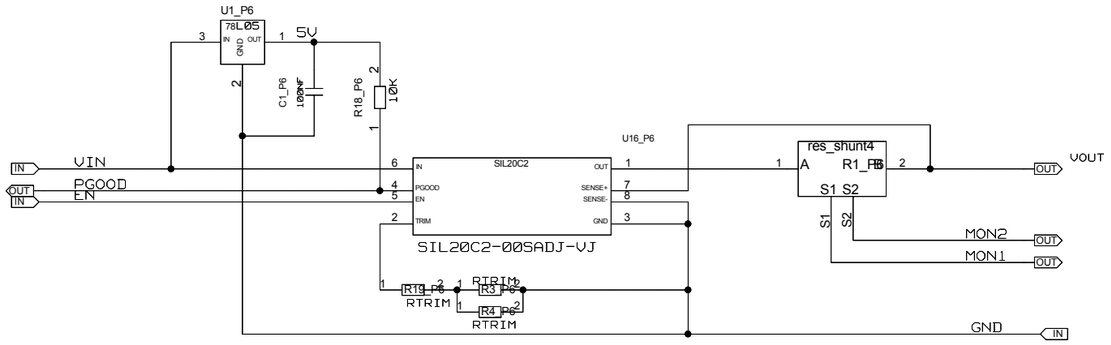
$$Rtrim\ (k\Omega) = \frac{1.182}{(Vout - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



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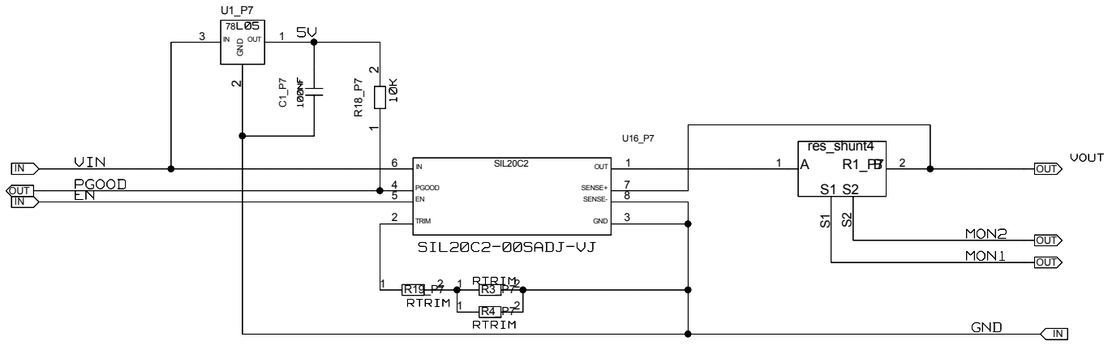
$$\text{Rtrim } (k\Omega) = \frac{1.182}{(\text{Vout} - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

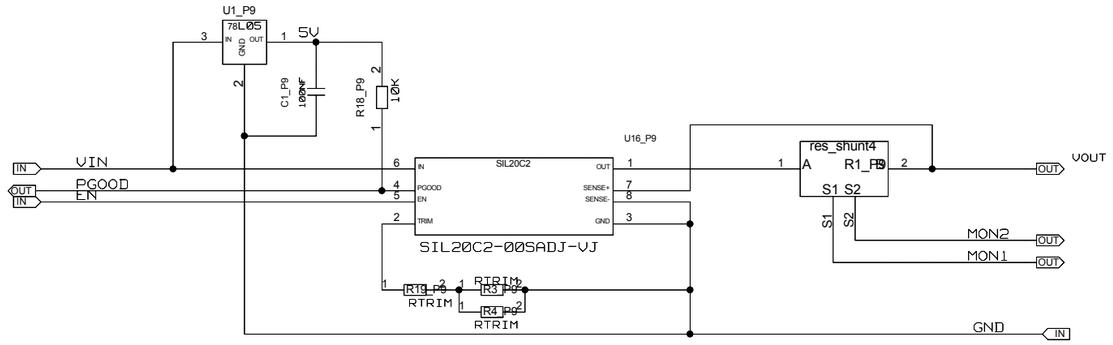


The resistor trim equation for the SIL20C2 is as follows:

$$\text{Rtrim } (k\Omega) = \frac{1.182}{(\text{Vout} - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

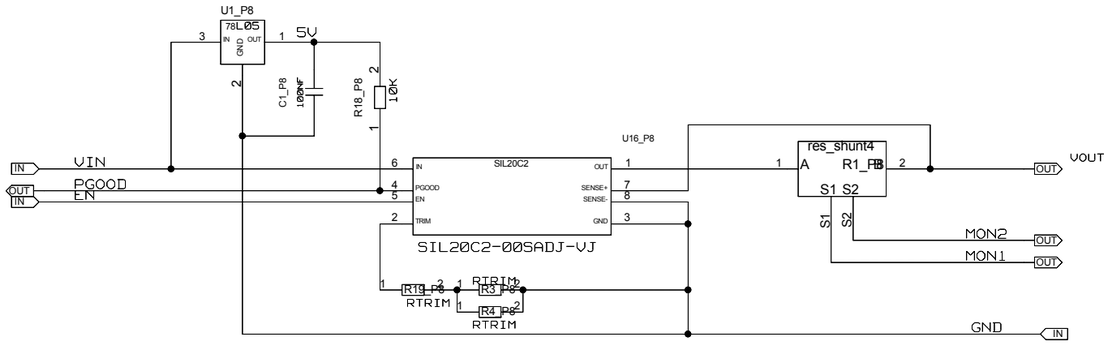


The resistor trim equation for the SIL20C2 is as follows:

$$Rtrim\ (k\Omega) = \frac{1.182}{(Vout - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

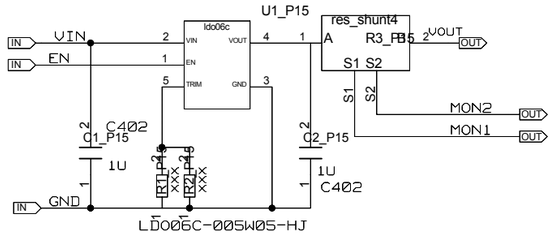


The resistor trim equation for the SIL20C2 is as follows:

$$\text{Rtrim } (k\Omega) = \frac{1.182}{(\text{Vout} - 0.591)}$$

UNIVERSITY OF MAINZ	DRAWING TITLE: SIL20C2_POWERSUPPLY		
	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

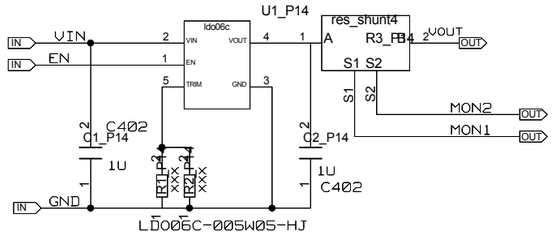
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



RTRIM(K)=1.182/(VOUT-0.591)

UNIVERSITY OF MAINZ	DRAWING TITLE: LD006C_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

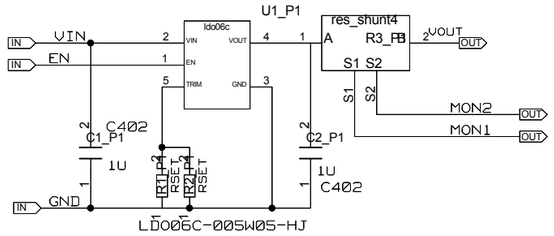
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



RTRIM(K)=1.182/(VOUT-0.591)

UNIVERSITY OF MAINZ	DRAWING TITLE: LD006C_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

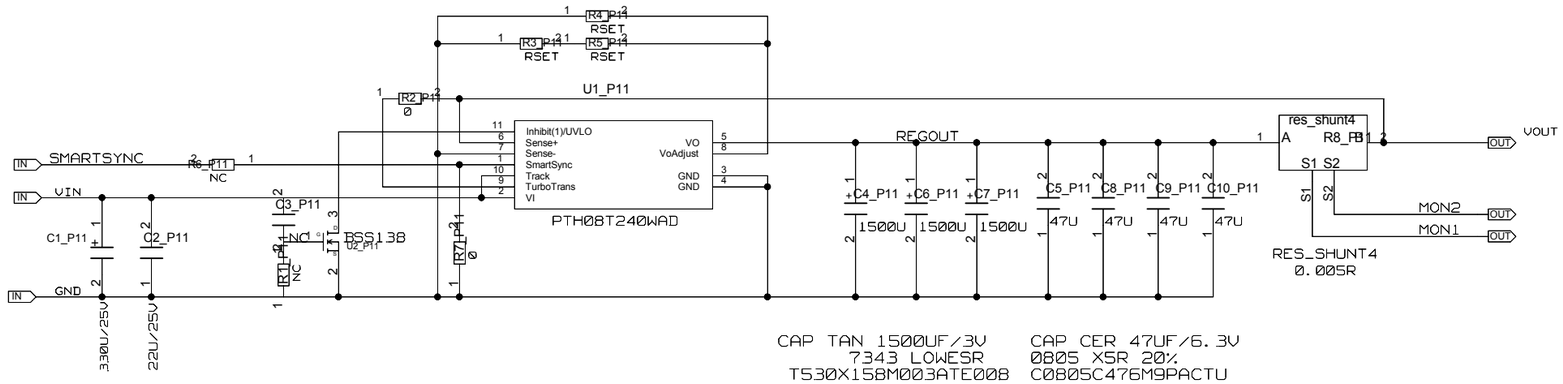
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



$$RTRIM(K) = 1.182 / (VOUT - 0.591)$$

UNIVERSITY OF MAINZ	DRAWING TITLE: LD006C_POWERSUPPLY		
	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CAP ALUM
330UF/25V 0810 SMD
EEE-HAE331UAP

CAP CER
22UF/25V 1210 Y5U
C3225Y5V1E226Z

CAP TAN 1500UF/3V
7343 LOWESR
T530X158M003ATE008

CAP CER 47UF/6.3V
0805 X5R 20%
C0805C476M9PACTU

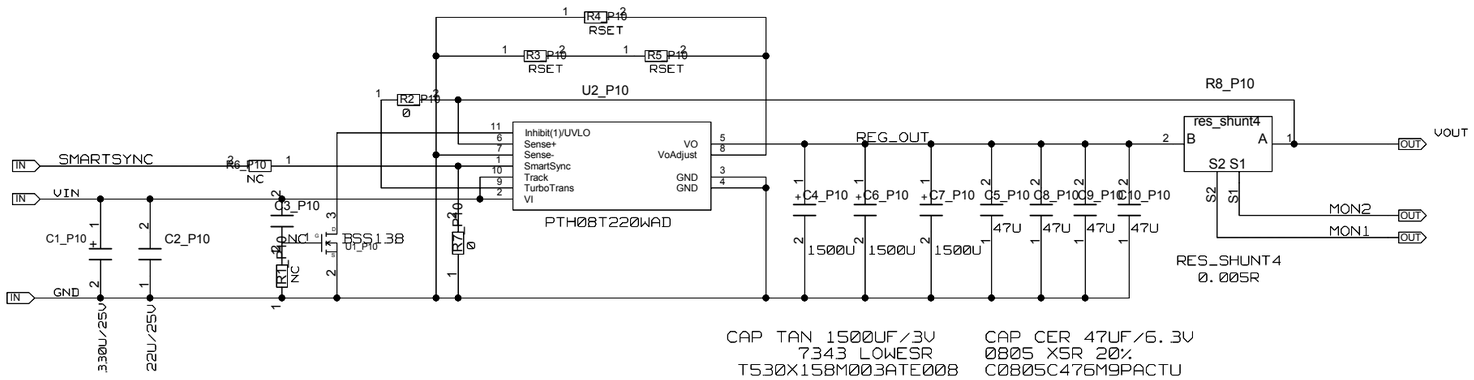
Table 2. Output Voltage Set-Point Resistor Values (Standard Values)

V_O Required (V)	R_{SET} (kΩ)	V_O Required (V)	R_{SET} (Ω)
0.70 (1)	681	2.50	2.37 k
0.75 (1)	113	2.60	2.15 k
0.80 (1)	61.9	2.70	2.00 k
0.85 (1)	41.2	2.80	1.82 k
0.90 (1)	31.6	2.90	1.69 k
0.95 (1)	24.9	3.00	1.54 k
1.00 (1)	20.5	3.10	1.43 k
1.05 (1)	17.8	3.20	1.33 k
1.10 (1)	15.4	3.30	1.21 k
1.15 (1)	13.3	3.40	1.10 k
1.20 (1)	12.1	3.50	1.02 k
1.25	10.7	3.60	931
1.30	9.88	3.70 (2)	866
1.35	9.09	3.80 (2)	767
1.40	8.25	3.90 (2)	715
1.45	7.68	4.00 (2)	649
1.50	6.98	4.10 (2)	590
1.55	6.49	4.20 (2)	536
1.60	6.04	4.30 (2)	475
1.65	5.76	4.40 (2)	432
1.70	5.36	4.50 (2)	383
1.75	5.11	4.60 (2)	332
1.80	4.75	4.70 (2)	287
1.85	4.53	4.80 (2)	249
1.90	4.22	4.90 (2)	210
1.95	4.02	5.00 (2)	169
2.00	3.83	5.10 (2)	133
2.10	3.40	5.20 (2)	100
2.20	3.09	5.30 (2)	66.5
2.30	2.67	5.40 (2)	34.8
2.40	2.61	5.50 (2)	4.99

(1) For output voltages ≤ 1.2V, at nominal operating frequency, the output ripple may increase (typically 2×) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature, review the SmartSync application section for further guidance.
(2) For V_O > 3.6 V, the minimum input voltage is (V_O + 2) V.

UNIVERSITY OF MAINZ	DRAWING TITLE: PTH08T240W_POWERSUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



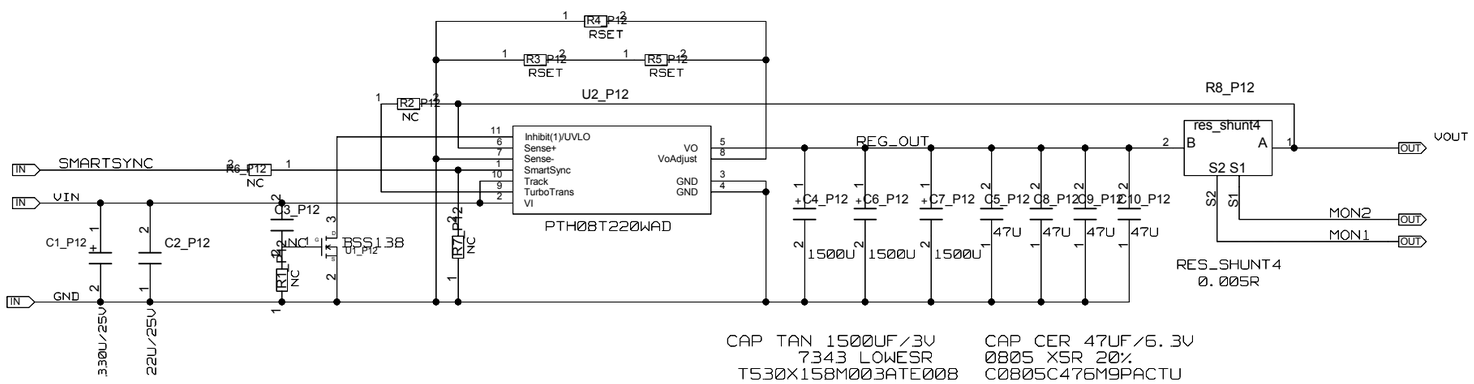
$$R_{SET} = 10\ k\Omega \times \frac{0.69}{V_O - 0.69} - 1.43\ k\Omega$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard)	R_{SET} (Standard Value)	V_O (Actual)
5.0 V (1)	169 Ω	5.005 V
3.3 V	1.21 kΩ	3.304 V
2.5 V	2.37 kΩ	2.506 V
1.8 V	4.75 kΩ	1.807 V
1.5 V	6.98 kΩ	1.510 V
1.2 V (2)	12.1 kΩ	1.200 V
1.0 V (2)	20.5 kΩ	1.004 V
0.7 V (2)	681 kΩ	0.700 V

UNIVERSITY OF MAINZ	DRAWING TITLE: PTH08T220W_POWER SUPPLY	
	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CAP TAN 1500UF/3V
7343 LOWESR
T530X158M003ATE008

CAP CER 47UF/6.3V
0805 X5R 20%
C0805C476M9PACTU

CAP ALUM
330UF/25V 0810 SMD
EEE-HAE331UAP

CAP CER
22UF/25V 1210 Y5U
C3225Y5V1E226Z

$$R_{SET} = 10\ k\Omega \times \frac{0.69}{V_O - 0.69} - 1.43\ k\Omega$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard)	R_{SET} (Standard Value)	V_O (Actual)
5.0 V (1)	169 Ω	5.005 V
3.3 V	1.21 kΩ	3.304 V
2.5 V	2.37 kΩ	2.506 V
1.8 V	4.75 kΩ	1.807 V
1.5 V	6.98 kΩ	1.510 V
1.2 V (2)	12.1 kΩ	1.200 V
1.0 V (2)	20.5 kΩ	1.004 V
0.7 V (2)	681 kΩ	0.700 V

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DRAWING TITLE: PTH08T220W_POWER SUPPLY

SIZE: C | REV. | DRAWING NO.

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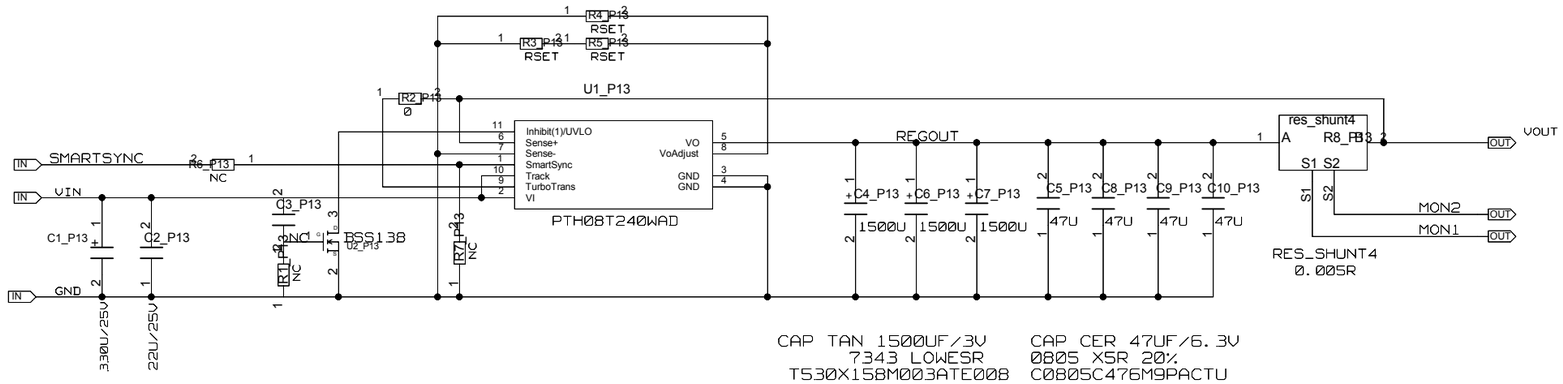

CAP ALUM
330UF/25V 0810 SMD
EEE-HAE331UAP

CAP CER
22UF/25V 1210 Y5U
C3225Y5V1E226Z

CAP TAN 1500UF/3V
7343 LOWESR
T530X158M003ATE008

CAP CER 47UF/6.3V
0805 X5R 20%
C0805C476M9PACTU

Table 2. Output Voltage Set-Point Resistor Values (Standard Values)

V_O Required (V)	R_{SET} (kΩ)	V_O Required (V)	R_{SET} (Ω)
0.70 (1)	681	2.50	2.37 k
0.75 (1)	113	2.60	2.15 k
0.80 (1)	61.9	2.70	2.00 k
0.85 (1)	41.2	2.80	1.82 k
0.90 (1)	31.6	2.90	1.69 k
0.95 (1)	24.9	3.00	1.54 k
1.00 (1)	20.5	3.10	1.43 k
1.05 (1)	17.8	3.20	1.33 k
1.10 (1)	15.4	3.30	1.21 k
1.15 (1)	13.3	3.40	1.10 k
1.20 (1)	12.1	3.50	1.02 k
1.25	10.7	3.60	931
1.30	9.88	3.70 (2)	866
1.35	9.09	3.80 (2)	767
1.40	8.25	3.90 (2)	715
1.45	7.68	4.00 (2)	649
1.50	6.98	4.10 (2)	590
1.55	6.49	4.20 (2)	536
1.60	6.04	4.30 (2)	475
1.65	5.76	4.40 (2)	432
1.70	5.36	4.50 (2)	383
1.75	5.11	4.60 (2)	332
1.80	4.75	4.70 (2)	287
1.85	4.53	4.80 (2)	249
1.90	4.22	4.90 (2)	210
1.95	4.02	5.00 (2)	169
2.00	3.83	5.10 (2)	133
2.10	3.40	5.20 (2)	100
2.20	3.09	5.30 (2)	66.5
2.30	2.67	5.40 (2)	34.8
2.40	2.61	5.50 (2)	4.99

(1) For output voltages ≤ 1.2V, at nominal operating frequency, the output ripple may increase (typically 2×) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature, review the SmartSync application section for further guidance.
(2) For V_O > 3.6 V, the minimum input voltage is (V_O + 2) V.

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	SIZE: C	REV. / DRAWING NO.
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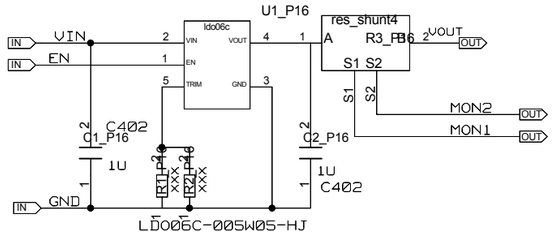
ZONE	LTR	DESCRIPTION	DATE	APPR.



RTRIM(K)=1.182/(VOUT-0.591)

UNIVERSITY OF MAINZ	DRAWING TITLE: LD006C_POWERSUPPLY		
	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

TTC CLOCK MGT1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

EXTENSION MODUL

CLOCK_LVPECL_SI591_AC — U4_39 — CLK_P, CLK_N

CLK_MGT1_P, CLK_MGT1_N

CLOCK_CML_FANOUT6_DC — U52_20 — SY58034U_DC_CML
CLK1_IN_P, CLK1_IN_N, CLK2_IN_P, CLK2_IN_N, SEL
CLK_OUT_P<5..0>, CLK_OUT_N<5..0>

MGT1_OSC_P<5..0>
MGT1_OSC_N<5..0>
CML DC

CLKIN=LVPECL_AC
R1=NC C1=10NF
R2=NC C2=10NF
R3=0 R4=0

MUX_CML_4X2_DC — U1_25 — SY56028XR_DC_CML
CLK1_IN_P, CLK1_IN_N, CLK2_IN_P, CLK2_IN_N, CLK3_IN_P, CLK3_IN_N, CLK4_IN_P, CLK4_IN_N, SEL0, SEL1
CLK_OUT_P_1, CLK_OUT_N_1, CLK_OUT_P_2, CLK_OUT_N_2

MGT1_OSC_P<0>
MGT1_OSC_N<0>
EXT_CLK_P<1>
EXT_CLK_N<1>
MUX_SEL<0>
MUX_SEL<1>

---> EXT CLOCK

R201 100 — U30, U42 (MMCX)

CLK1IN=CML_DC
CLK2IN=CML_AC
CLK3IN=CML_AC
CLK4IN=NC
R3=NC C1=NC
R4=NC C2=100NF
R5=NC C3=100NF
R6=NC C4=NC

CLOCK_CML_FANOUT6_DC — U52_19 — SY58034U_DC_CML
CLK1_IN_P, CLK1_IN_N, CLK2_IN_P, CLK2_IN_N, SEL
CLK_OUT_P<5..0>, CLK_OUT_N<5..0>

MGT1_1_CLK_P<5..0>
MGT1_1_CLK_N<5..0>

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLOCK_CML_FANOUT6_AC — U52_5 — A LEFT
MGT1_CLK_P<6..1>
MGT1_CLK_N<6..1>

CLOCK_CML_FANOUT6_AC — U52_6 — B RIGHT
MGT1_CLK_P<12..7>
MGT1_CLK_N<12..7>

CLOCK_CML_FANOUT6_AC — U52_7 — C LEFT
MGT1_CLK_P<18..13>
MGT1_CLK_N<18..13>

CLOCK_CML_FANOUT6_AC — U52_8 — D RIGHT
MGT1_CLK_P<24..19>
MGT1_CLK_N<24..19>

MGT1_CLK_KINTEX U3

C453 100NF — MGT1_CLK_P<25>
C454 100NF — MGT1_CLK_N<25>

MGT1_CLK_P<6..1>
MGT1_CLK_P<12..7>
MGT1_CLK_P<18..13>
MGT1_CLK_P<24..19>
MGT1_CLK_P<25>
→ MGT1_CLK_P<25..1> OUT

MGT1 CLOCK

MGT1_CLK_N<6..1>
MGT1_CLK_N<12..7>
MGT1_CLK_N<18..13>
MGT1_CLK_N<24..19>
MGT1_CLK_N<25>
→ MGT1_CLK_N<25..1> OUT

TTC_CLK<0> = JITTERCLEANER
TTC_CLK<1> = GCK
TTC_CLK<2> = EXTENSION_MODUL
TTC_CLK<3> = MMCX_SPARE

TTC_OPTO_IN — TTC_P, TTC_N, DETECT
TTC_IN_P, TTC_IN_N

TTC — IN_P, IN_N, TTC_CTRL<56..0>
TTC_CLK_P<0>, TTC_CLK_N<0>, TTC_CLK_P<3..1>, TTC_CLK_N<3..1>

LVDS

JITTERCLEANER_SI5326 — U54 — CML AC
DIFF1_P, DIFF1_N, DIFF2_P, DIFF2_N, CTRL<12..0>
DIFF1OUT_P, DIFF1OUT_N, DIFF2OUT_P, DIFF2OUT_N

TTC_CLK_P<0>, TTC_CLK_N<0>
JC_OUT2_P, JC_OUT2_N

TTC_DETECT (OUT)
TTC_CTRL<55..0> (IO)
JC_CTRL<12..0> (IO)

EXT_CLK_P<0>
EXT_CLK_N<0>

---> EXT_TTC_INPUT

TTC_CLK_P<3> — U31
TTC_CLK_N<3> — U43

<---EXT_GCK_CLOCK

EXT_CLK_P<5> — R204 NC
EXT_CLK_N<5> — R210 NC

TTC_CLK_P<3..1>
TTC_CLK_N<3..1>
→ TO GCK

EXT_CLK_P/N 0 JT
EXT_CLK_P/N 1 MGT1
EXT_CLK_P/N 2 MGT2
EXT_CLK_P/N 3 MGT3
EXT_CLK_P/N 4 MGT4
EXT_CLK_P/N 5 TTC OUT
EXT_CLK_P/N 6 GCK1

EXT_CLK_P<6..0> (IO)
EXT_CLK_N<6..0> (IO)
MUX_SEL<9..0> (IN)

UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ		DRAWING TITLE: MGT1 CLOCK CML	
BLOCK: CLOCK		SIZE: C	REV.: 27.05.2014
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		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

MGT2 CLOCK

EXTENSION MODUL

---> EXT CLOCK

160,3148 MHZ

CLOCK_LVPECL_SI591_AC
U4_38
CLK_P
CLK_N
CLK_MGT2_P
CLK_MGT2_N

CLOCK_CML_FANOUT6_DC
U52_18
SY58034U_DC_CML
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK_OUT_P<5..0>
CLK_OUT_N<5..0>
SEL
MGT2_OSC_P<5..0>
MGT2_OSC_N<5..0>

CLKIN=LVPECL_AC
R1=NC C1=10NF
R2=NC C2=10NF
R3=0 R4=0

MUX_CML_4X2_DC
U1_23
SY56028XR_DC_CML
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK3_IN_P
CLK3_IN_N
CLK4_IN_P
CLK4_IN_N
CLK_OUT_P_1
CLK_OUT_N_1
CLK_OUT_P_2
CLK_OUT_N_2
SEL0
SEL1
MGT2_OSC_P<0>
MGT2_OSC_N<0>
EXT_CLK_P<2>
EXT_CLK_N<2>
MUX_SEL<2>
MUX_SEL<3>

R21 100
U22
U23

CLK1IN=CML_DC
CLK2IN=CML_AC
CLK3IN=NC
CLK4IN=NC
R3=NC C1=NC
R4=NC C2=100NF
R5=NC C3=NC
R6=NC C4=NC

CLOCK_CML_FANOUT6_DC
U52_17
SY58034U_DC_CML
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK_OUT_P<5..0>
CLK_OUT_N<5..0>
SEL
MGT2_1_CLK_P<5..0>
MGT2_1_CLK_N<5..0>

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLOCK_CML_FANOUT6_AC
U52_1
SY58034U_DC_CML
A LEFT
MGT2_CLK_P<6..1>
MGT2_CLK_N<6..1>

CLOCK_CML_FANOUT6_AC
U52_2
SY58034U_DC_CML
B RIGHT
MGT2_CLK_P<12..7>
MGT2_CLK_N<12..7>

CLOCK_CML_FANOUT6_AC
U52_3
SY58034U_DC_CML
C LEFT
MGT2_CLK_P<18..13>
MGT2_CLK_N<18..13>

CLOCK_CML_FANOUT6_AC
U52_4
SY58034U_DC_CML
D RIGHT
MGT2_CLK_P<24..19>
MGT2_CLK_N<24..19>

MGT2_CLK_KINTEX U3

C458 100NF
C459 100NF
MGT2_CLK_P<25>
MGT2_CLK_N<25>

MGT2_CLK_P<6..1>
MGT2_CLK_P<12..7>
MGT2_CLK_P<18..13>
MGT2_CLK_P<24..19>
MGT2_CLK_P<25>
MGT2_CLK_P<25..1> OUT

MGT2 CLOCK

MGT2_CLK_N<6..1>
MGT2_CLK_N<12..7>
MGT2_CLK_N<18..13>
MGT2_CLK_N<24..19>
MGT2_CLK_N<25>
MGT2_CLK_N<25..1> OUT

UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ		DRAWING TITLE: MGT2 CLOCK CML	
BLOCK: CLOCK		SIZE: C	REV.: 27.05.2014
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ZONE	LTR	DESCRIPTION	DATE	APPR.

MGT3 CLOCK

EXTENSION MODUL

CLOCK_LVPECL_SI591_AC
U4_40
CLK_P
CLK_N
CLK_MGT3_P
CLK_MGT3_N

MUX_CML_4X2_DC
U1_26
SY56028XR_DC_CML
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK3_IN_P
CLK3_IN_N
CLK4_IN_P
CLK4_IN_N
CLK_OUT_P_1
CLK_OUT_N_1
CLK_OUT_P_2
CLK_OUT_N_2
SEL0
SEL1
MGT1_OSC_P<1>
MGT1_OSC_N<1>
EXT_CLK_P<3>
EXT_CLK_N<3>
JC_OUT2_P
JC_OUT2_N
MUX_SEL<4>
MUX_SEL<5>
R21
100
U33
U45

CLK1IN=LVPECL_AC
CLK2IN=CML_DC
CLK3IN=CML_AC
CLK4IN=CML_AC
R3=NC C1=100NF
R4=NC C2=NC
R5=NC C3=100NF
R6=NC C4=100NF

CLOCK_CML_FANOUT6_DC
U52_21
SY58034U_DC_CML
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK_OUT_P<5..0>
CLK_OUT_N<5..0>
SEL
MGT3_1_CLK_P<5..0>
MGT3_1_CLK_N<5..0>

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLOCK_CML_FANOUT6_AC
U52_9
A LEFT
MGT3_CLK_P<6..1>
MGT3_CLK_N<6..1>

CLOCK_CML_FANOUT6_AC
U52_10
B RIGHT
MGT3_CLK_P<12..7>
MGT3_CLK_N<12..7>

CLOCK_CML_FANOUT6_AC
U52_11
C LEFT
MGT3_CLK_P<18..13>
MGT3_CLK_N<18..13>

CLOCK_CML_FANOUT6_AC
U52_12
D RIGHT
MGT3_CLK_P<24..19>
MGT3_CLK_N<24..19>

MGT3_CLK_P<6..1>
MGT3_CLK_P<12..7>
MGT3_CLK_P<18..13>
MGT3_CLK_P<24..19>
MGT3_CLK_P<24..1>
OUT

MGT3 CLOCK

MGT3_CLK_N<6..1>
MGT3_CLK_N<12..7>
MGT3_CLK_N<18..13>
MGT3_CLK_N<24..19>
MGT3_CLK_N<24..1>
OUT

UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ		DRAWING TITLE: MGT3 CLOCK CML	
BLOCK: CLOCK		SIZE: C	REV.: 27.05.2014
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ZONE	LTR	DESCRIPTION	DATE	APPR.

MGT4 CLOCK

EXTENSION MODUL

40,0787 MHZ

CLOCK_LVPECL_SI591_AC
U4_41
CLK_P
CLK_N
CLK_MGT4_P
CLK_MGT4_N

---> EXT CLOCK

EXT_CLK_P<4>
EXT_CLK_N<4>
MGT2_OSC_P<1>
MGT2_OSC_N<1>

MUX_CML_4X2_DC
U1_27
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK3_IN_P
CLK3_IN_N
CLK4_IN_P
CLK4_IN_N
CLK_OUT_P_1
CLK_OUT_N_1
CLK_OUT_P_2
CLK_OUT_N_2
SEL0
SEL1
SY56028XR_DC_CML

R21 100
U32
U44

MUX_SEL<6>
MUX_SEL<7>

CLK1IN=LVPECL_AC
CLK2IN=CML_AC
CLK3IN=CML_DC
CLK4IN=NC
R3=NC C1=100NF
R4=NC C2=100NF
R5=NC C3=NC
R6=NC C4=NC

CLOCK_CML_FANOUT6_DC
U52_22
CLK1_IN_P
CLK1_IN_N
CLK2_IN_P
CLK2_IN_N
CLK_OUT_P<5..0>
CLK_OUT_N<5..0>
SEL
SY58034U_DC_CML
MGT4_1_CLK_P<5..0>
MGT4_1_CLK_N<5..0>

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLKIN=CML
R1=NC C1=NC
R2=NC C2=NC
R3=NC R4=NC

CLOCK_CML_FANOUT6_AC
U52_13
A LEFT
MGT4_CLK_P<6..1>
MGT4_CLK_N<6..1>

CLOCK_CML_FANOUT6_AC
U52_14
B RIGHT
MGT4_CLK_P<12..7>
MGT4_CLK_N<12..7>

CLOCK_CML_FANOUT6_AC
U52_15
C LEFT
MGT4_CLK_P<18..13>
MGT4_CLK_N<18..13>

CLOCK_CML_FANOUT6_AC
U52_16
D RIGHT
MGT4_CLK_P<24..19>
MGT4_CLK_N<24..19>

MGT4_CLK_P<6..1>
MGT4_CLK_P<12..7>
MGT4_CLK_P<18..13>
MGT4_CLK_P<24..19>
MGT4_CLK_P<24..1>
OUT

MGT4 CLOCK

MGT4_CLK_N<6..1>
MGT4_CLK_N<12..7>
MGT4_CLK_N<18..13>
MGT4_CLK_N<24..19>
MGT4_CLK_N<24..1>
OUT

UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ		DRAWING TITLE: MGT4 CLOCK CML	
BLOCK: CLOCK		SIZE: C	REV.: 27.05.2014
		DRAWING NO.	
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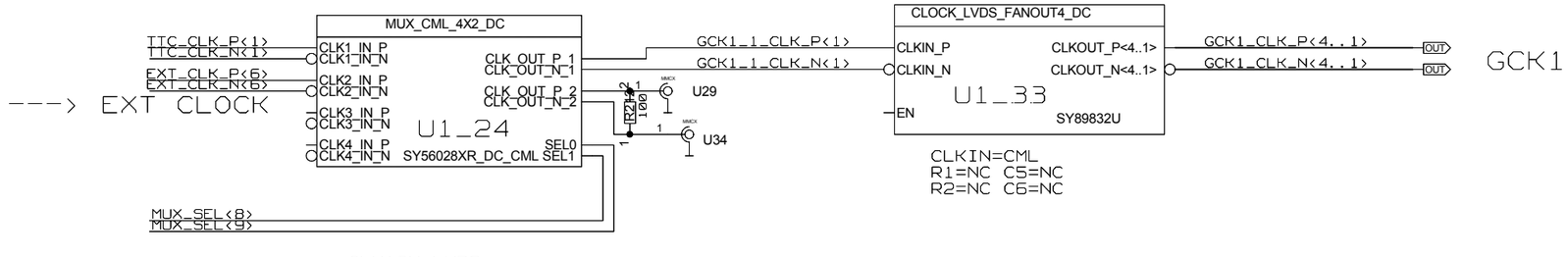
ZONE	LTR	DESCRIPTION	DATE	APPR.

GCK1 + GCK2 CLOCK

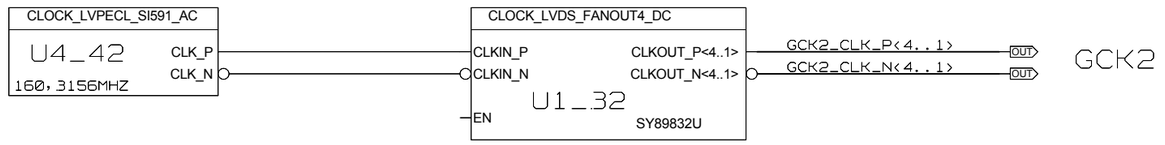
EXTENSION MODUL

---> EXT CLOCK



CLK1IN=LVDS
CLK2IN=CML_AC
CLK3IN=NC
CLK4IN=NC
R3=NC C1=100NF
R4=NC C2=100NF
R5=NC C3=NC
R6=NC C4=NC

CLKIN=CML
R1=NC C5=NC
R2=NC C6=NC

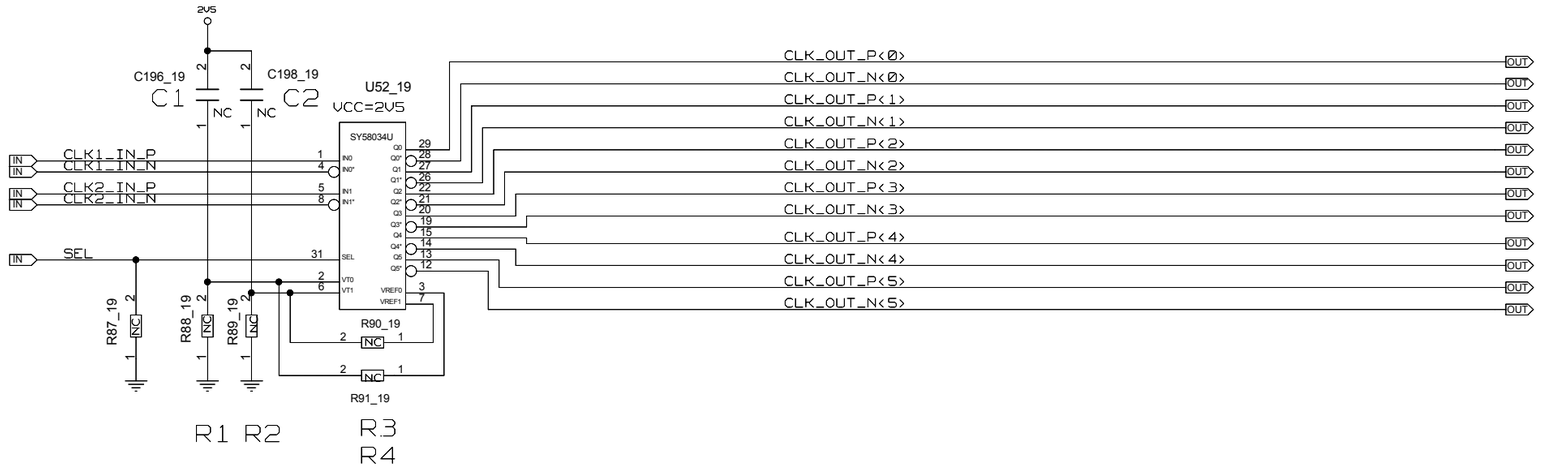


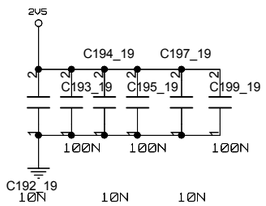
CLKIN=LVPECL_AC
R1=NC C5=10NF
R2=0 C6=NC

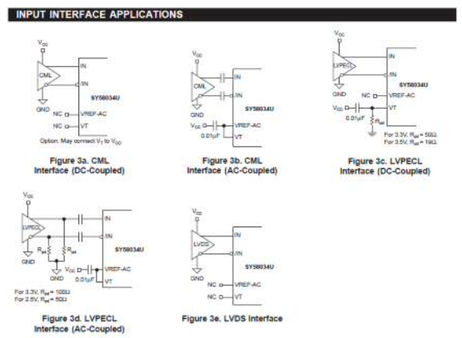
UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ	DRAWING TITLE: GCK1+2 CLOCK LVDS	
BLOCK: CLOCK	SIZE: C	REV.: 27.05.2014
	DRAWING NO.	
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

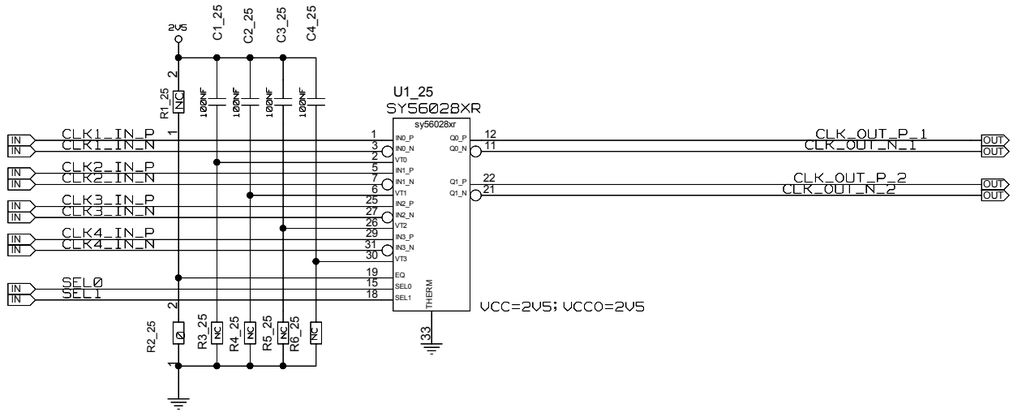


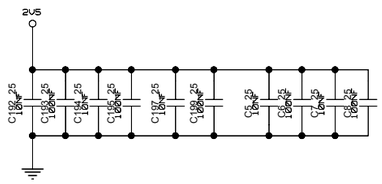




UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_CML_FANOUT6_DC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





Input Interface Applications

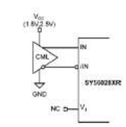


Figure 4a. CML Interface 100 Ω Differential (DC-Coupled, 1.8V, 2.5V)

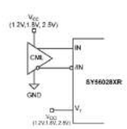


Figure 4b. CML Interface 50 Ω to Vcc (DC-Coupled, 1.2V,1.8V,2.5V)

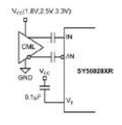


Figure 4c. CML Interface (AC-Coupled) *See note in Functional Description for 1.2V CML driver with AC-Coupling

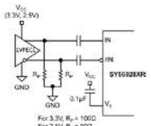


Figure 4d. LVPECL Interface (AC-Coupled)

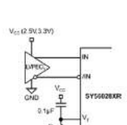


Figure 4e. LVPECL Interface (DC-Coupled 2.5V and 3.3V)

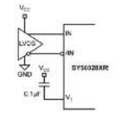


Figure 4f. LVDS Interface

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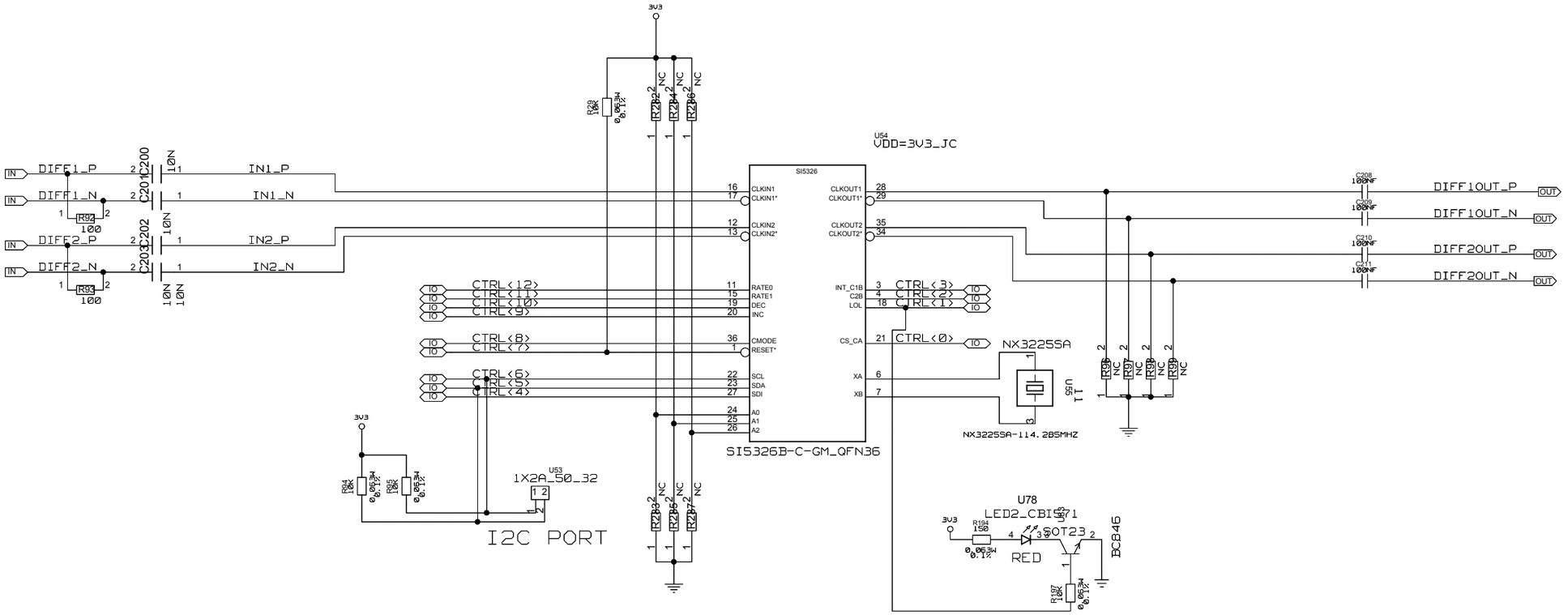

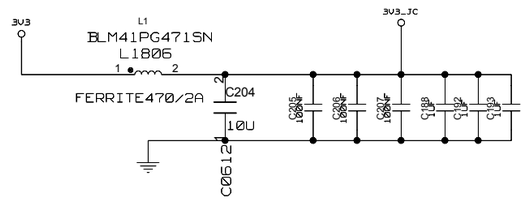

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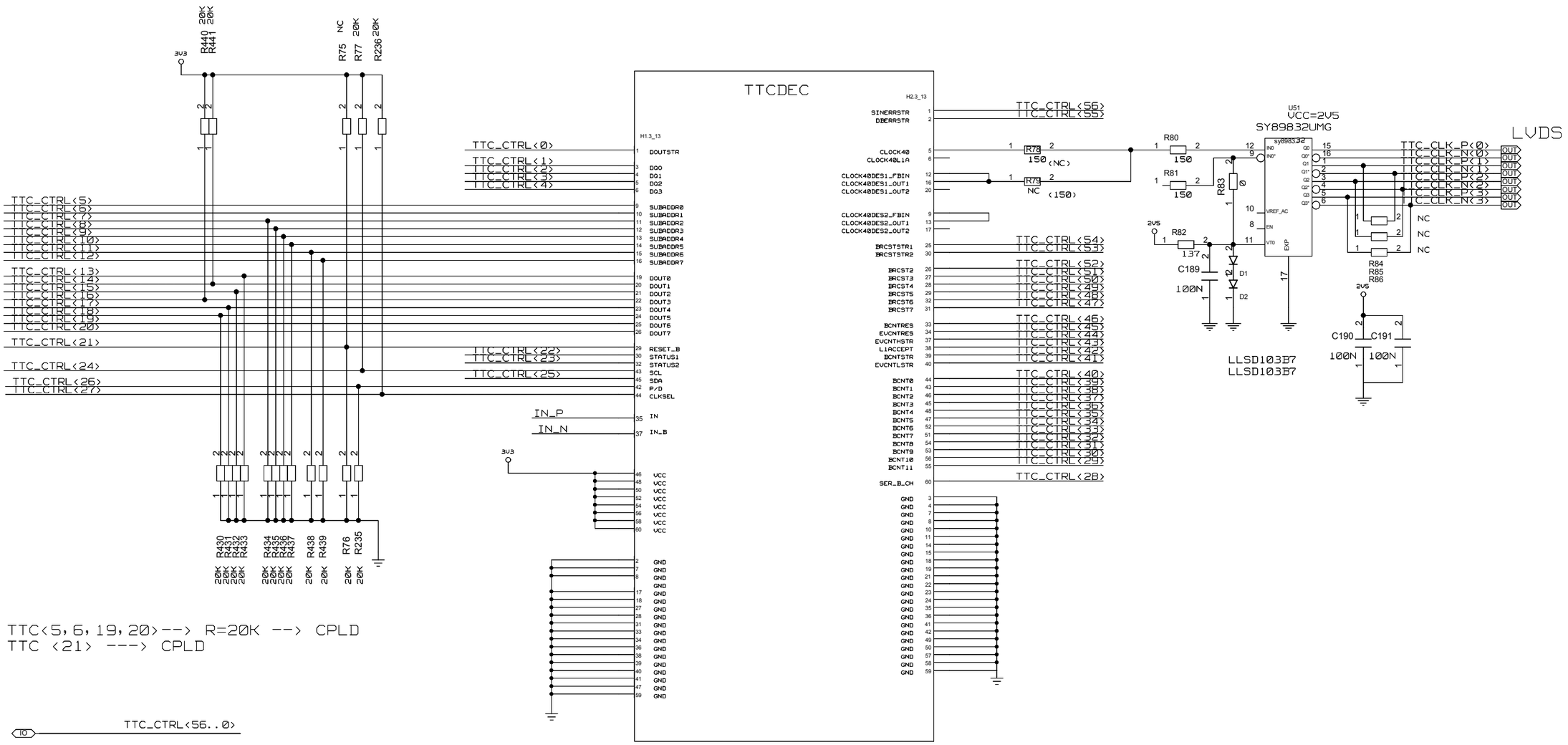

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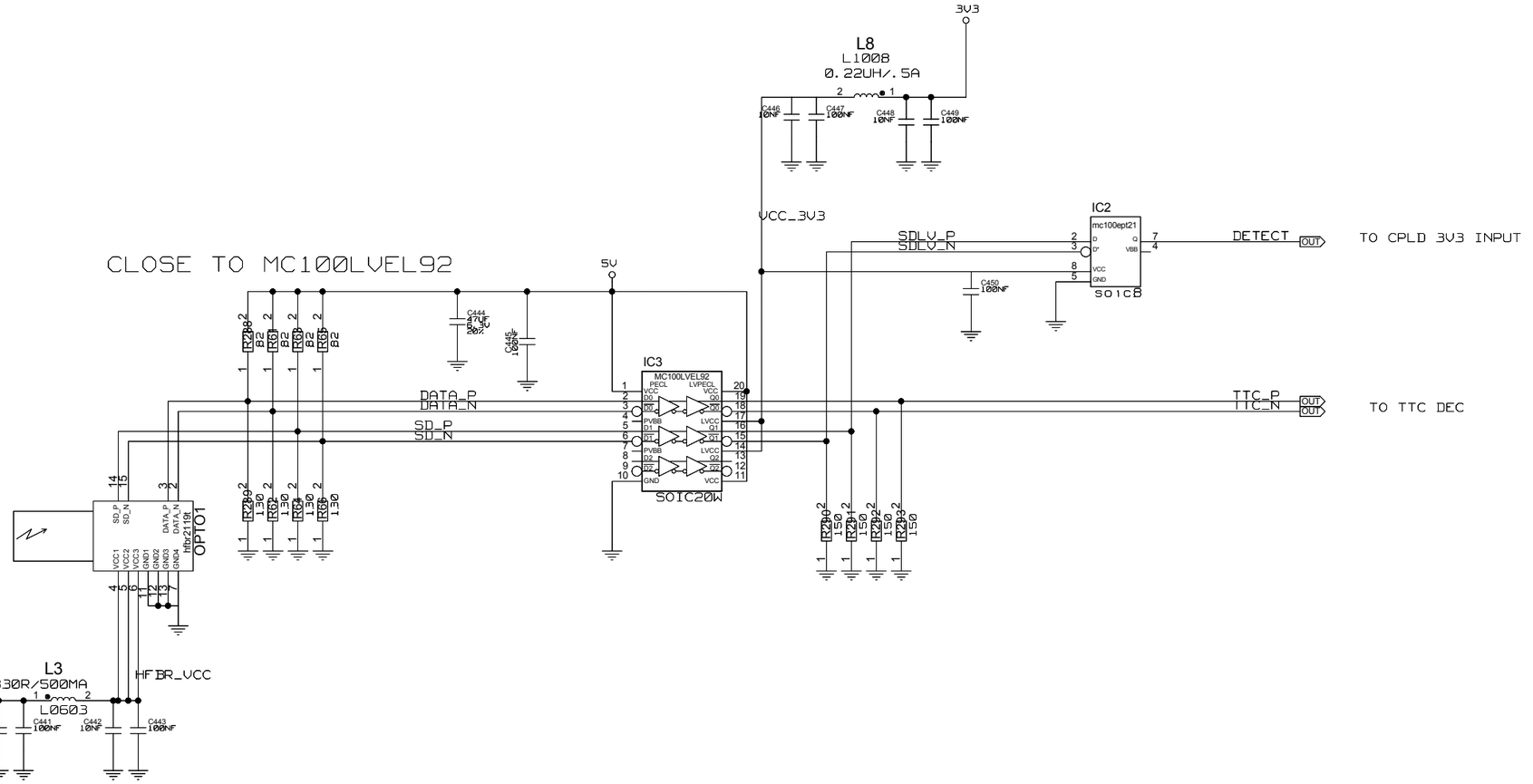

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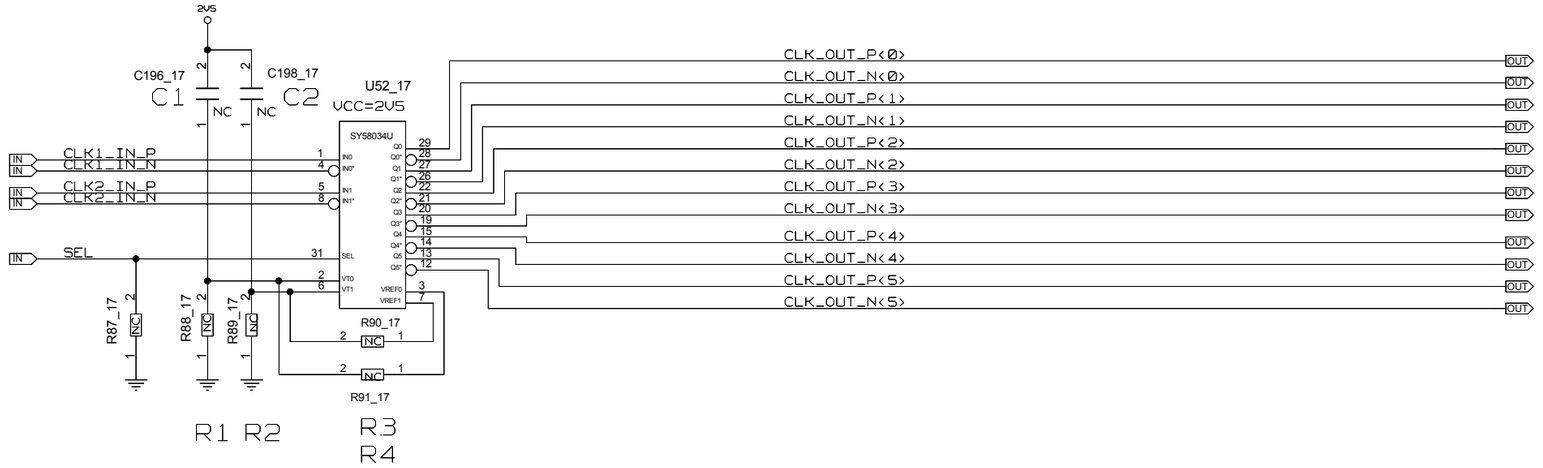

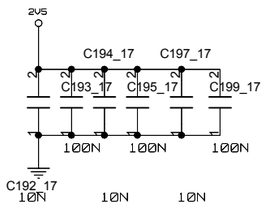

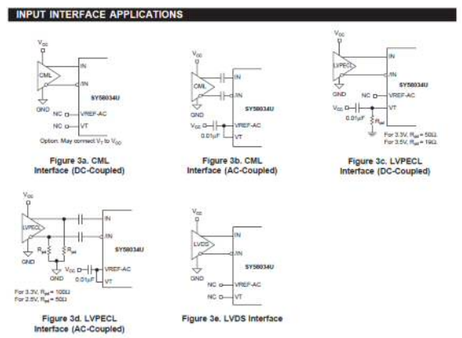

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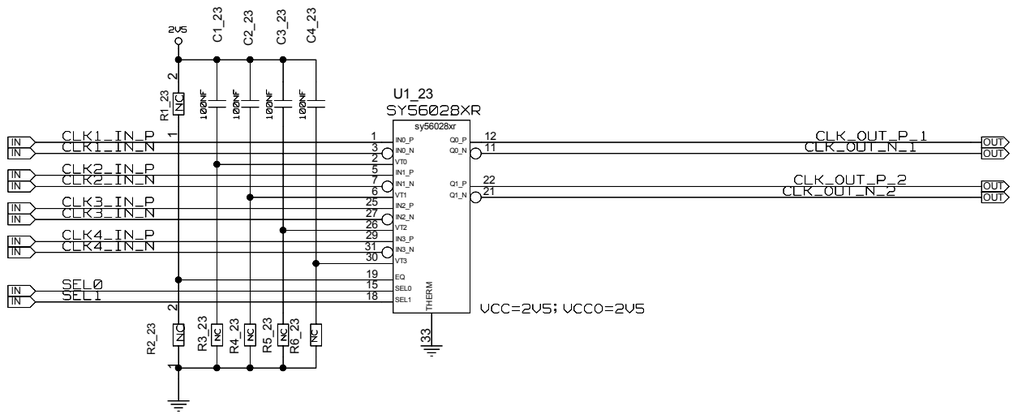

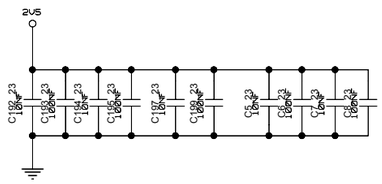

Input Interface Applications

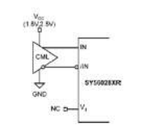

Figure 4a. CML Interface
100 Ω Differential
(DC-Coupled, 1.8V, 2.5V)

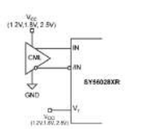

Figure 4b. CML Interface
50 Ω to Vcc
(DC-Coupled, 1.2V,1.8V,2.5V)

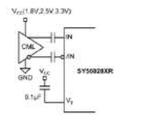

Figure 4c. CML Interface
(AC-Coupled)
*See note in Functional Description
for 1.2V CML driver with AC-Coupling

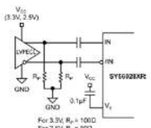

Figure 4d. LVPECL Interface
(AC-Coupled)

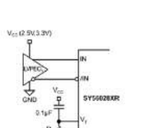

Figure 4e. LVPECL Interface
(DC-Coupled 2.5V and 3.3V)

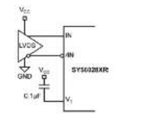

Figure 4f. LVDS Interface

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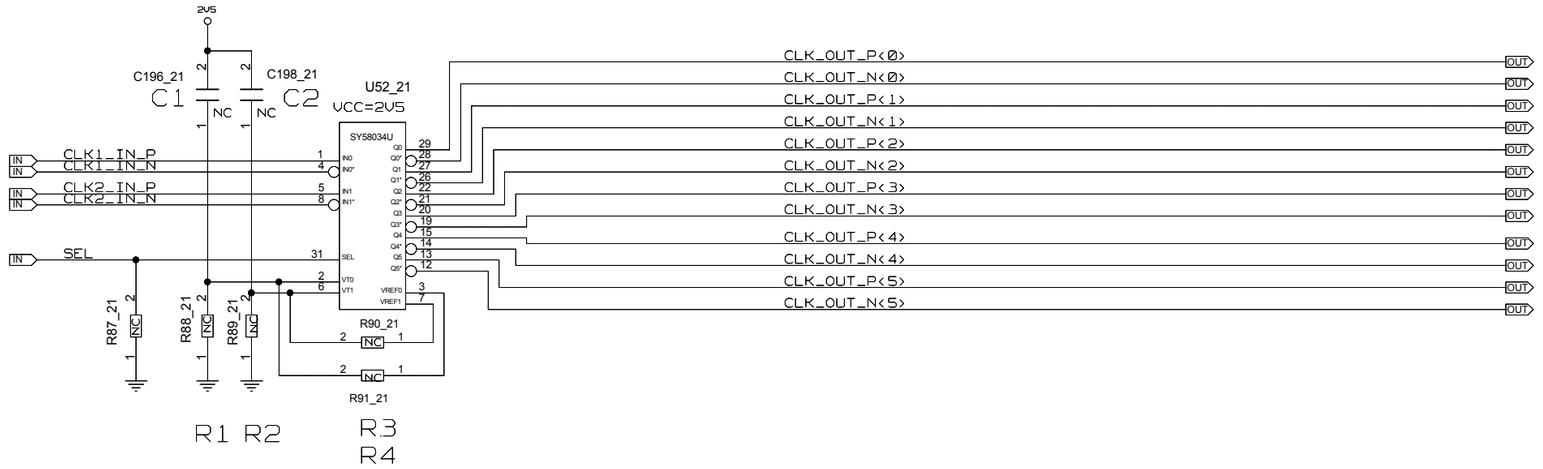

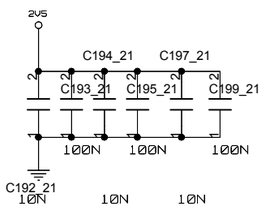

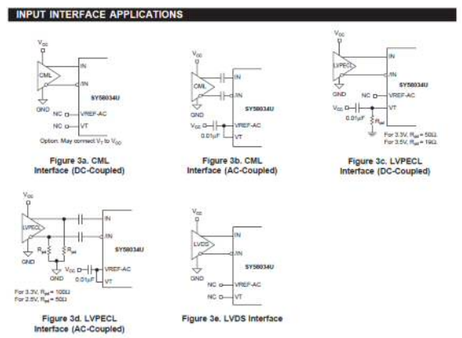

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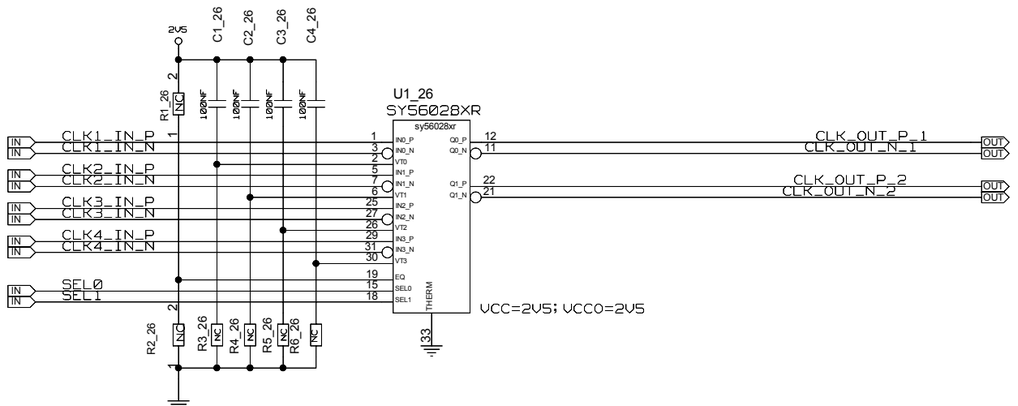

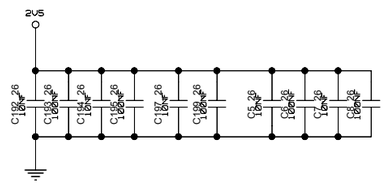

Input Interface Applications

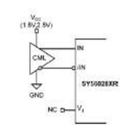

Figure 4a. CML Interface
100 Ω Differential
(DC-Coupled, 1.8V, 2.5V)

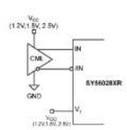

Figure 4b. CML Interface
50 Ω to Vcc
(DC-Coupled, 1.2V,1.8V,2.5V)

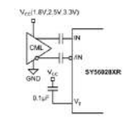

Figure 4c. CML Interface
(AC-Coupled)
*See note in Functional Description
for 1.2V CML driver with AC-Coupling

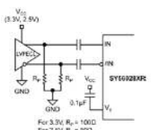

Figure 4d. LVPECL Interface
(AC-Coupled)

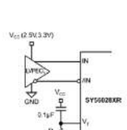

Figure 4e. LVPECL Interface
(DC-Coupled 2.5V and 3.3V)

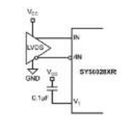

Figure 4f. LVDS Interface

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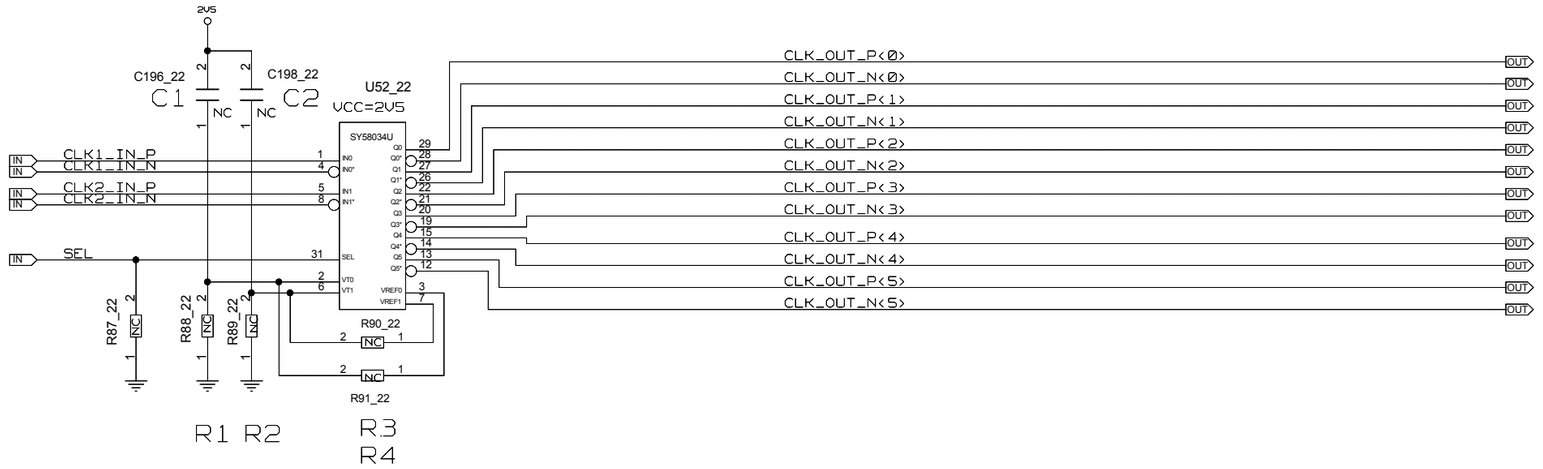

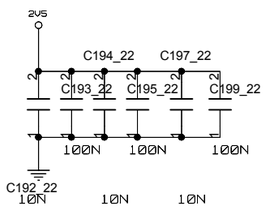

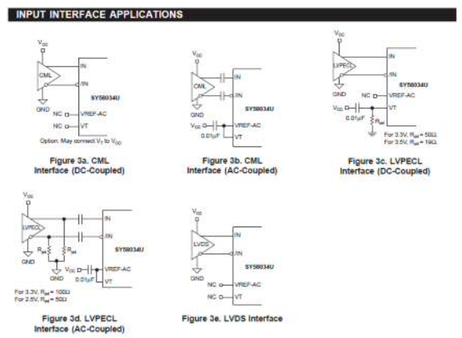

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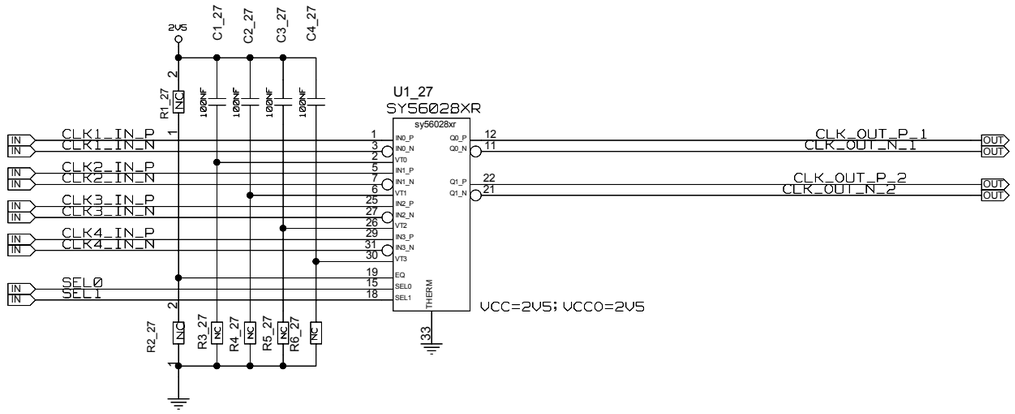

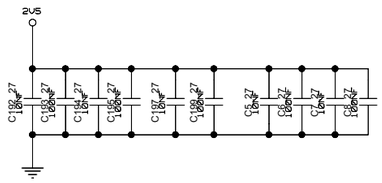

Input Interface Applications

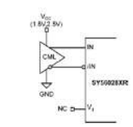

Figure 4a. CML Interface
100 Ω Differential
(DC-Coupled, 1.8V, 2.5V)

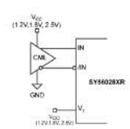

Figure 4b. CML Interface
50 Ω to Vcc
(DC-Coupled, 1.2V,1.8V,2.5V)

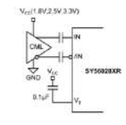

Figure 4c. CML Interface
(AC-Coupled)
*See note in Functional Description
for 1.2V CML driver with AC-Coupling

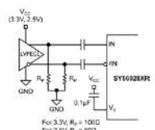

Figure 4d. LVPECL Interface
(AC-Coupled)

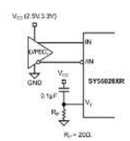

Figure 4e. LVPECL Interface
(DC-Coupled 2.5V and 3.3V)

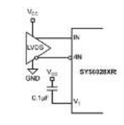

Figure 4f. LVDS Interface

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REVISIONS				
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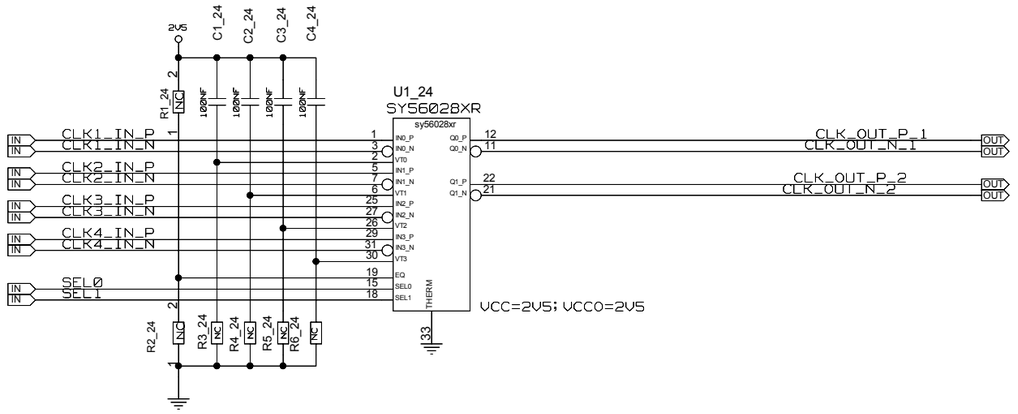

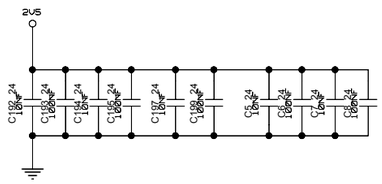

Input Interface Applications

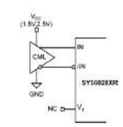

Figure 4a. CML Interface 100 Ω Differential (DC-Coupled, 1.8V, 2.5V)

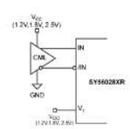

Figure 4b. CML Interface 50 Ω to Vcc (DC-Coupled, 1.2V,1.8V,2.5V)

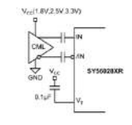

Figure 4c. CML Interface (AC-Coupled) *See note in Functional Description for 1.2V CML driver with AC-Coupling

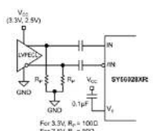

Figure 4d. LVPECL Interface (AC-Coupled)

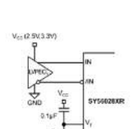

Figure 4e. LVPECL Interface (DC-Coupled 2.5V and 3.3V)

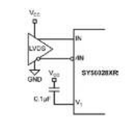

Figure 4f. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: MULTIPLEXER		
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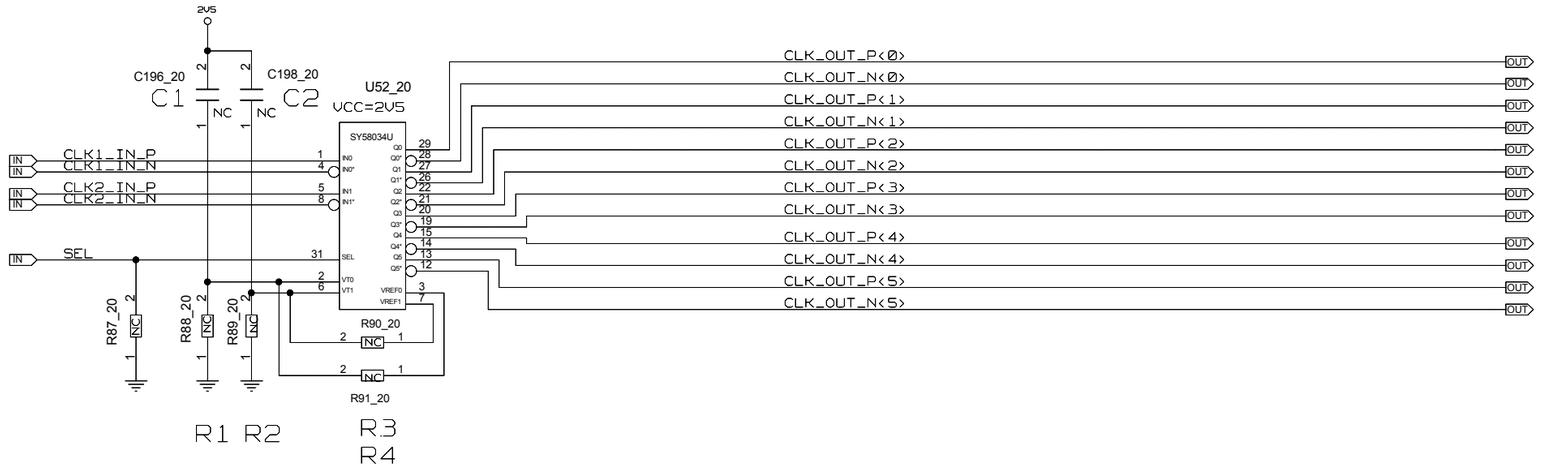
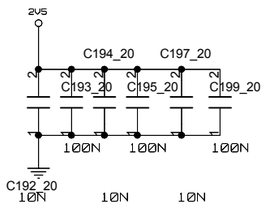
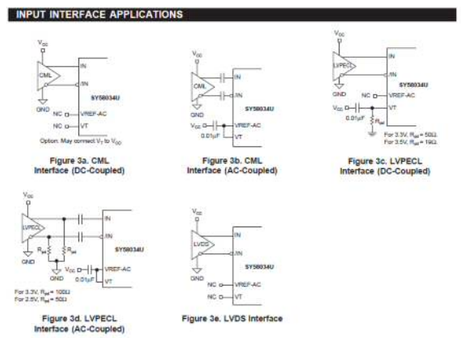
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_CML_FANOUT6_DC		
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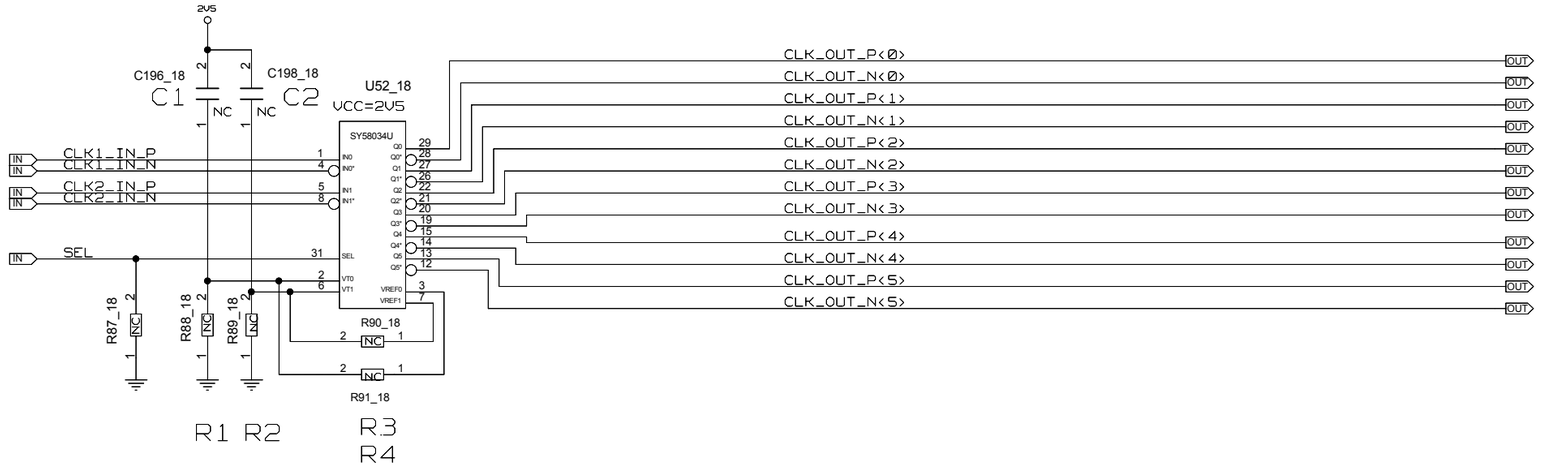
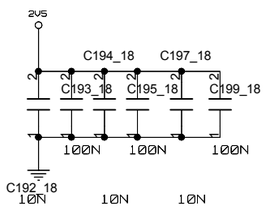
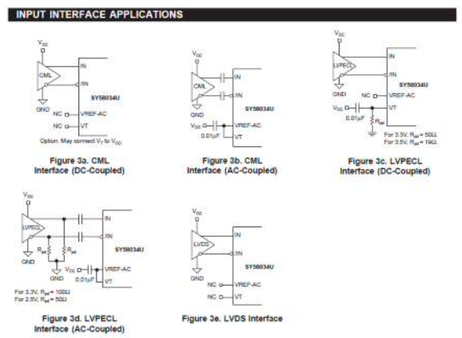
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_CML_FANOUT6_DC		
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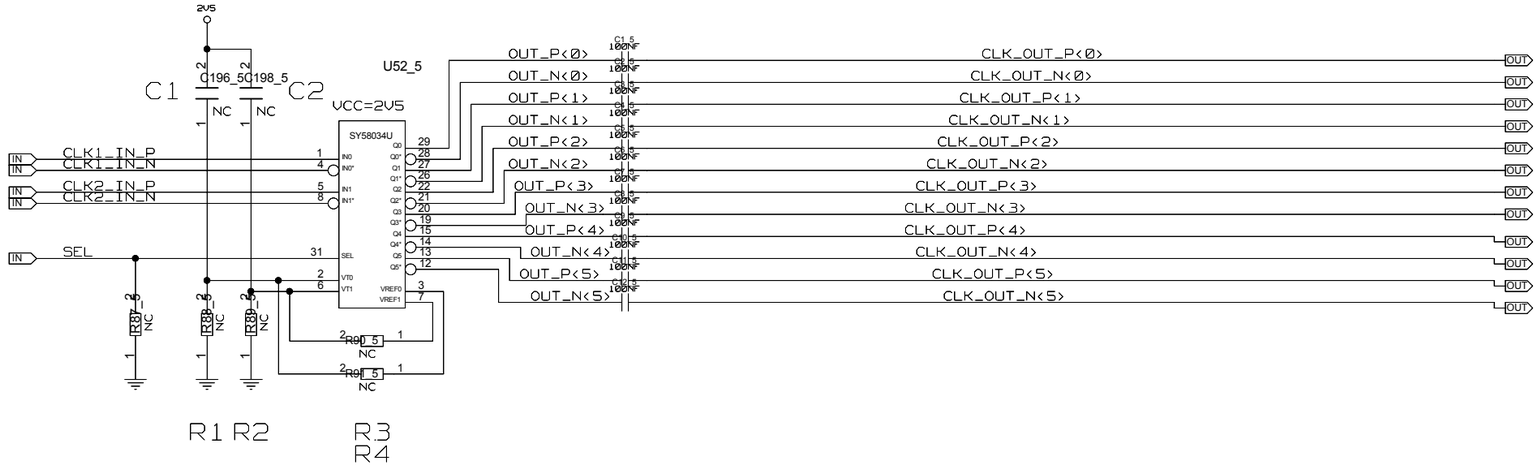
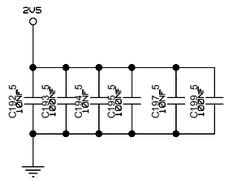
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

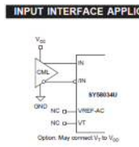


Figure 3a. CML Interface (DC-Coupled)

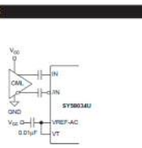


Figure 3b. CML Interface (AC-Coupled)

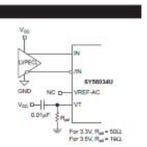


Figure 3c. LVPECL Interface (DC-Coupled)

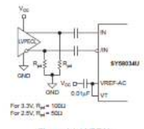


Figure 3d. LVPECL Interface (AC-Coupled)

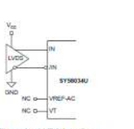
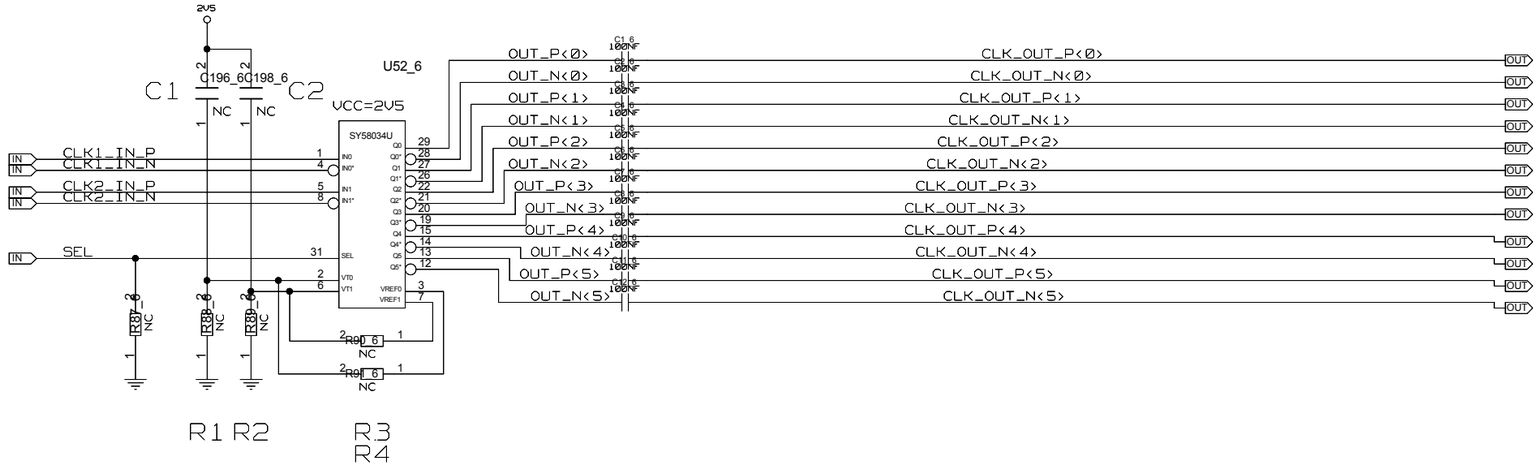
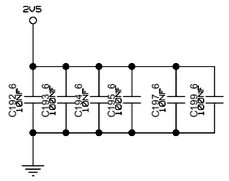


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

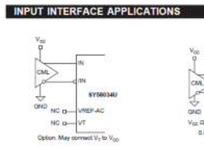


Figure 3a. CML Interface (DC-Coupled)

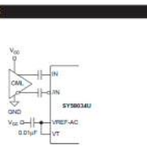


Figure 3b. CML Interface (AC-Coupled)

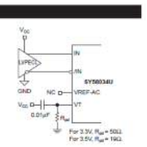


Figure 3c. LVPECL Interface (DC-Coupled)

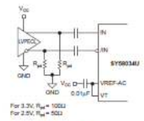


Figure 3d. LVPECL Interface (AC-Coupled)

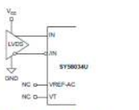
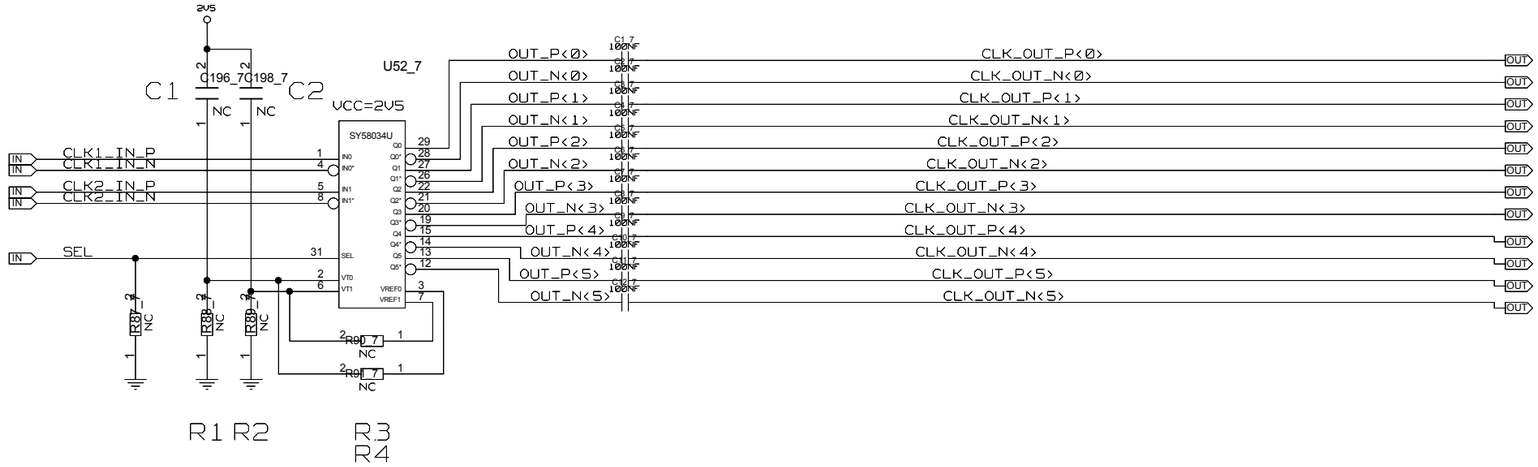
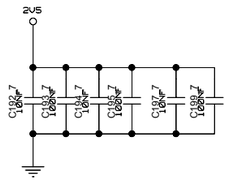


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

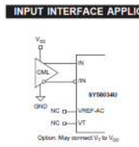


Figure 3a. CML Interface (DC-Coupled)

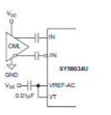


Figure 3b. CML Interface (AC-Coupled)

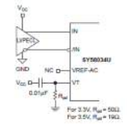


Figure 3c. LVPECL Interface (DC-Coupled)

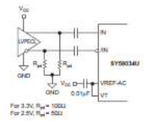


Figure 3d. LVPECL Interface (AC-Coupled)

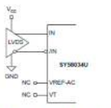
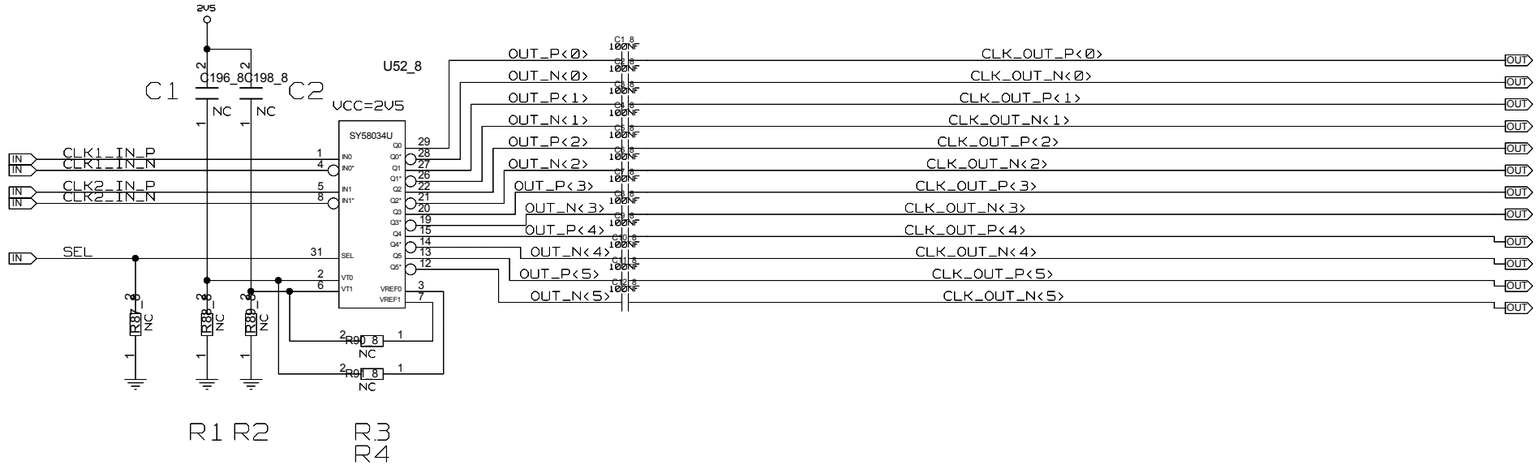
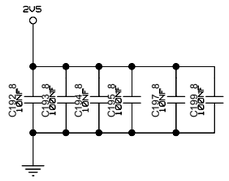


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

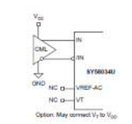


Figure 3a. CML Interface (DC-Coupled)

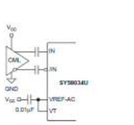


Figure 3b. CML Interface (AC-Coupled)

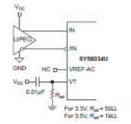


Figure 3c. LVPECL Interface (DC-Coupled)

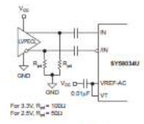


Figure 3d. LVPECL Interface (AC-Coupled)

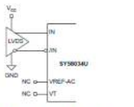
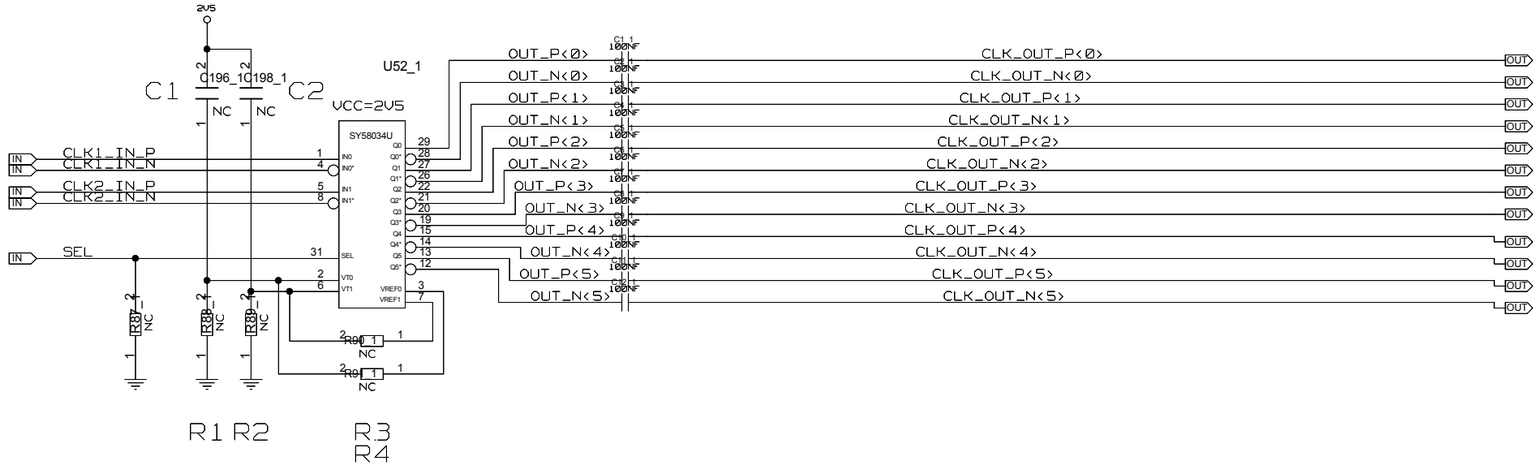
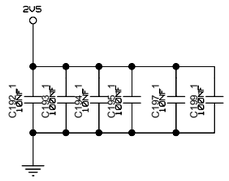


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

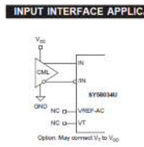


Figure 3a. CML Interface (DC-Coupled)

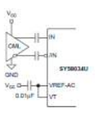


Figure 3b. CML Interface (AC-Coupled)

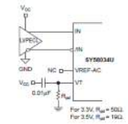


Figure 3c. LVPECL Interface (DC-Coupled)

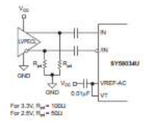


Figure 3d. LVPECL Interface (AC-Coupled)

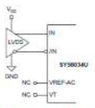
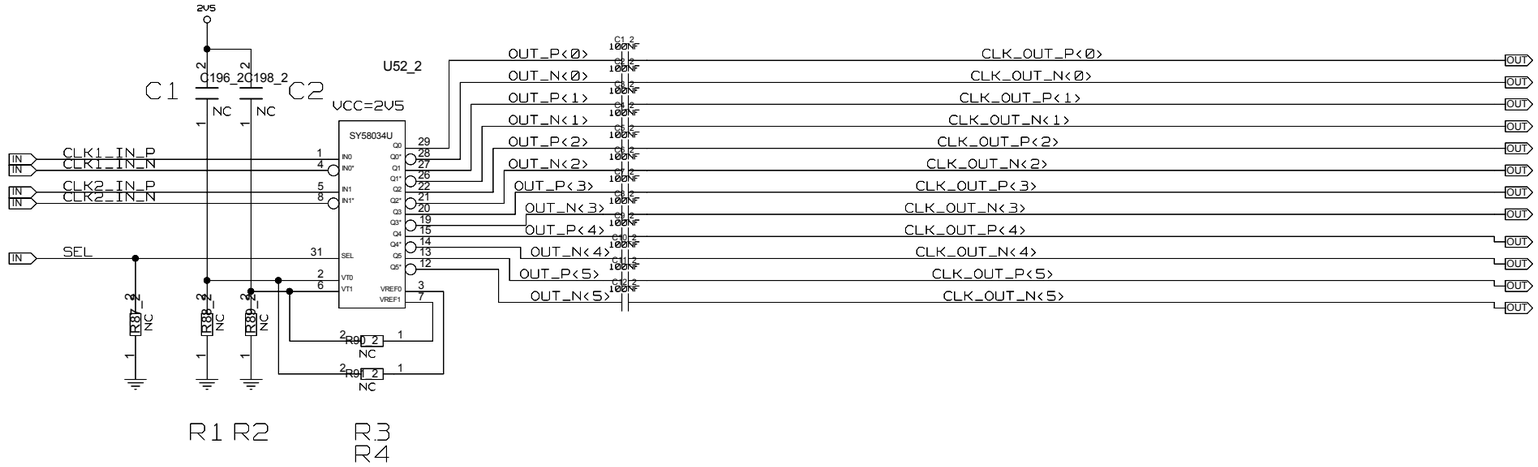
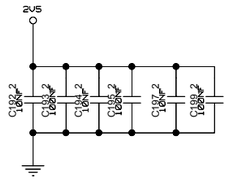


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

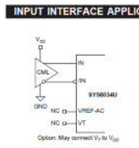


Figure 3a. CML Interface (DC-Coupled)

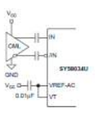


Figure 3b. CML Interface (AC-Coupled)

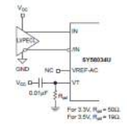


Figure 3c. LVPECL Interface (DC-Coupled)

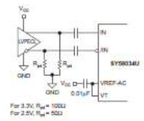


Figure 3d. LVPECL Interface (AC-Coupled)

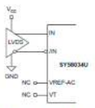
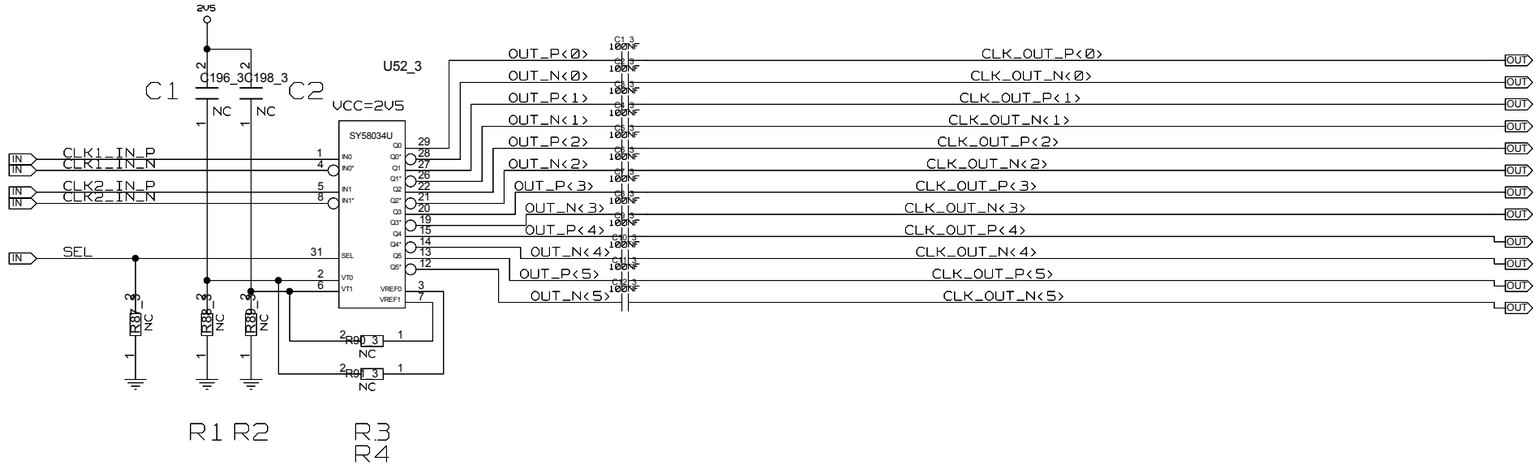
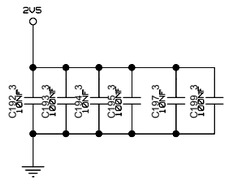


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

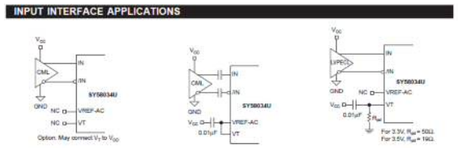


Figure 3a. CML Interface (DC-Coupled)

Figure 3b. CML Interface (AC-Coupled)

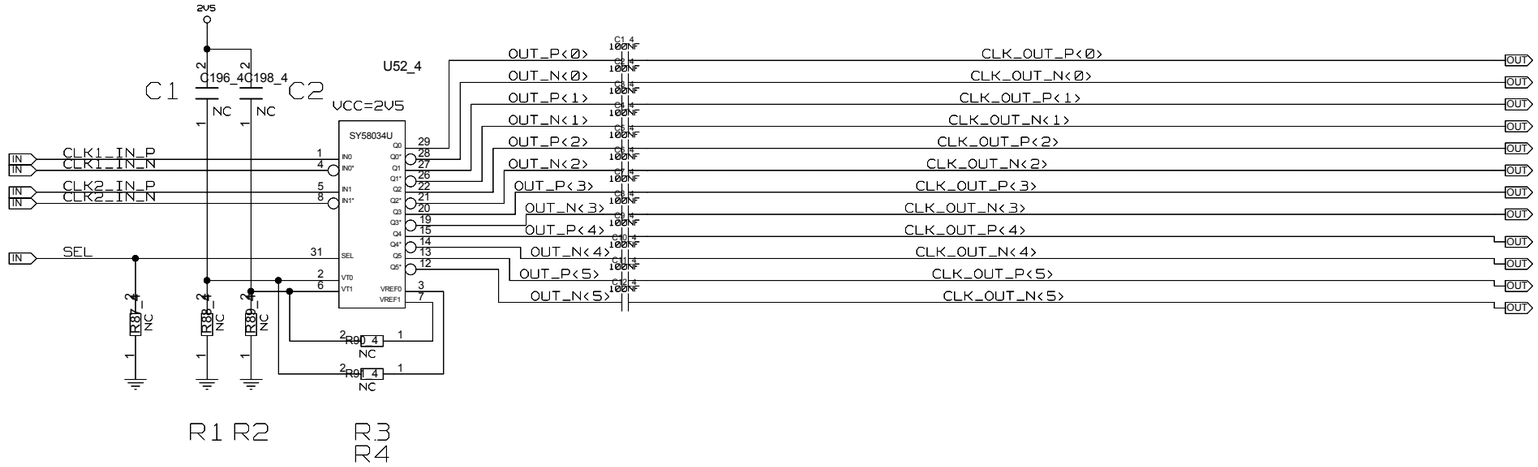
Figure 3c. LVPECL Interface (DC-Coupled)

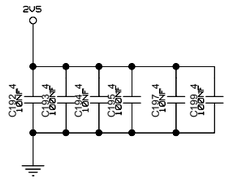
Figure 3d. LVPECL Interface (AC-Coupled)

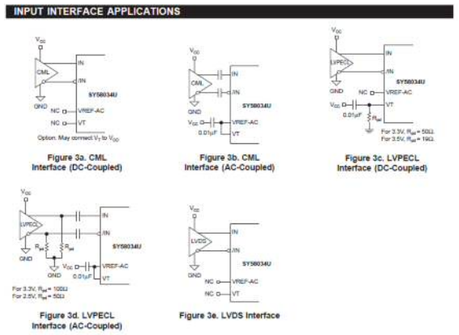
Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
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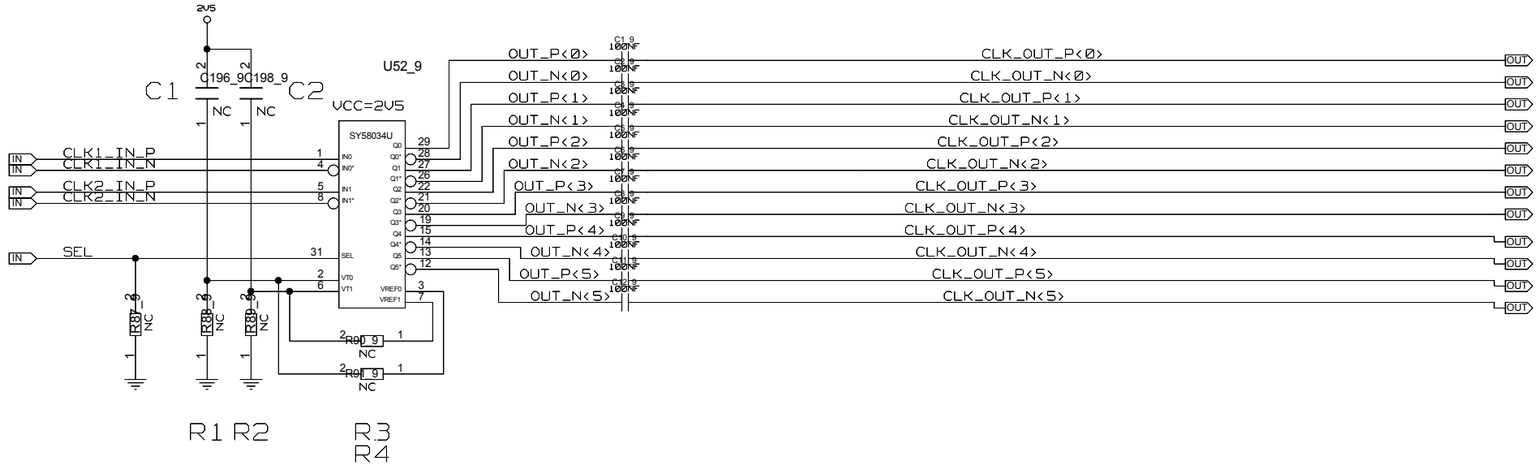
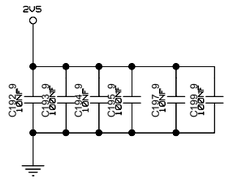
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

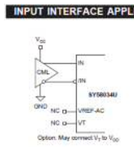


Figure 3a. CML Interface (DC-Coupled)

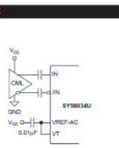


Figure 3b. CML Interface (AC-Coupled)

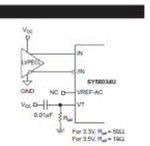


Figure 3c. LVPECL Interface (DC-Coupled)

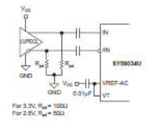


Figure 3d. LVPECL Interface (AC-Coupled)

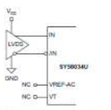
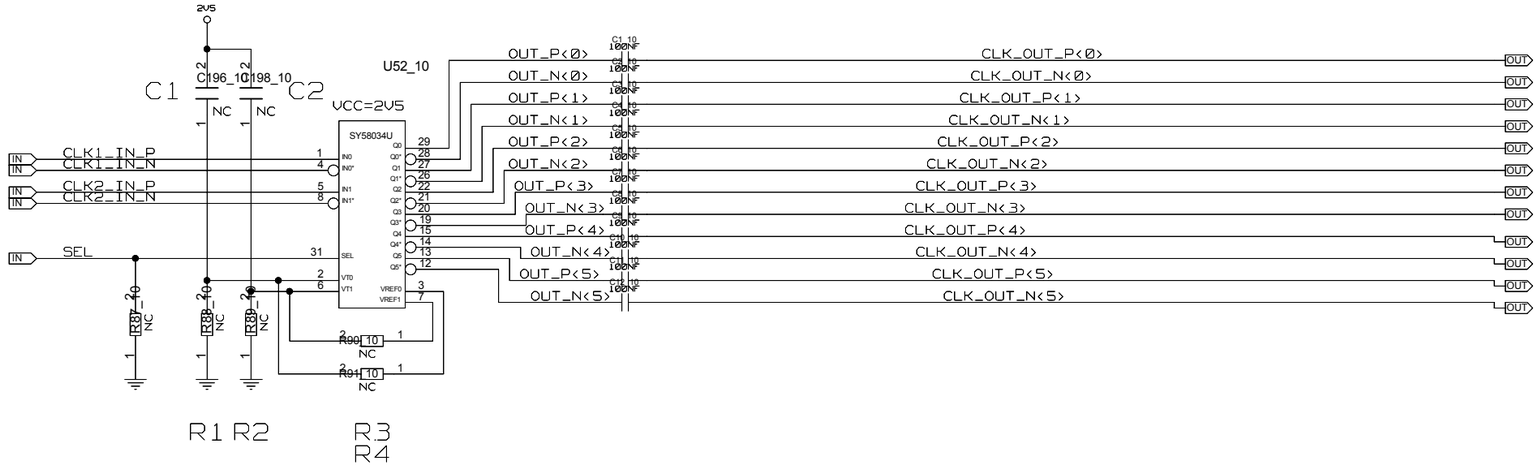
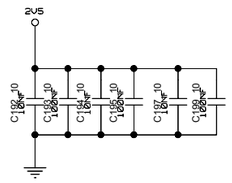


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

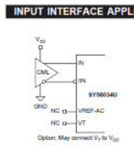


Figure 3a. CML Interface (DC-Coupled)

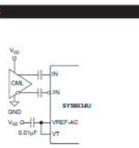


Figure 3b. CML Interface (AC-Coupled)

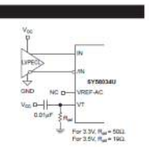


Figure 3c. LVPECL Interface (DC-Coupled)

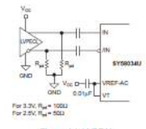


Figure 3d. LVPECL Interface (AC-Coupled)

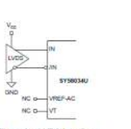
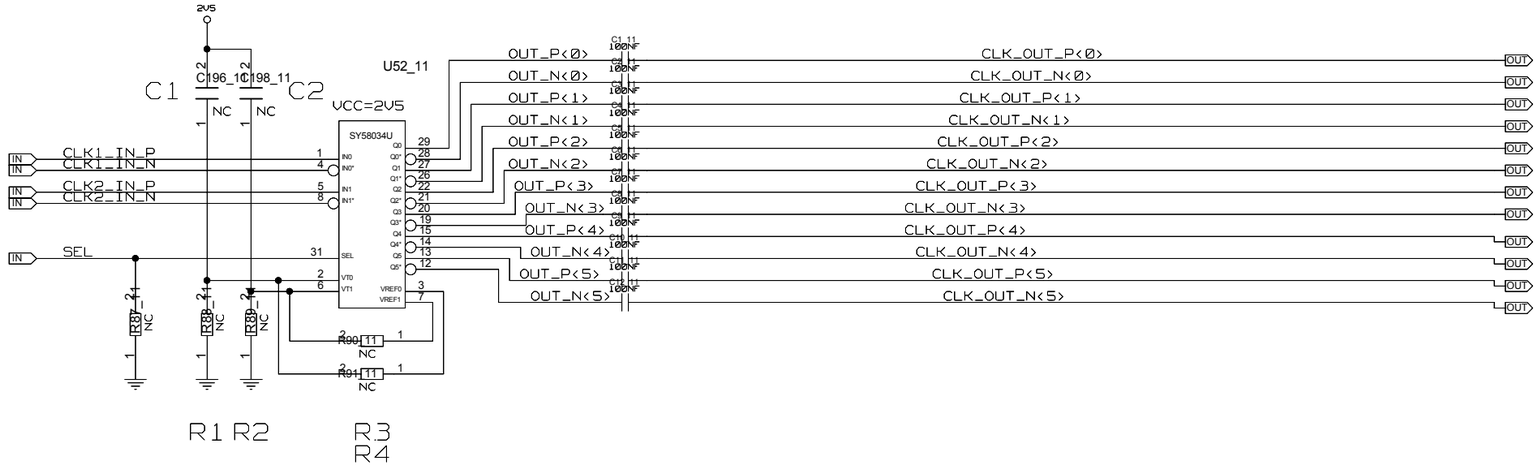
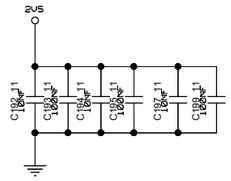


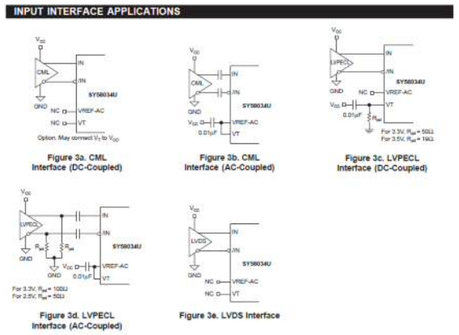
Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
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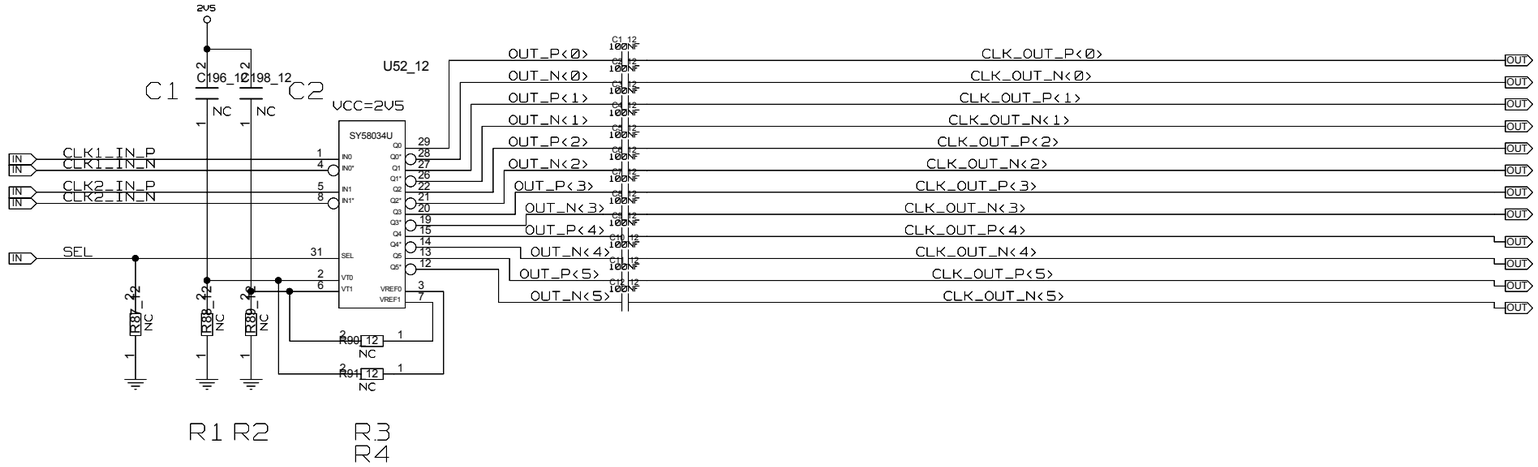
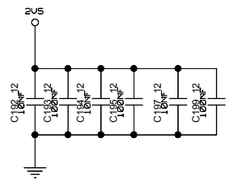
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

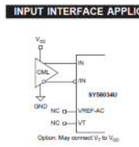


Figure 3a. CML Interface (DC-Coupled)

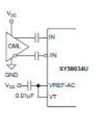


Figure 3b. CML Interface (AC-Coupled)

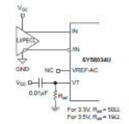


Figure 3c. LVPECL Interface (DC-Coupled)

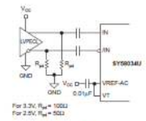


Figure 3d. LVPECL Interface (AC-Coupled)

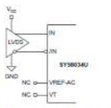
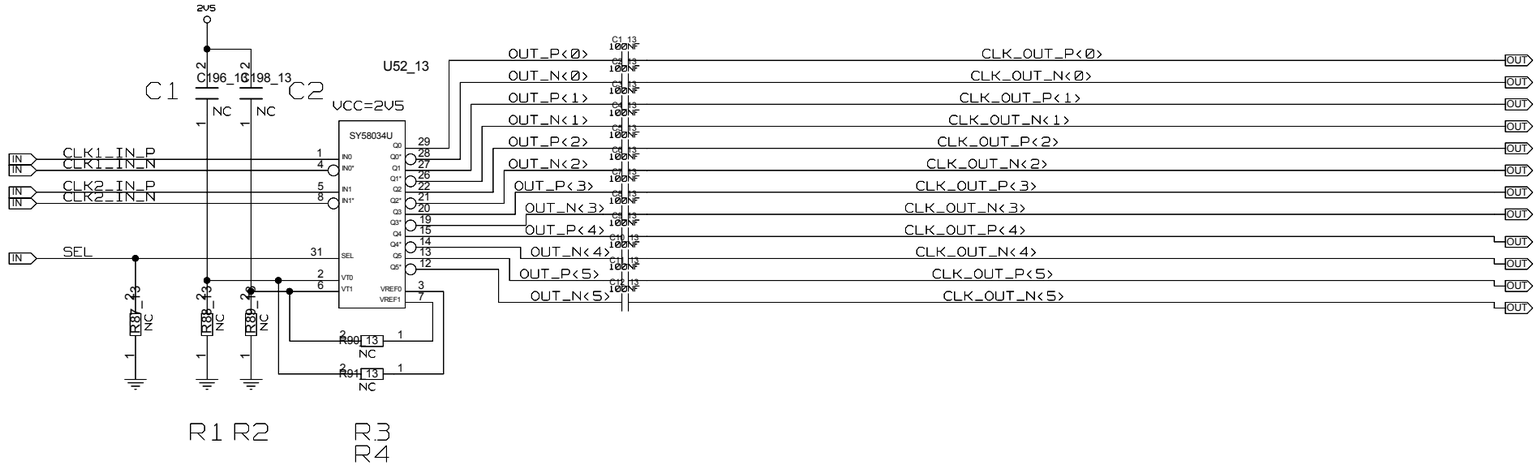
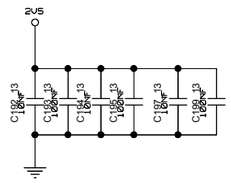


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

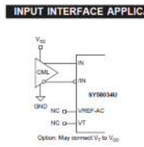


Figure 3a. CML Interface (DC-Coupled)

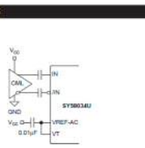


Figure 3b. CML Interface (AC-Coupled)

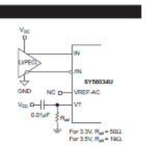


Figure 3c. LVPECL Interface (DC-Coupled)

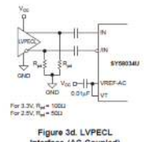


Figure 3d. LVPECL Interface (AC-Coupled)

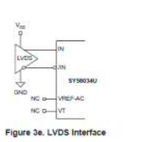


Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC		
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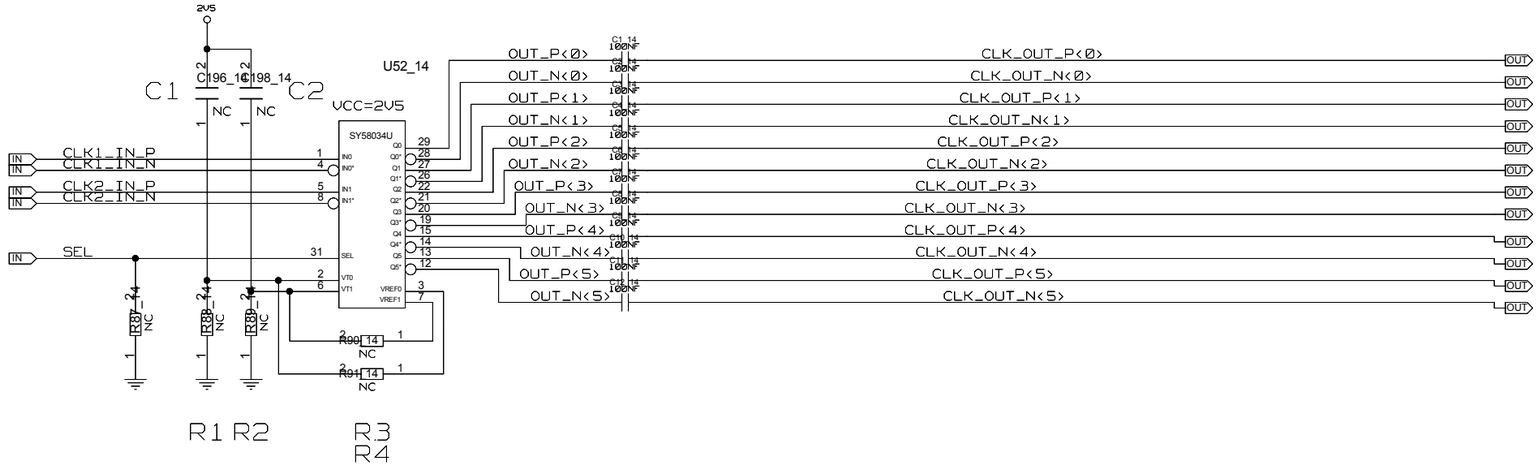
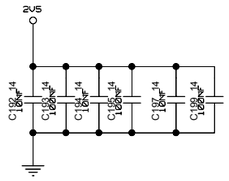
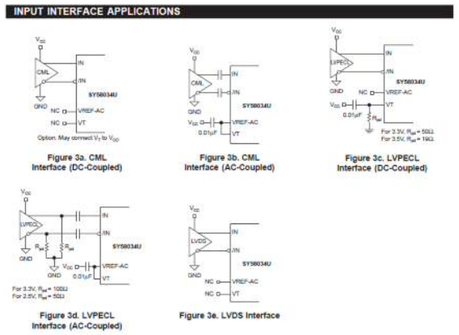
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.







UNIVERSITY OF MAINZ		DRAWING TITLE: CLOCK CML FANOUT6 AC	
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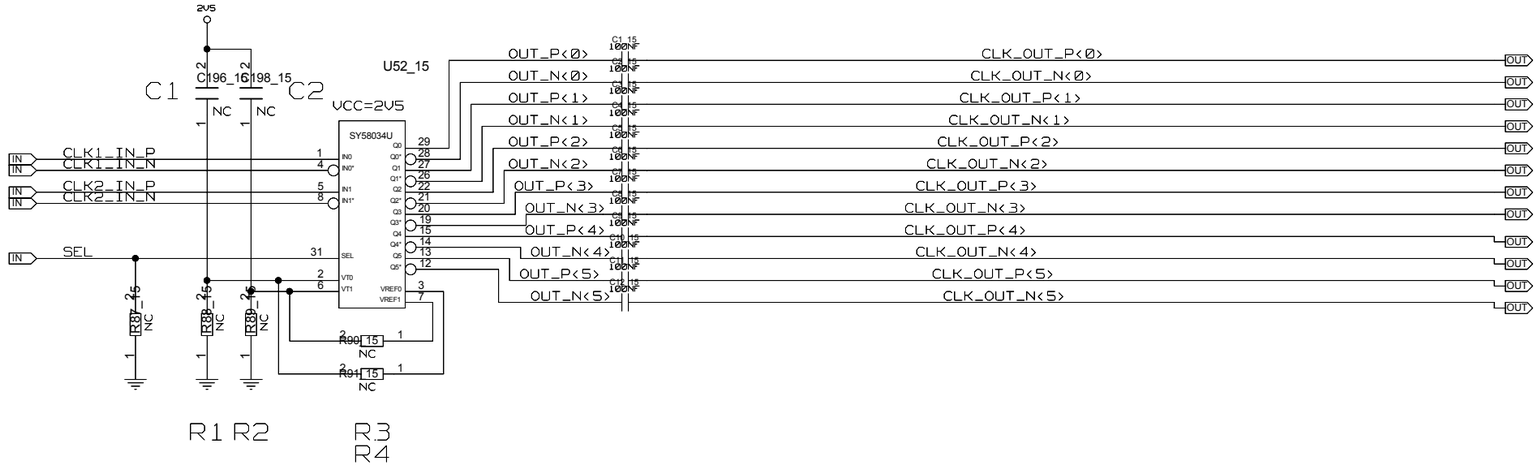
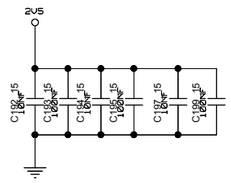
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

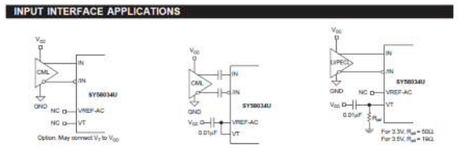


Figure 3a. CML Interface (DC-Coupled)

Figure 3b. CML Interface (AC-Coupled)

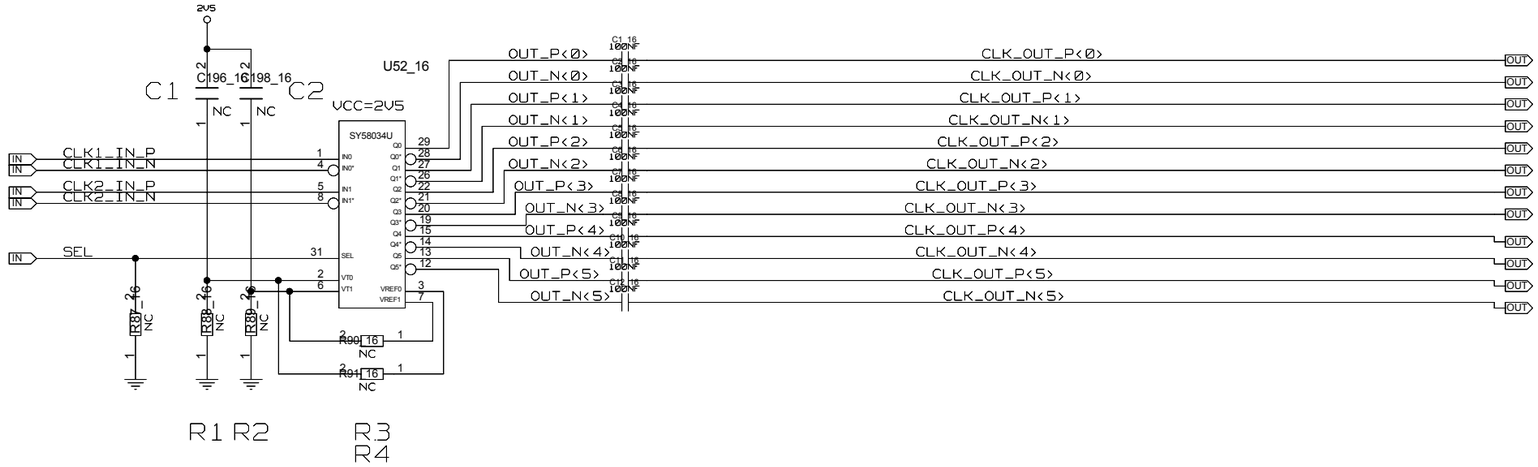
Figure 3c. LVPECL Interface (DC-Coupled)

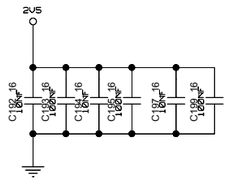
Figure 3d. LVPECL Interface (AC-Coupled)

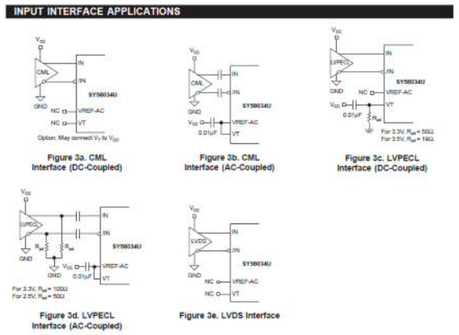
Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

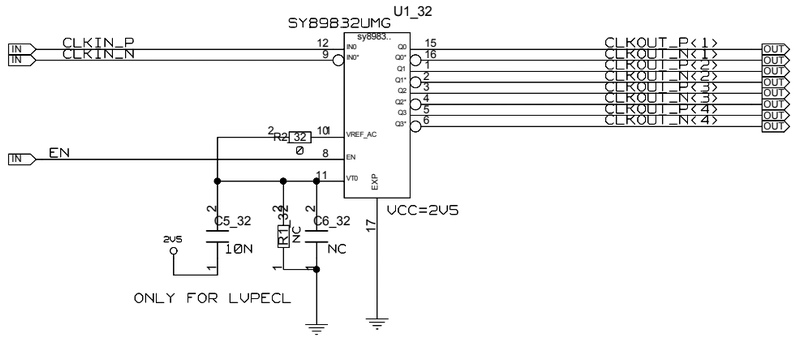


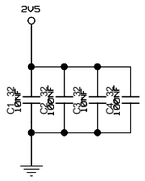




UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK CML FANOUT6 AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

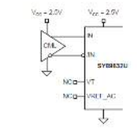


Figure 3a. DC-Coupled CML Input Interface

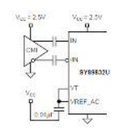


Figure 3b. AC-Coupled CML Input Interface

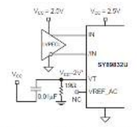


Figure 3c. DC-Coupled LVPECL Input Interface
(*Bypass with 0.01µF to GND)

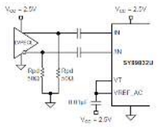


Figure 3d. AC-Coupled LVPECL Input Interface

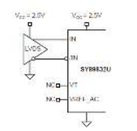
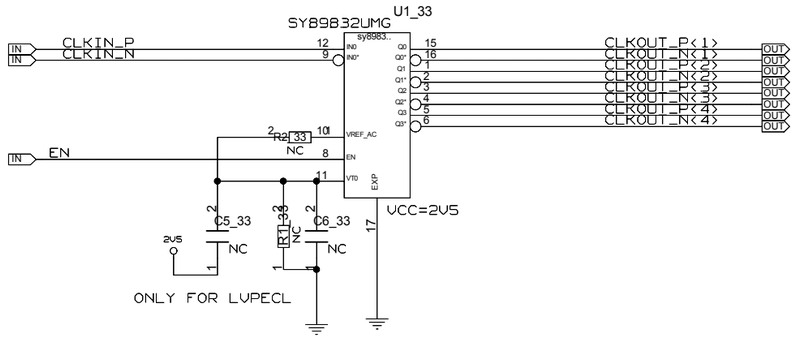
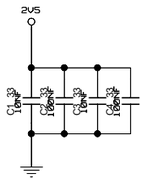


Figure 3e. LVDS Input Interface

UNIVERSITY OF MAINZ		DRAWING TITLE: CLOCK LVDS FANOUT4 DC	
BLOCK: CLOCK	SIZE C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





INPUT INTERFACE APPLICATIONS

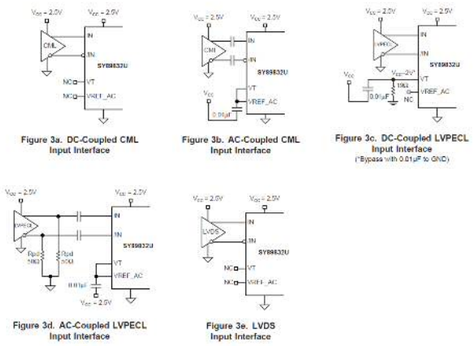


Figure 3a. DC-Coupled CML Input Interface

Figure 3b. AC-Coupled CML Input Interface

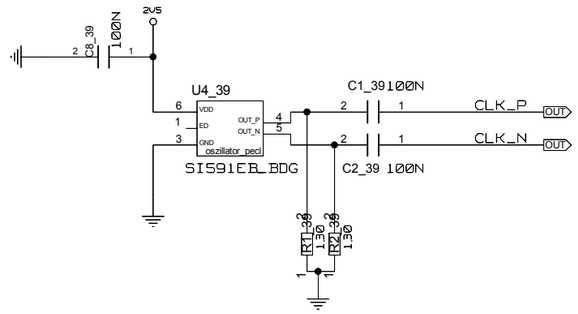
Figure 3c. DC-Coupled LVPECL Input Interface (*Bypass with 0.01µF to GND)

Figure 3d. AC-Coupled LVPECL Input Interface

Figure 3e. LVDS Input Interface

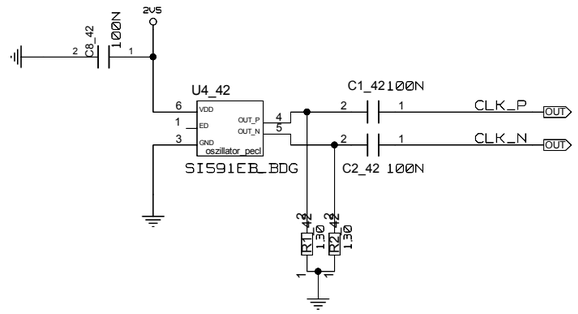
UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK LVDS FANOUT4 DC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



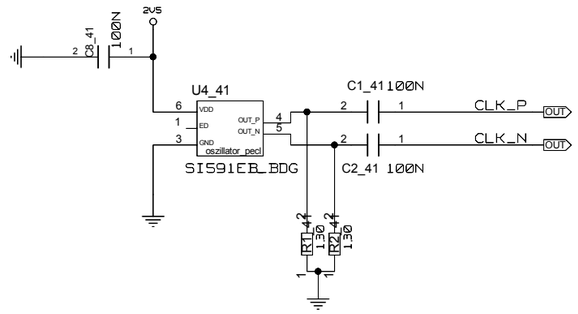
UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



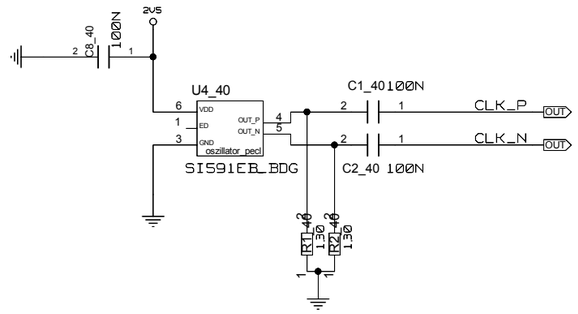
UNIVERSITY OF MAINZ		DRAWING TITLE: CLOCK_LVPECL_AC	
BLOCK: CLOCK		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



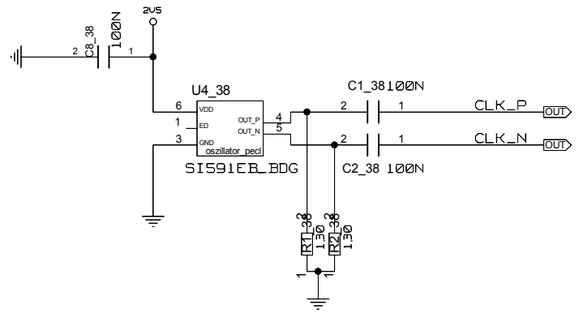
UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC	
BLOCK: CLOCK	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ		DRAWING TITLE: CLOCK_LVPECL_AC	
BLOCK: CLOCK		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: CLOCK_LVPECL_AC		
BLOCK: CLOCK	SIZE: C	REV.	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

GCK2_CLK_N<4..1>
GCK2_CLK_P<4..1>
GCK1_CLK_N<4..1>
GCK1_CLK_P<4..1>

VIRTEX7_CONTROL
VIRTEX7_CTRL<19..0>
CTRLBUS_P<41..0>
CTRLBUS_N<41..0>
EXT_V7_P<43..0>
EXT_V7_N<43..0>
GCK1_P<2..1>
GCK1_N<2..1>
GCK2_P<2..1>
GCK2_N<2..1>
DXP_U1
DXN_U1
DXP_U2
DXN_U2

KINTEX7_CONTROL
KINTEX7_CTRL<6..0>
CTRLBUS_P<41..0>
CTRLBUS_N<41..0>
JC_CTRL<12..0>
TTC_CTRL<56..0>
EXT_K7_P<23..0>
EXT_K7_N<23..0>
EXT_K7<49..0>
AVAGO_SDA<2..0>
AVAGO_SCL<2..0>
AVAGO_CTRL<35..0>
POWER_SDA
POWER_SCL
GCK1_P<2..1>
GCK1_N<2..1>
GCK2_P<2..1>
GCK2_N<2..1>
IPMC_K7_3V3<51..0>
ATCA_CTRL<11..0>
KINTEX_CPLD<26..0>
DXP_U3
DXN_U3
ACE_DA<20..0>

IPMC
IPMC_K7_3V3<51..0>
ATCA_CTRL<11..0>
PWR_ON
IPMC_MGT_I2C_SDA
IPMC_MGT_I2C_SCL
A_OK
B_OK
DXP_U1
DXN_U1
DXP_U2
DXN_U2
DXP_U3
DXN_U3

JC_CTRL<12..0>
TTC_CTRL<56..0>
AVAGO_SDA<2..0>
AVAGO_SCL<2..0>
AVAGO_CTRL<35..0>
POWER_SDA
POWER_SCL
ATCA_CTRL<11..0>
IPMC_K7_3V3<51..0>
ATCA_CTRL_B<11..0>
KINTEX_CPLD<26..0>
DXP_U3
DXN_U3
ACE_DA<20..0>

CPLD
TTC_DETECT
MUX_SEL<9..0>
VIRTEX7_CTRL<19..0>
KINTEX7_CTRL<6..0>
EXT_CPLD<15..0>
TTC_CTRL<56..0>
KINTEX_CPLD<26..0>
ATCA_CTRL<11..0>
ACE_CTRL<5..0>
I3

JTAG_PORT
ACE_DA<20..0>
ACE_CTRL<5..0>
ACE INTERFACE

EXTENSION_MODUL
EXT_V7_P<43..0>
EXT_V7_N<43..0>
EXT_K7_P<23..0>
EXT_K7_N<23..0>
EXT_K7<49..0>
EXT_CPLD<15..0>
MGT8_CLK_P
MGT8_CLK_N
EXT_CLK_P<6..0>
EXT_CLK_N<6..0>
V7_MGTTX_P<7..0>
V7_MGTTX_N<7..0>
K7_MGTRX_P<3..0>
K7_MGTRX_N<3..0>
K7_MGTTX_P<3..0>
K7_MGTTX_N<3..0>
SMARTSYNC<5..0>

FROM POWERSUPPLY

3V3_UP
C711
100N
U37

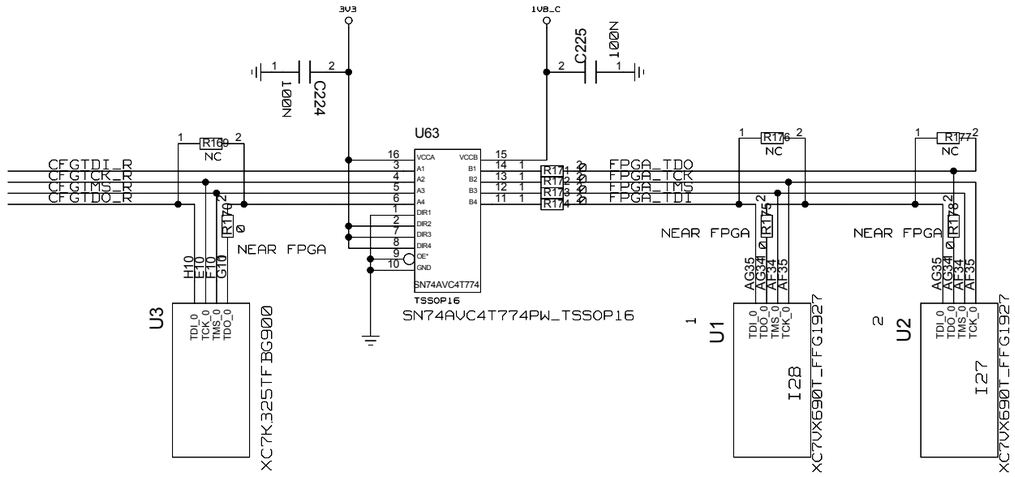
IC1
ATCA_CTRL<11..0>
ATCA_CTRL_B<11..0>
1OE*
2OE*
1A0
1A1
1A2
1A3
2A0
2A1
2A2
2A3
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
VCC
GND
SN74HCT244PW

FROM ATCA BACKPLANE
TO KINTEX AND CPLD

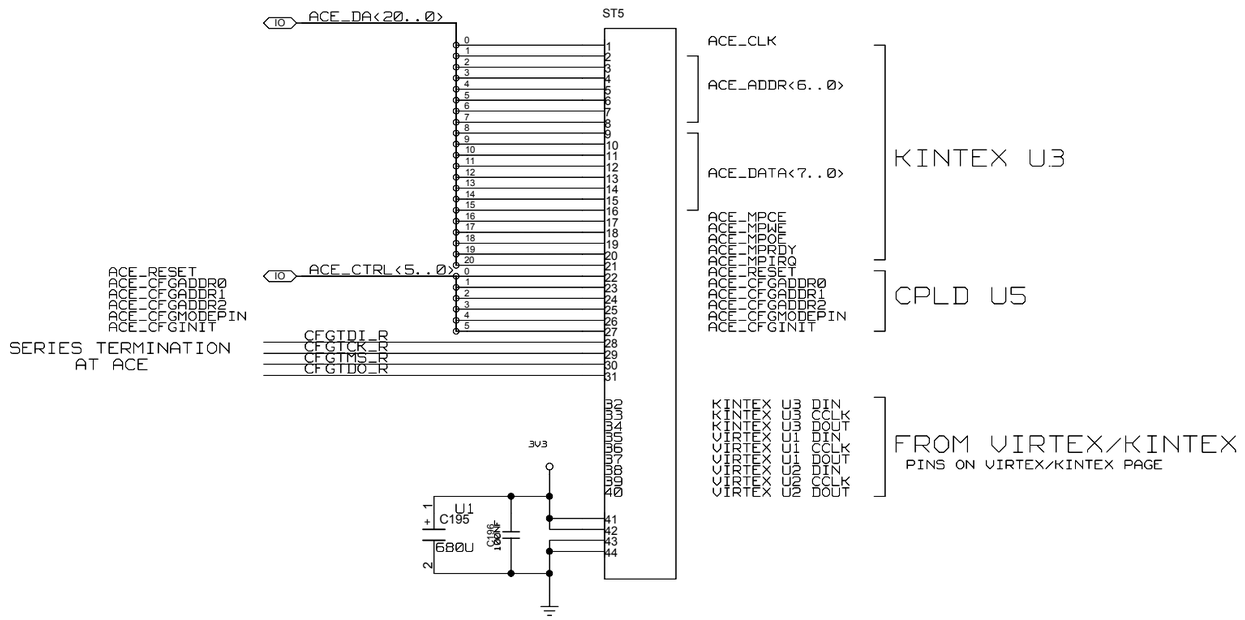
UNIVERSITY OF MAINZ	DRAWING TITLE: BOARDCONTROL		
BLOCK: CONTROL	SIZE: C	REV.: 30.05.2014	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

SERIES TERMINATION
AT ACE

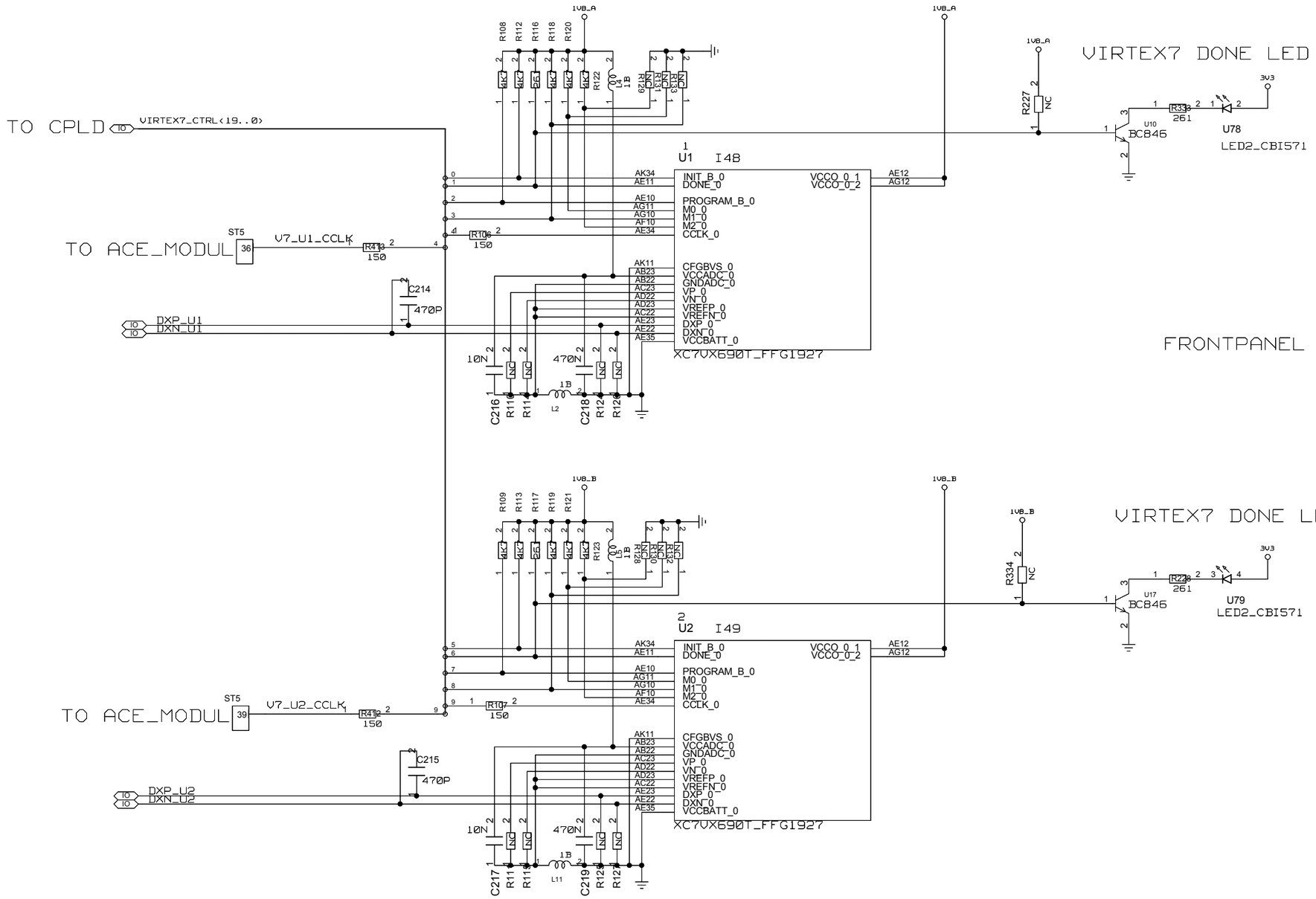


TO ACE DAUGHTERBOARD



UNIVERSITY OF MAINZ		DRAWING TITLE: JTAG + ACE INTERFACE	
BLOCK: CONTROL JTAG		SIZE: C	REV.: 02.05.2014
		SCALE	SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ	DRAWING TITLE: CONTROL		
BLOCK: CONTROL VIRTEX7 CONTROL	SIZE: C	REV.: 26.05.2014	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

ROD

TO KINTEX
TO CPLD

CTRLBUS_P<41..0>
CTRLBUS_N<41..0>
VIRTEX7_CTRL<19..0>

TO ACE_MODUL
ST5
V7_U1_DIN
V7_U1_DOUT
V7_U2_DIN
V7_U2_DOUT

R414 150
R415 150
R416 150
R417 150
R434 150
R435 150
R436 150
R437 150
R438 150
R439 150

1V8_A
R440 1K
R419 NC

PUDC PIN BB27

U1 I26

AT30	IO_0_VRN_14	VCCO_14_1	AL27
BC27	IO_L1P_T0_D00_MOSI_14	VCCO_14_2	AP28
BD27	IO_L1N_T0_D01_DIN_14	VCCO_14_3	AU29
BD29	IO_L2P_T0_D02_14	VCCO_14_4	AY30
BD30	IO_L2N_T0_D03_14	VCCO_14_5	BA27
BB27	IO_L3P_T0_DQS_PUDC_B_VREF_14	VCCO_14_6	BD28
BB28	IO_L3N_T0_DQS_EMCCLK_14		
BB30	IO_L4P_T0_D04_14		
BC30	IO_L4N_T0_D05_14		
BC28	IO_L5P_T0_D06_14		
BC29	IO_L5N_T0_D07_14		
BA29	IO_L6P_T0_FCS_B_14		
BA30	IO_L6N_T0_D08_VREF_14		
AW29	IO_L7P_T1_D09_14		
AY29	IO_L7N_T1_D10_14		
AW27	IO_L8P_T1_D11_14		
AY27	IO_L8N_T1_D12_14		
AY31	IO_L9P_T1_DQS_14		
BA31	IO_L9N_T1_DQS_D13_14		
AY28	IO_L10P_T1_D14_14		
BA28	IO_L10N_T1_D15_14		
AW30	IO_L11P_T1_SRCC_14		
AW31	IO_L11N_T1_SRCC_14		
AV27	IO_L12P_T1_MRCC_14		
AV28	IO_L12N_T1_MRCC_14		
AU30	IO_L13P_T2_MRCC_14		
AV30	IO_L13N_T2_MRCC_14		
AU28	IO_L14P_T2_SRCC_14		
AV29	IO_L14N_T2_SRCC_14		
AN27	IO_L15P_T2_DQS_RDWR_B_14		
AP27	IO_L15N_T2_DQS_DOUT_CSO_B_14		
AT28	IO_L16P_T2_CSI_B_14		
A129	IO_L16N_T2_A15_D31_14		
AP29	IO_L17P_T2_A14_D30_14		
AP30	IO_L17N_T2_A13_D29_14		
AR28	IO_L18P_T2_A12_D28_14		
AR29	IO_L18N_T2_A11_D27_14		
AN28	IO_L19P_T3_A10_D26_14		
AN29	IO_L19N_T3_A09_D25_VREF_14		
AM30	IO_L20P_T3_A08_D24_14		
AN30	IO_L20N_T3_A07_D23_14		
AK27	IO_L21P_T3_DQS_14		
AK28	IO_L21N_T3_DQS_A06_D22_14		
AM27	IO_L22P_T3_A05_D21_14		
AM28	IO_L22N_T3_A04_D20_14		
AJ29	IO_L23P_T3_A03_D19_14		
AK29	IO_L23N_T3_A02_D18_14		
AL28	IO_L24P_T3_A01_D17_14		
AL29	IO_L24N_T3_A00_D16_14		
AR27	IO_25_VRP_14		

XC7VX690T_FFG1927

1V8_B
R441 1K
R418 NC

PUDC PIN BB27

U2 I101

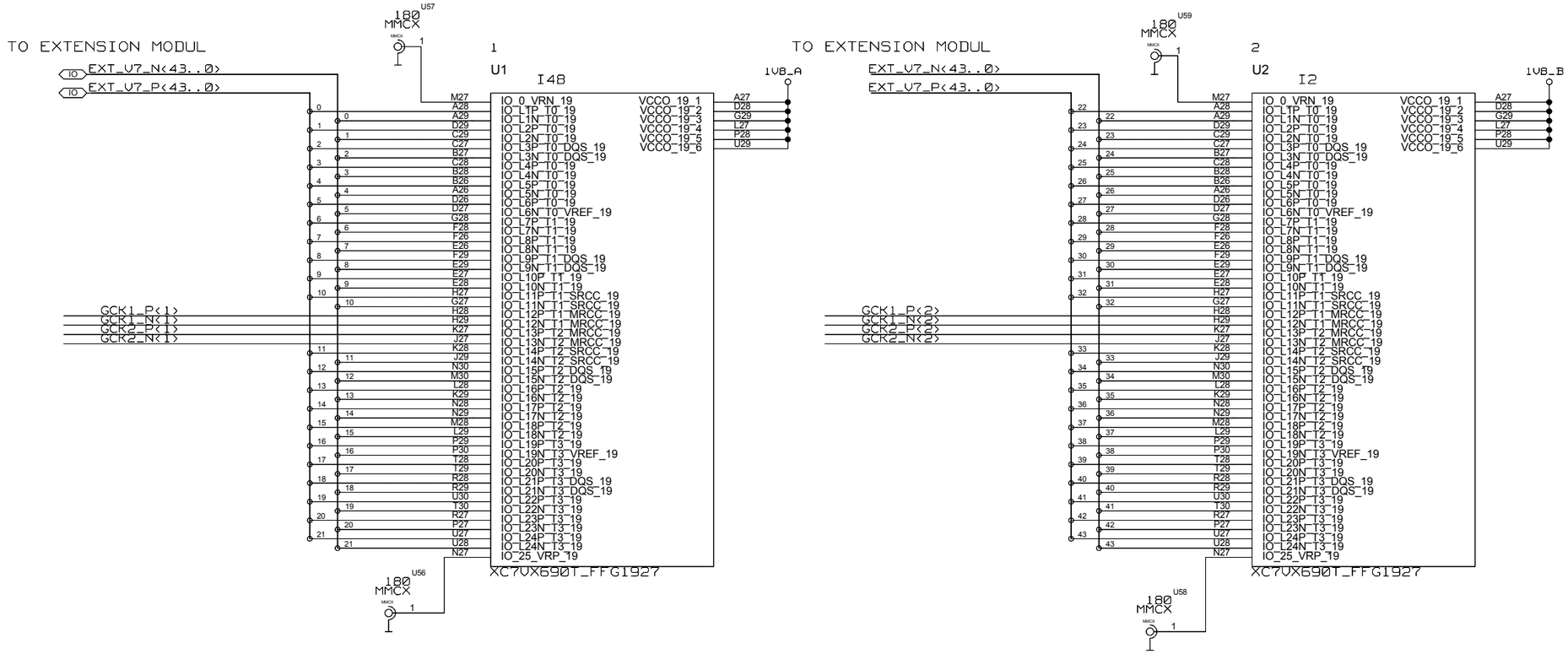
AT30	IO_0_VRN_14	VCCO_14_1	AL27
BC27	IO_L1P_T0_D00_MOSI_14	VCCO_14_2	AP28
BD27	IO_L1N_T0_D01_DIN_14	VCCO_14_3	AU29
BD29	IO_L2P_T0_D02_14	VCCO_14_4	AY30
BD30	IO_L2N_T0_D03_14	VCCO_14_5	BA27
BB27	IO_L3P_T0_DQS_PUDC_B_VREF_14	VCCO_14_6	BD28
BB28	IO_L3N_T0_DQS_EMCCLK_14		
BB30	IO_L4P_T0_D04_14		
BC30	IO_L4N_T0_D05_14		
BC28	IO_L5P_T0_D06_14		
BC29	IO_L5N_T0_D07_14		
BA29	IO_L6P_T0_FCS_B_14		
BA30	IO_L6N_T0_D08_VREF_14		
AW29	IO_L7P_T1_D09_14		
AY29	IO_L7N_T1_D10_14		
AW27	IO_L8P_T1_D11_14		
AY27	IO_L8N_T1_D12_14		
AY31	IO_L9P_T1_DQS_14		
BA31	IO_L9N_T1_DQS_D13_14		
AY28	IO_L10P_T1_D14_14		
BA28	IO_L10N_T1_D15_14		
AW30	IO_L11P_T1_SRCC_14		
AW31	IO_L11N_T1_SRCC_14		
AV27	IO_L12P_T1_MRCC_14		
AV28	IO_L12N_T1_MRCC_14		
AU30	IO_L13P_T2_MRCC_14		
AV30	IO_L13N_T2_MRCC_14		
AU28	IO_L14P_T2_SRCC_14		
AV29	IO_L14N_T2_SRCC_14		
AN27	IO_L15P_T2_DQS_RDWR_B_14		
AP27	IO_L15N_T2_DQS_DOUT_CSO_B_14		
AT28	IO_L16P_T2_CSI_B_14		
A129	IO_L16N_T2_A15_D31_14		
AP29	IO_L17P_T2_A14_D30_14		
AP30	IO_L17N_T2_A13_D29_14		
AR28	IO_L18P_T2_A12_D28_14		
AR29	IO_L18N_T2_A11_D27_14		
AN28	IO_L19P_T3_A10_D26_14		
AN29	IO_L19N_T3_A09_D25_VREF_14		
AM30	IO_L20P_T3_A08_D24_14		
AN30	IO_L20N_T3_A07_D23_14		
AK27	IO_L21P_T3_DQS_14		
AK28	IO_L21N_T3_DQS_A06_D22_14		
AM27	IO_L22P_T3_A05_D21_14		
AM28	IO_L22N_T3_A04_D20_14		
AJ29	IO_L23P_T3_A03_D19_14		
AK29	IO_L23N_T3_A02_D18_14		
AL28	IO_L24P_T3_A01_D17_14		
AL29	IO_L24N_T3_A00_D16_14		
AR27	IO_25_VRP_14		

XC7VX690T_FFG1927

UNIVERSITY OF MAINZ	DRAWING TITLE: U1+U2 CONTROLBUS --> CPLD U1+U2 RODBUS --> KINTEX7 U1+U2 --> ACE_MODUL	
BLOCK: CONTROL VIRTEX7 CONTROL	SIZE: C	REV.: 26.05.2014
	SCALE:	SHEET OF

DRAWING NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

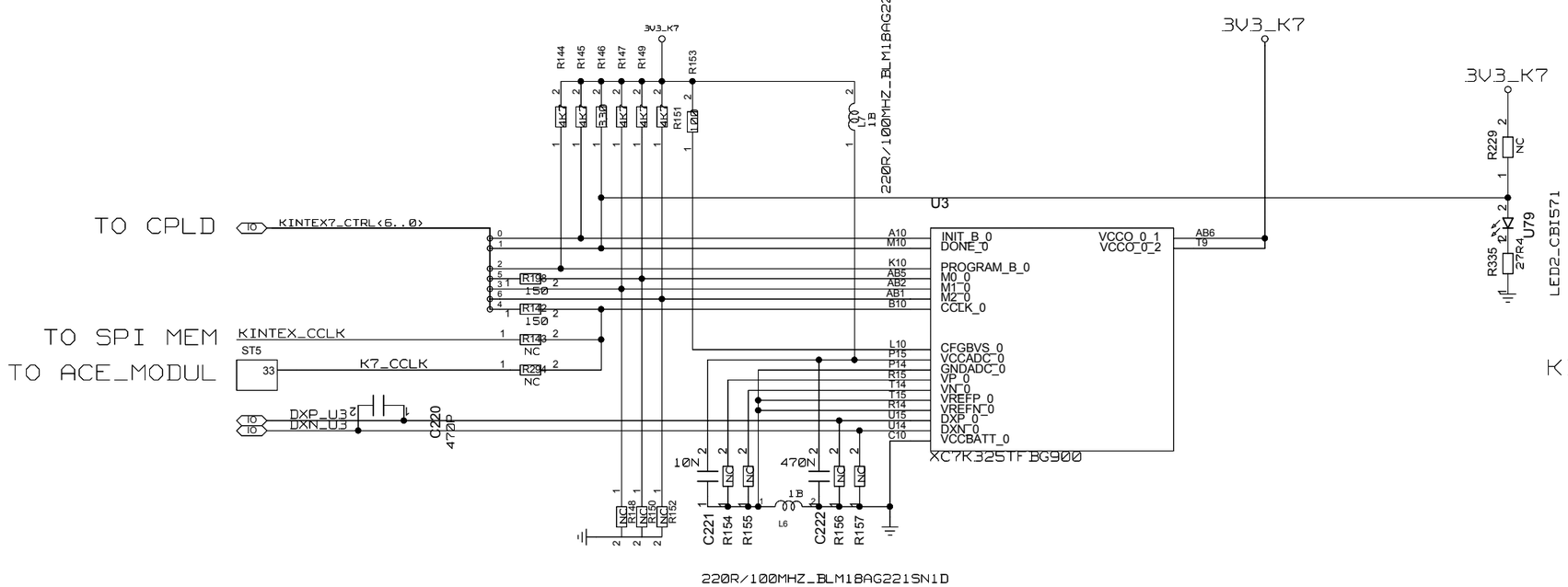


IN GCK1_P<2..1>
IN GCK1_N<2..1>

IN GCK2_P<2..1>
IN GCK2_N<2..1>

UNIVERSITY OF MAINZ	DRAWING TITLE: VIRTEX7 TO EXTENSION MODUL VIRTEX7 GCK	
BLOCK: CONTROL VIRTEX7 CONTROL	SIZE: C	REV. / DRAWING NO.
	SCALE	SHEET OF

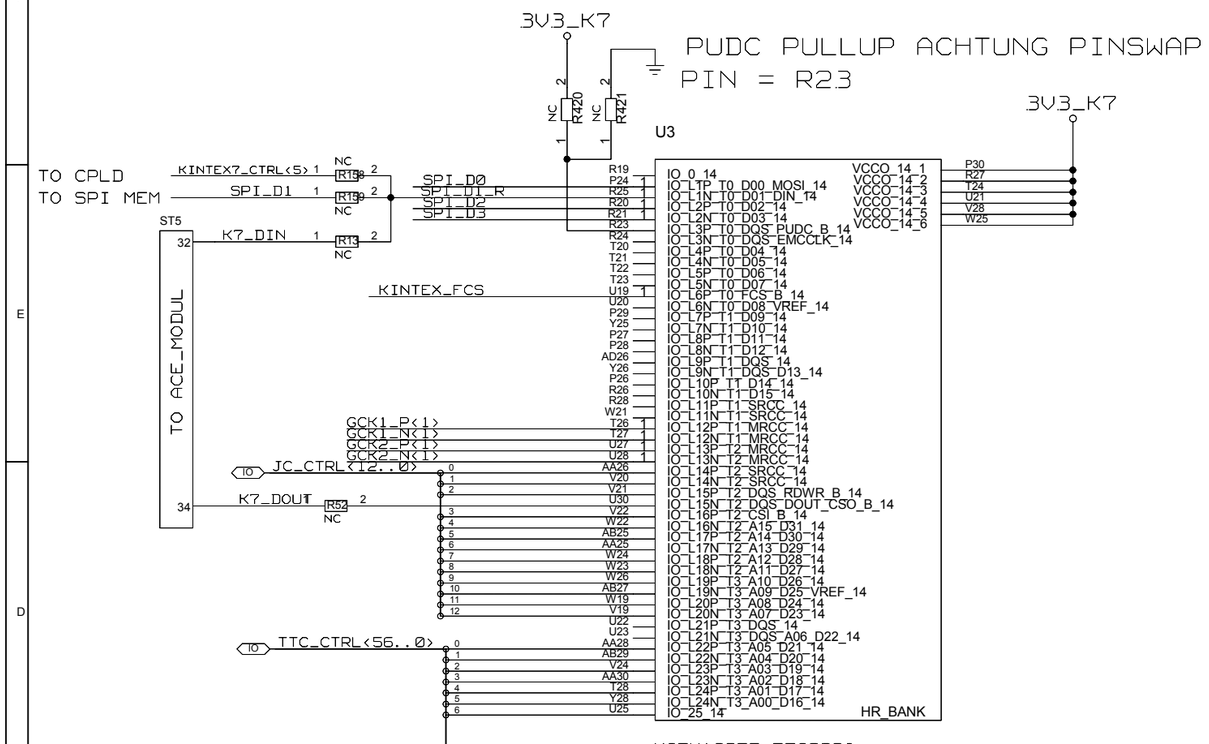
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

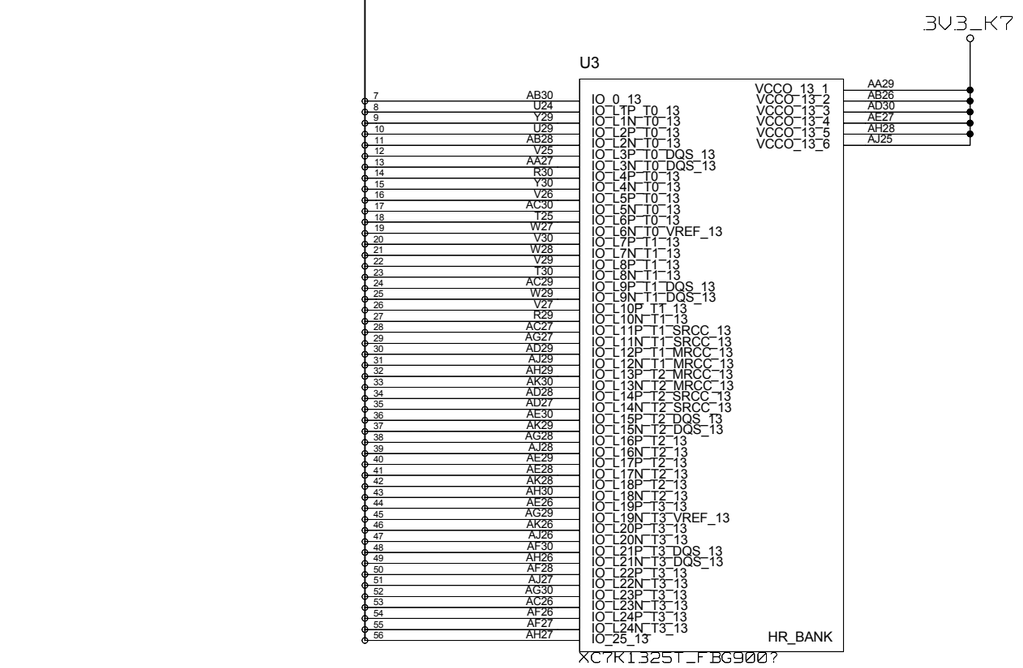


UNIVERSITY OF MAINZ		DRAWING TITLE: KINTEX CONTROL	
BLOCK: CONTROL KINTEX7 CONTROL		SIZE: C	REV. / DRAWING NO.
		SCALE	SHEET OF

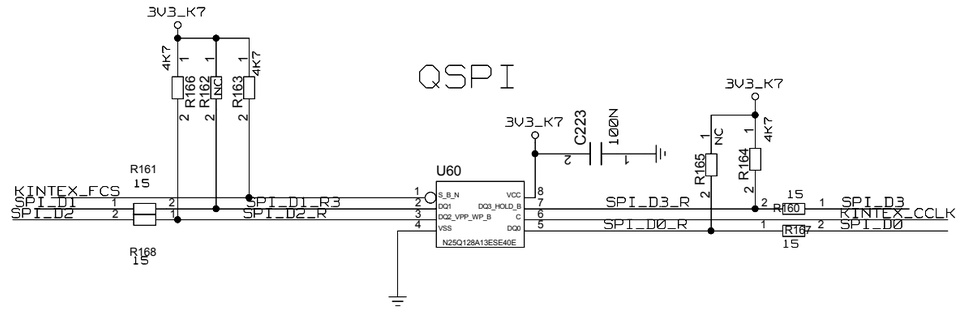
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HIGH RANGE BANKS





BANK14 VCCO ABHAENGIG VON SPI SPANNUNG

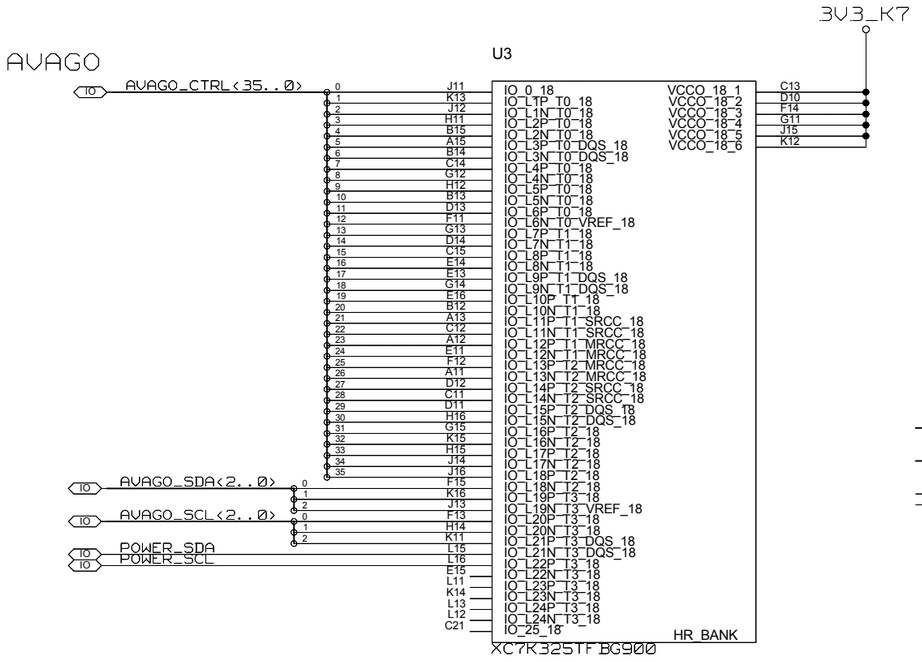


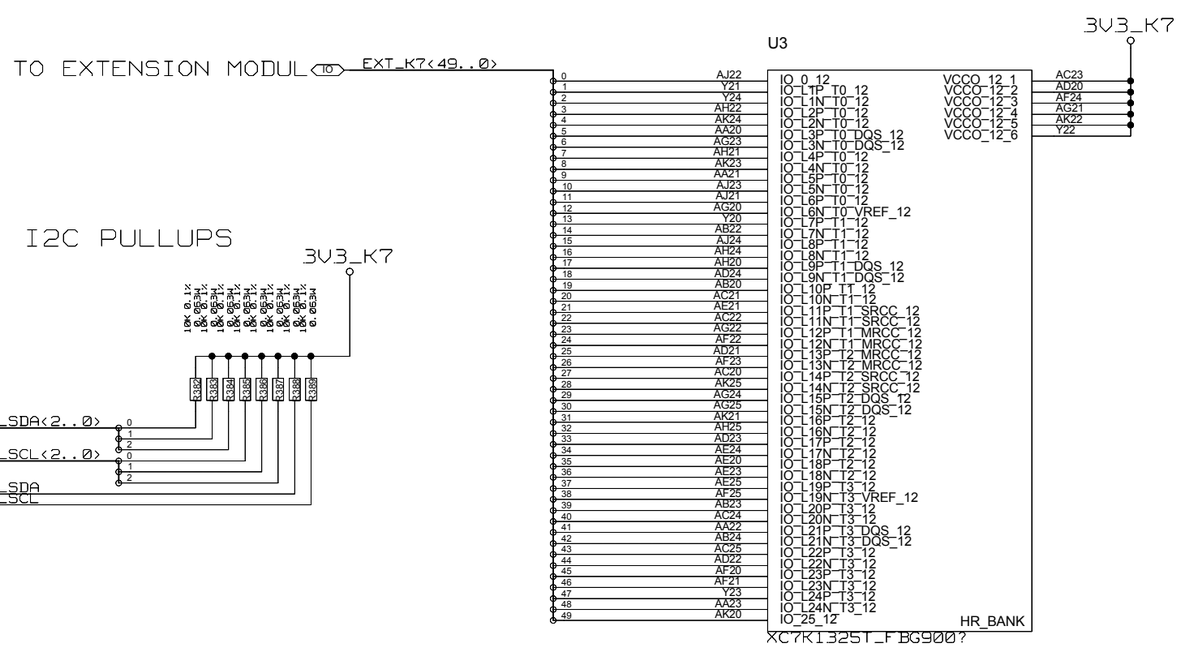
GCK1_P<2..1>
GCK1_N<2..1>
GCK2_P<2..1>
GCK2_N<2..1>

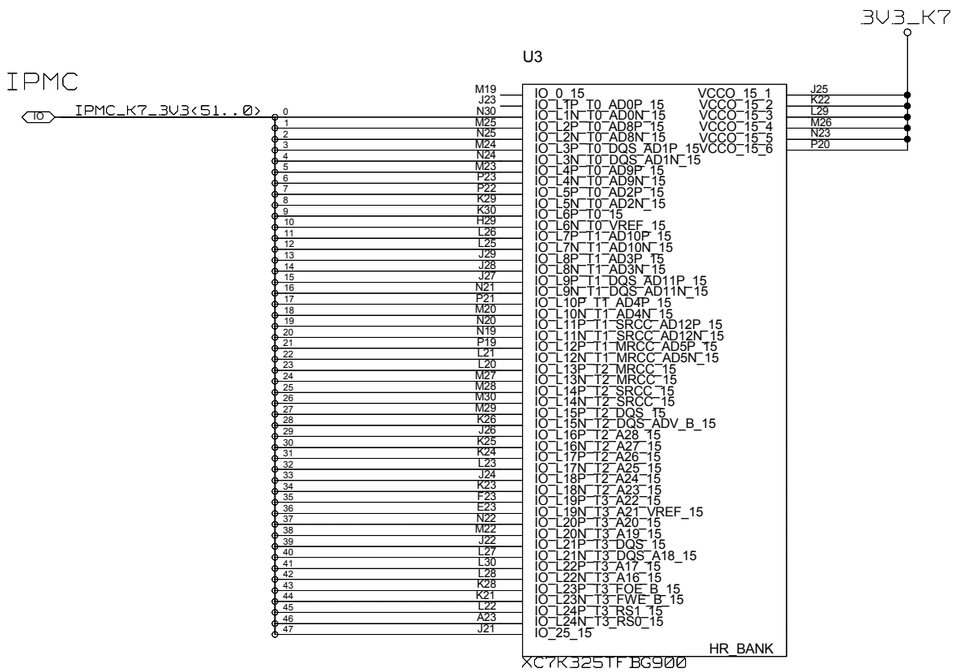
UNIVERSITY OF MAINZ	DRAWING TITLE: SD, JITTERCLEANER, TTC, QSPI CONTROL		
BLOCK: CONTROL KINTEX7 CONTROL	SIZE C	REV. 03.06.2014	DRAWING NO.
	SCALE		SHEET OF

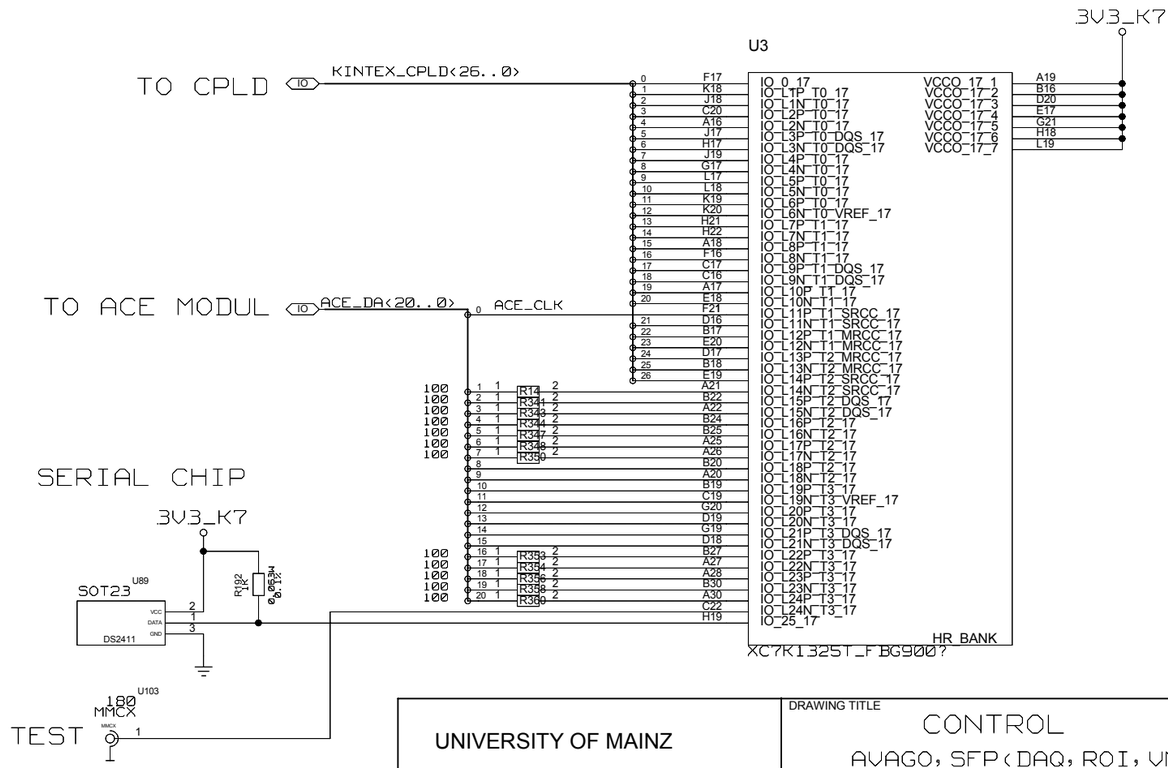
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HIGH RANGE BANKS





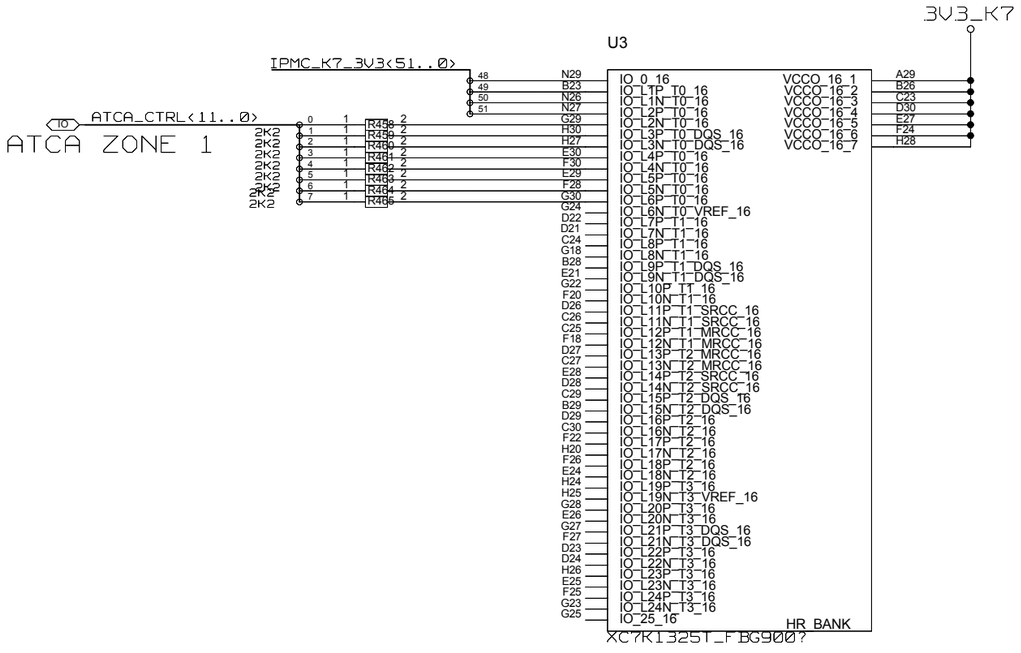




UNIVERSITY OF MAINZ	DRAWING TITLE: CONTROL AVAGO, SFP(DAQ, ROI, VME)		
BLOCK: CONTROL KINTEX7 CONTROL	SIZE: C	REV.: 03.06.2014	DRAWING NO.
	SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HIGH RANGE BANKS



UNIVERSITY OF MAINZ	DRAWING TITLE		
BLOCK: CONTROL KINTEX7 CONTROL	SIZE C	REV.	DRAWING NO.
	SCALE		SHEET OF

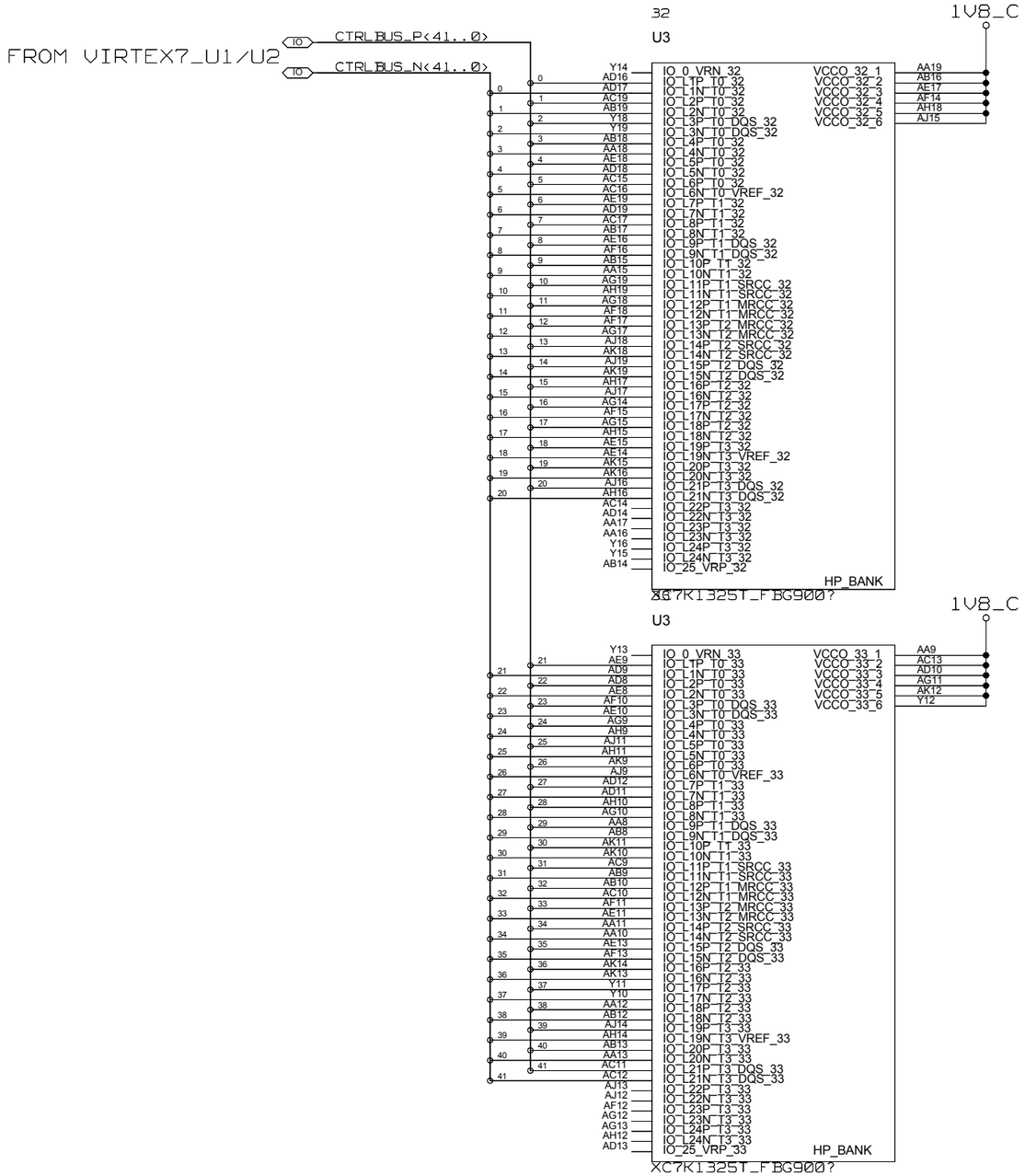
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HIGH PERFORMACE BANKS 32, 33, 34

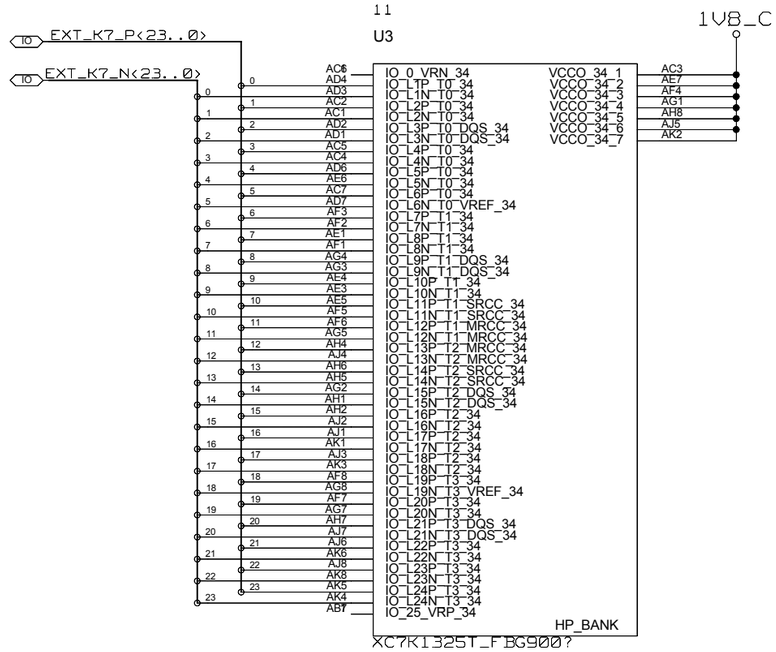
ROD BUS

PINSWAP ONLY INSIDE SAME BANK

FROM VIRTEX7_U1/U2



TO EXTENSION MODUL



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ZONE	LTR	DESCRIPTION	DATE	APPR.

XC2C256_FG256

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3V3

U16

C230 100N

VCC GND OUT CONTROL

KC5032A_20MHZ

R179 51

R180 162

100MHZ

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TTC_SUB1
TTC_DOUT6
TTC_DOUT7
TTC_RESET

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IN TTC_DETECT

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CLOCK MUX

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OI KINTEX_CPLD<26..0>

ATCA ZONE 1

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R466 R467 R468 R469 R470 R471 R472 R473 2

J4

JTAG_USB

VREF TDI TDO TMS TCK

CONNECTOR

3V3 FUSE2

POLYFUSE 300MA

R11 A10 N12 P12

TDI TDO TMS TCK

XC2C256

U5

xc2c256_FT256

XC2C256

1V8_CPLD 3V3

F4

VCCAUX
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VCCIO1[7..0]
VCCIO2[6..0]
GND[19..0]

U5

XC2C256

xc2c256_FT256

1V8_CPLD

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10N

U37

3V3

C238 C239 C240 C241 C242 C243 C244 C245 C246

10N

U37

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LEVELTRANSLATOR

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IN

U11

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SN74AVC4T774

TSSOP16

SN74AVC4T774PW_TSSOP16

C159 100N 3V3

C168 100N 2V5

U13

SN74AVC4T774PW_TSSOP16

C166 100N 3V3

C186 100N 2V5

U68

SN74AVC4T774PW_TSSOP16

C167 100N 3V3

C187 100N 2V5

VCC=3V3

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NC

SN74AHC1G14

C247 100N

C248 NC

R182

R183 51

100MHZ

R184 162

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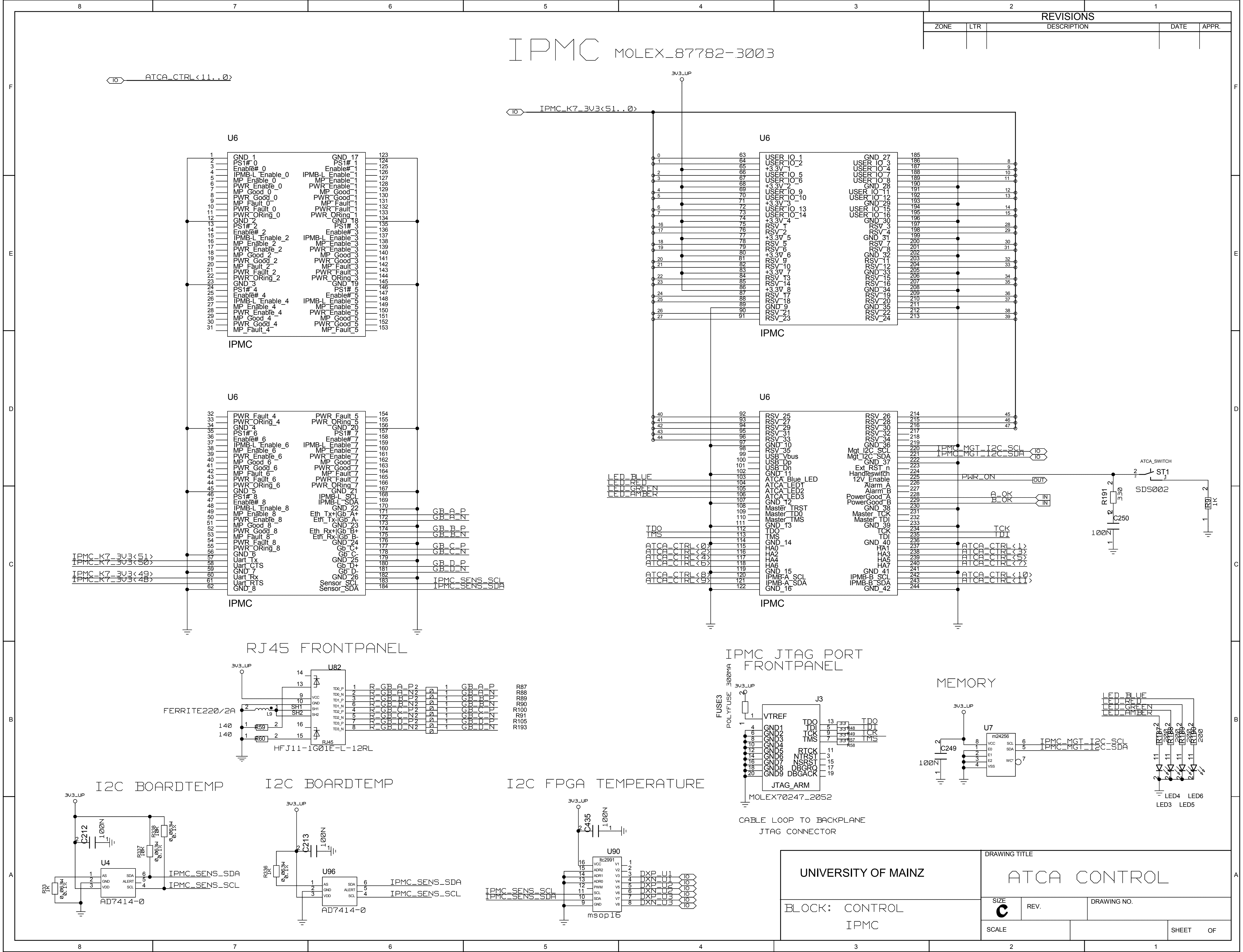
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U6
IPMC
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U82
FERRITE220/2A
HFJ11-1G01E-L-12RL
IPMC JTAG PORT
FRONTPANEL
FUSE3
POLYFUSE 300MA
J3
JTAG_ARM
MOLEX70247_2052
CABLE LOOP TO BACKPLANE
JTAG CONNECTOR
MEMORY
U7
m24256
IPMC_MGT_I2C_SCL
IPMC_MGT_I2C_SDA
LED_BLUE
LED_RED
LED_GREEN
LED_AMBER
ATCA_SWITCH
SDS002
I2C BOARDTEMP
U4
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I2C BOARDTEMP
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I2C FPGA TEMPERATURE
U90
ltc2991
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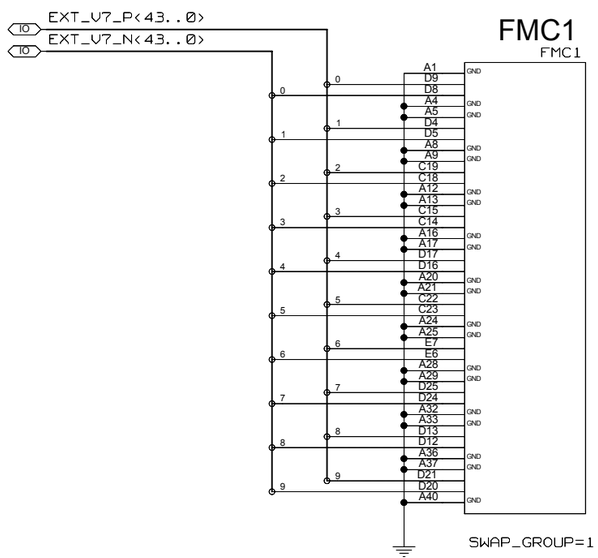

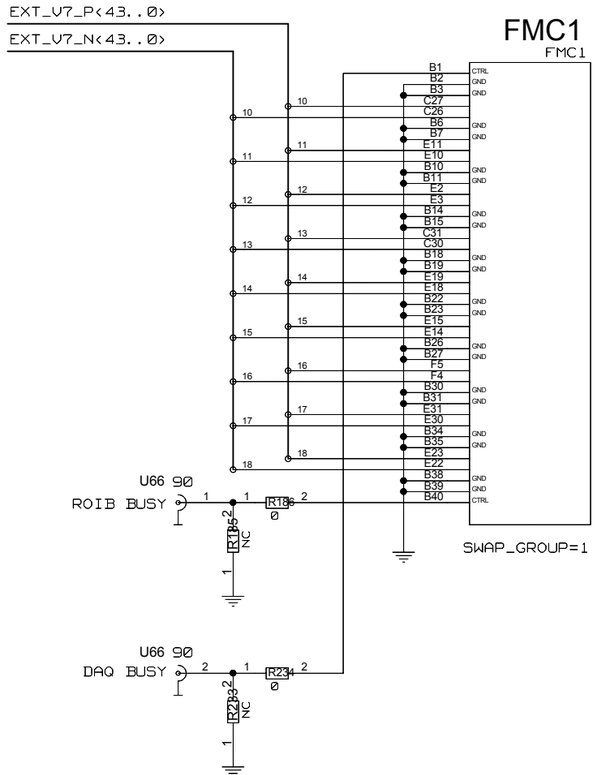

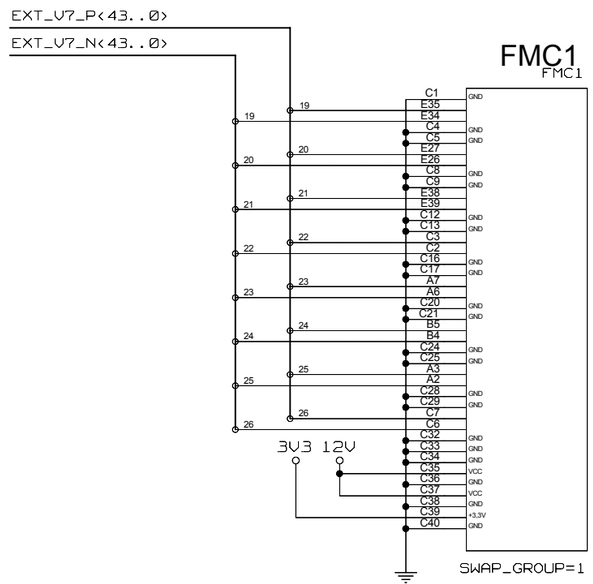

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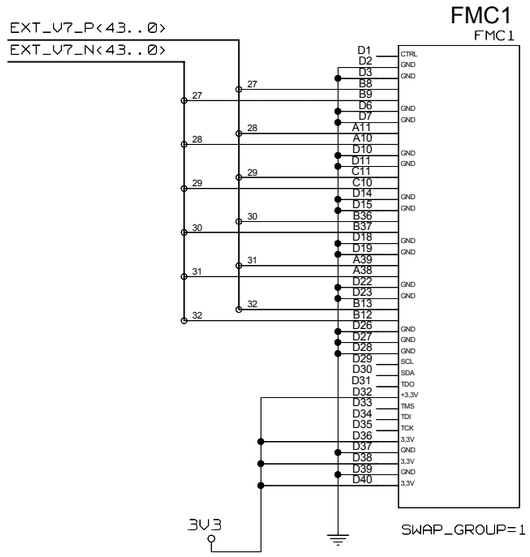

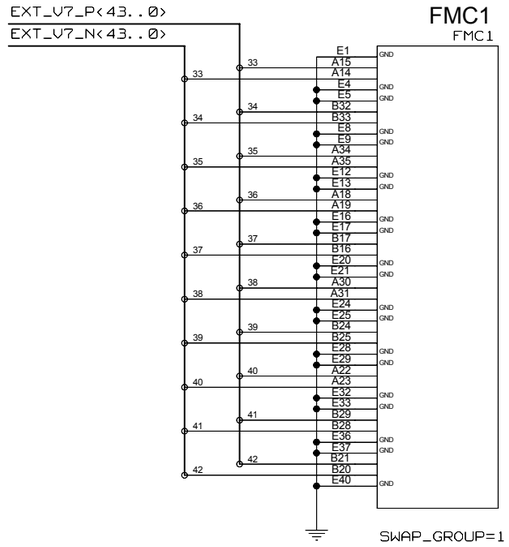

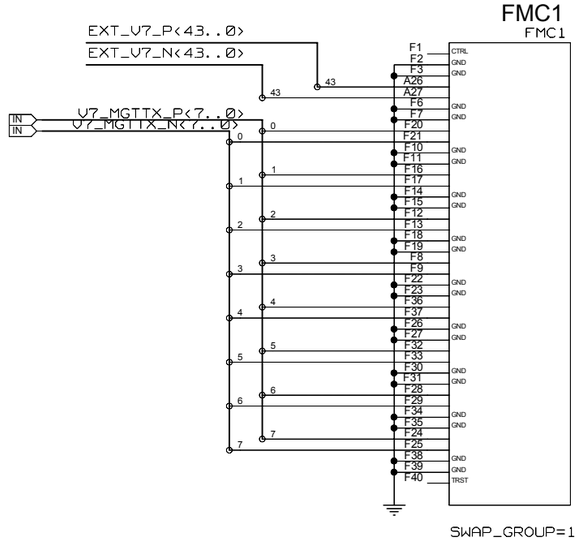

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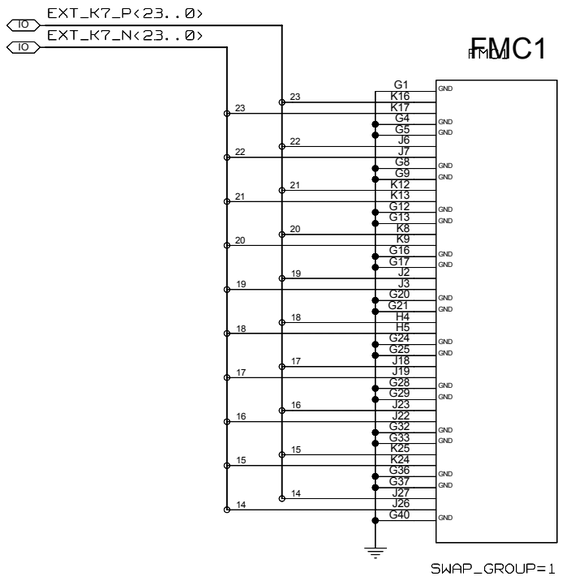

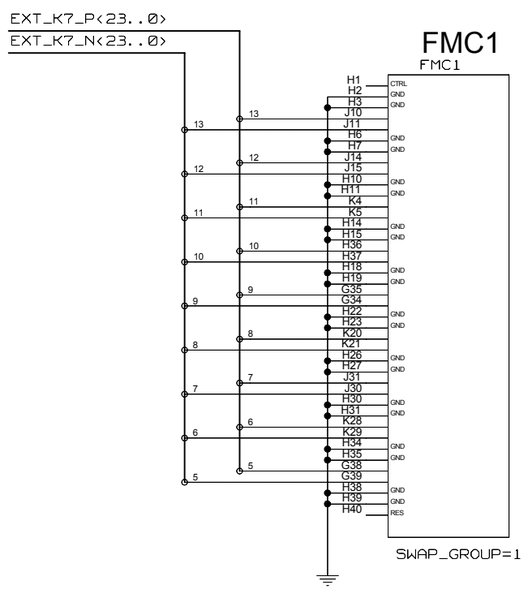

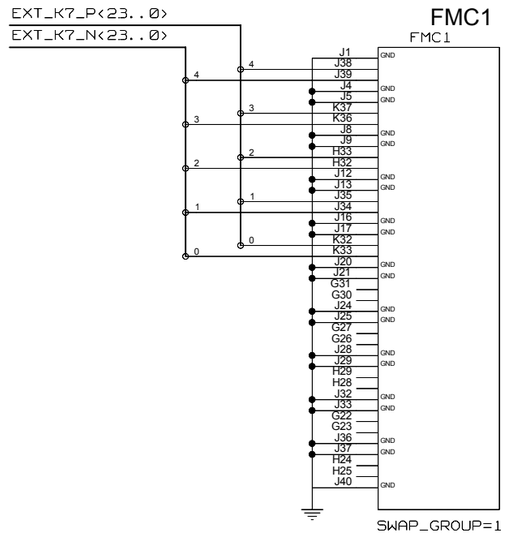

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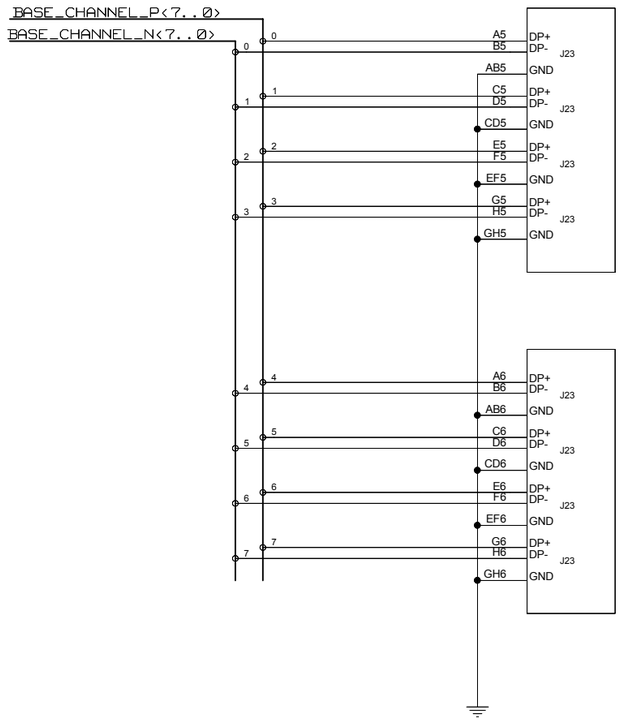

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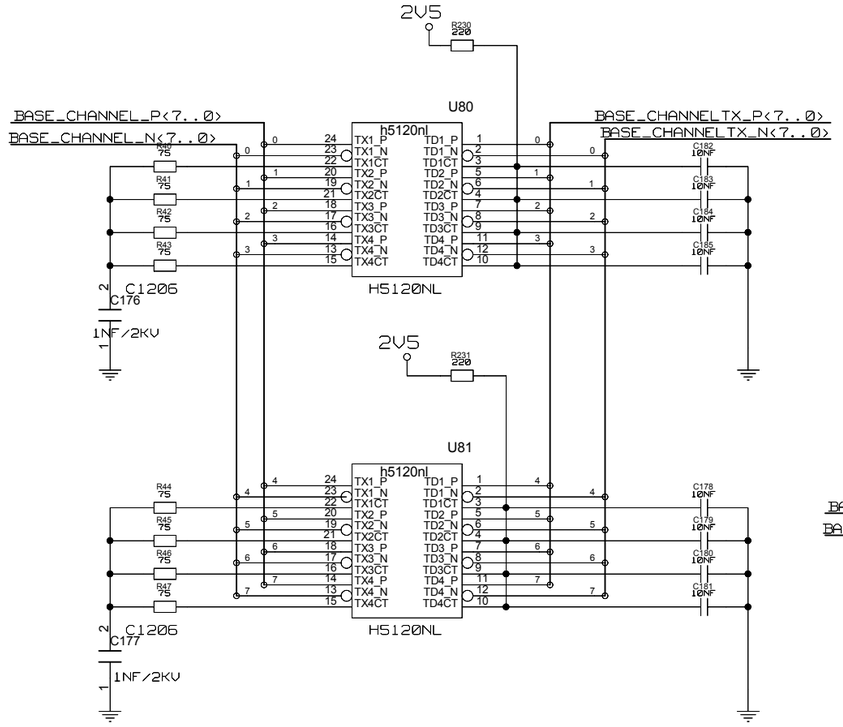

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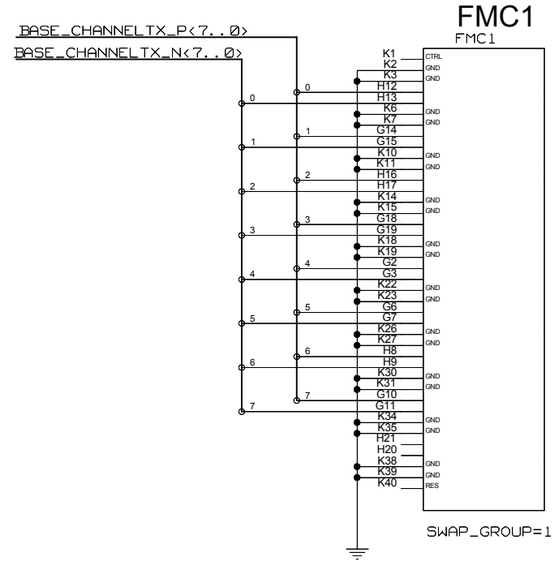

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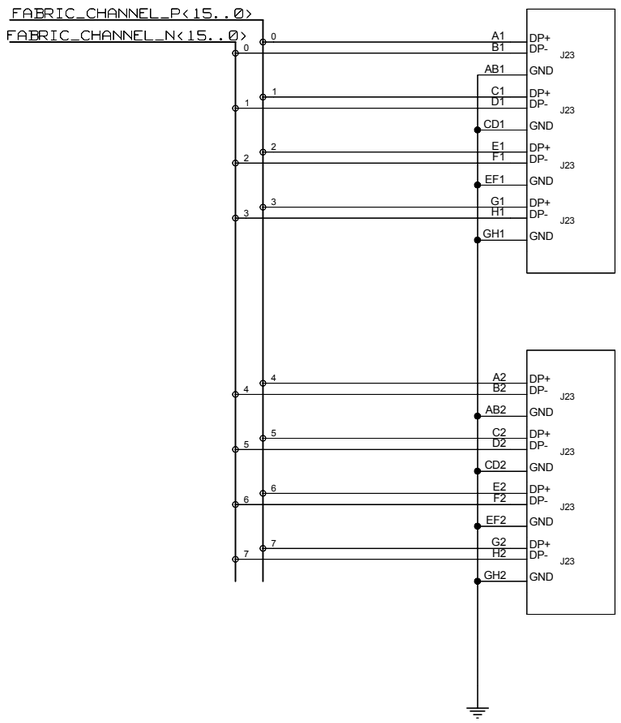

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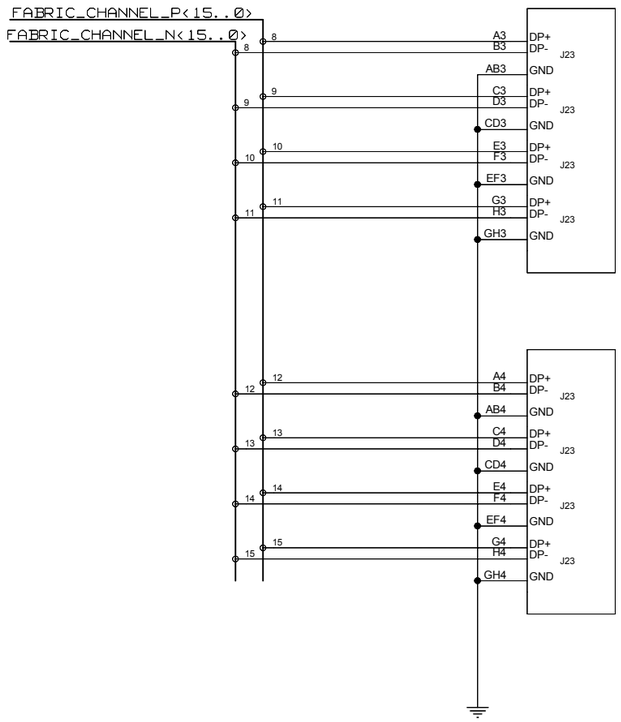

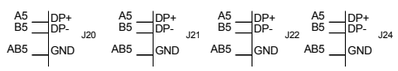

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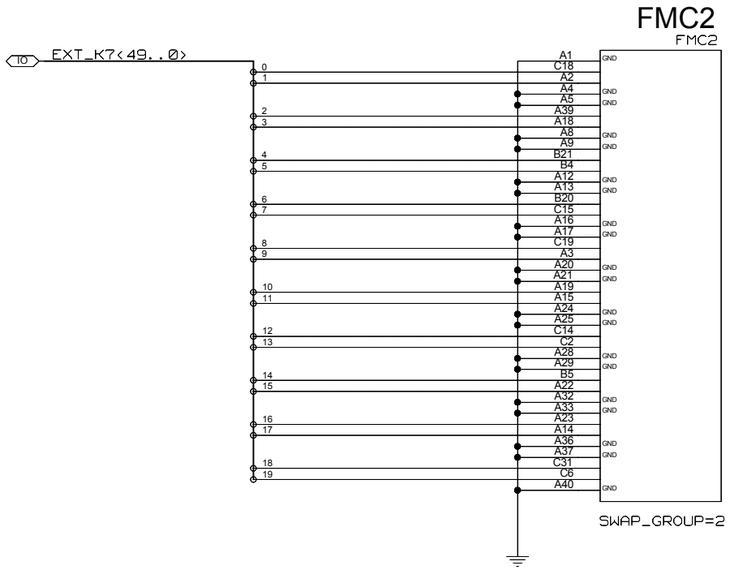

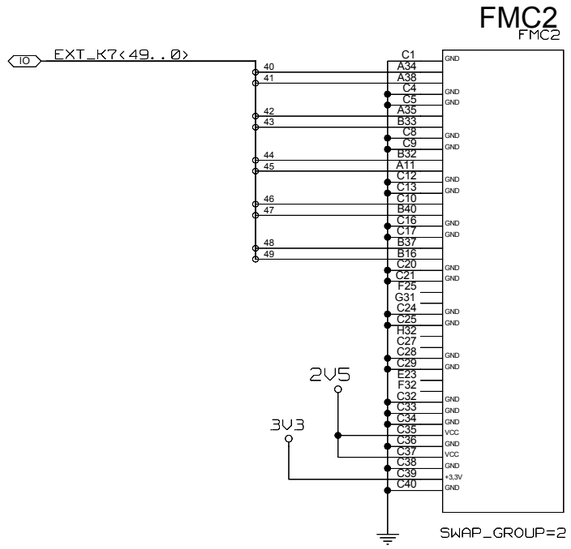

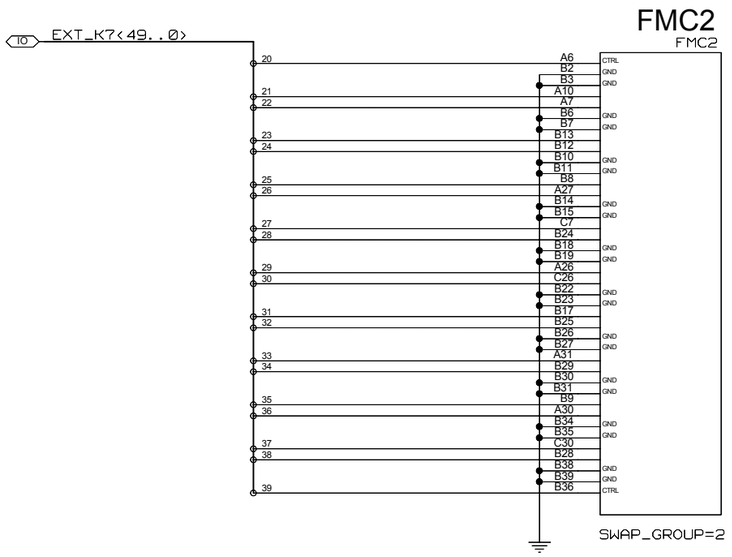

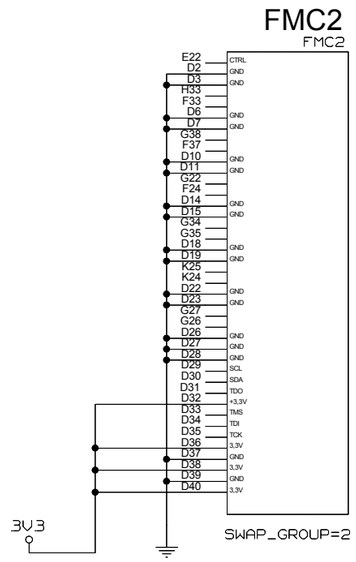

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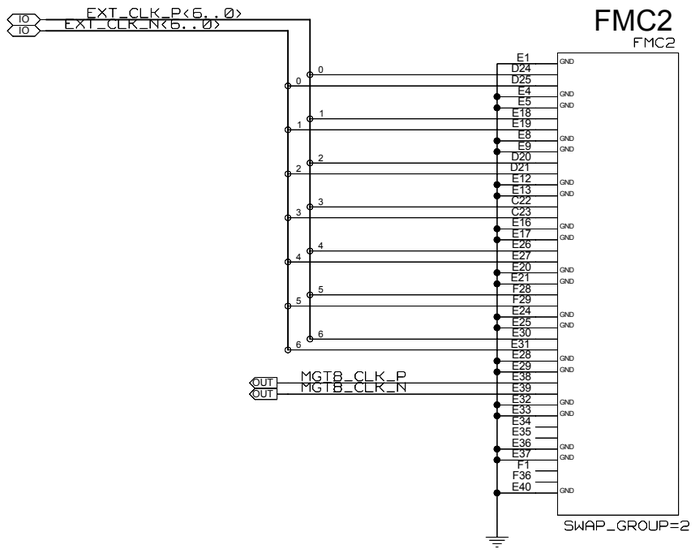

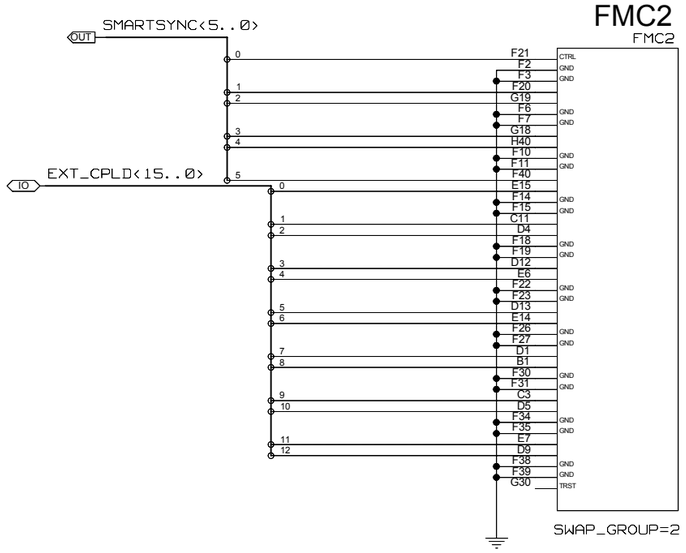

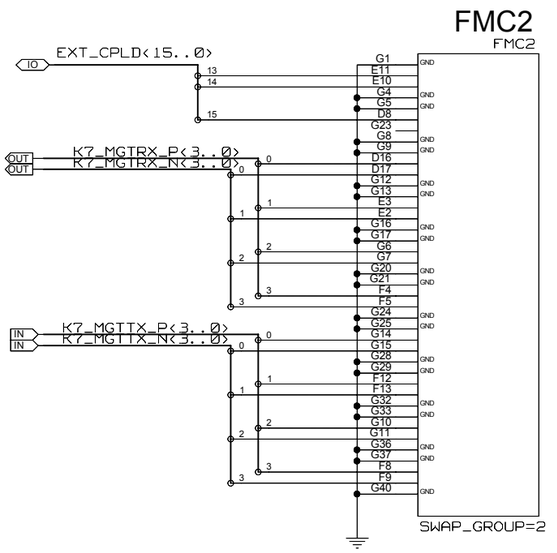

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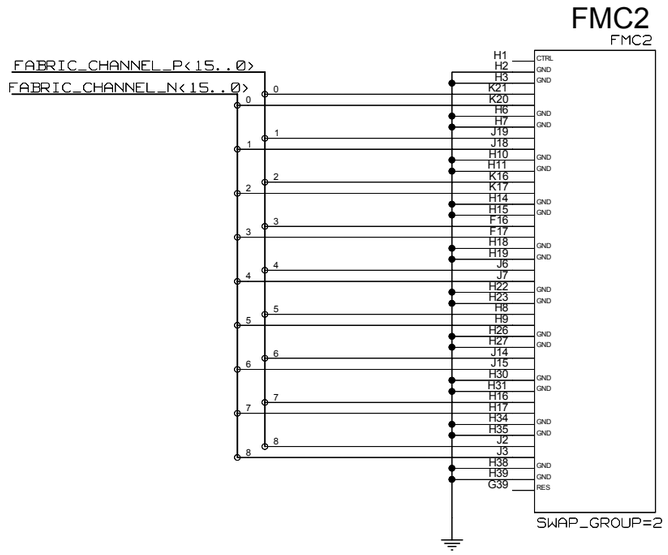

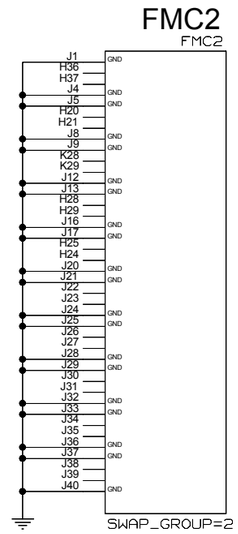

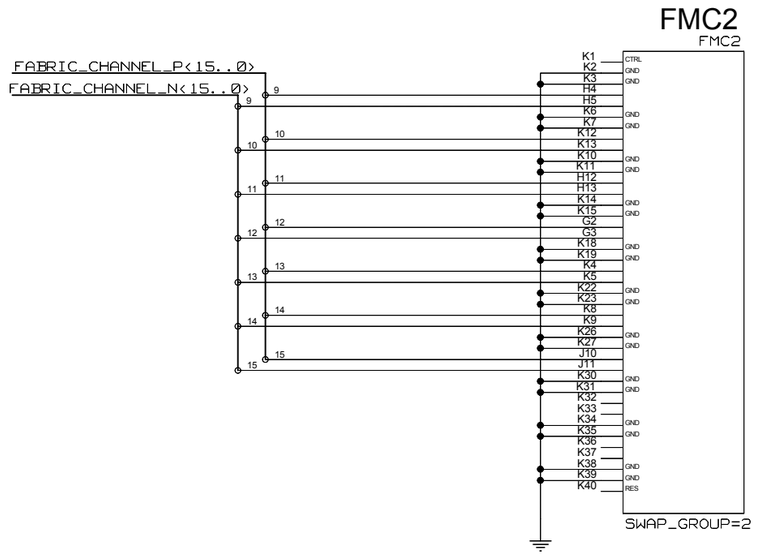

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