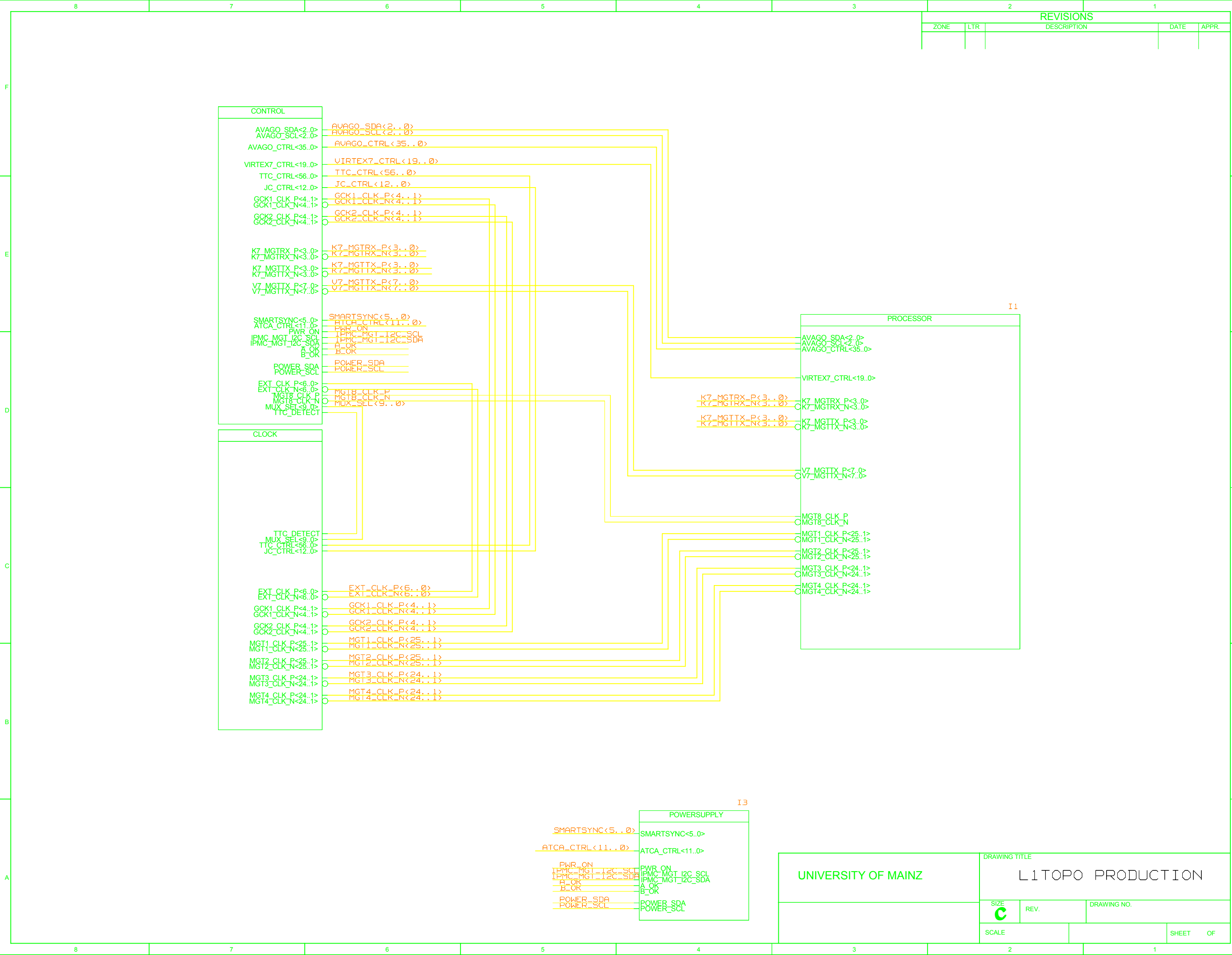
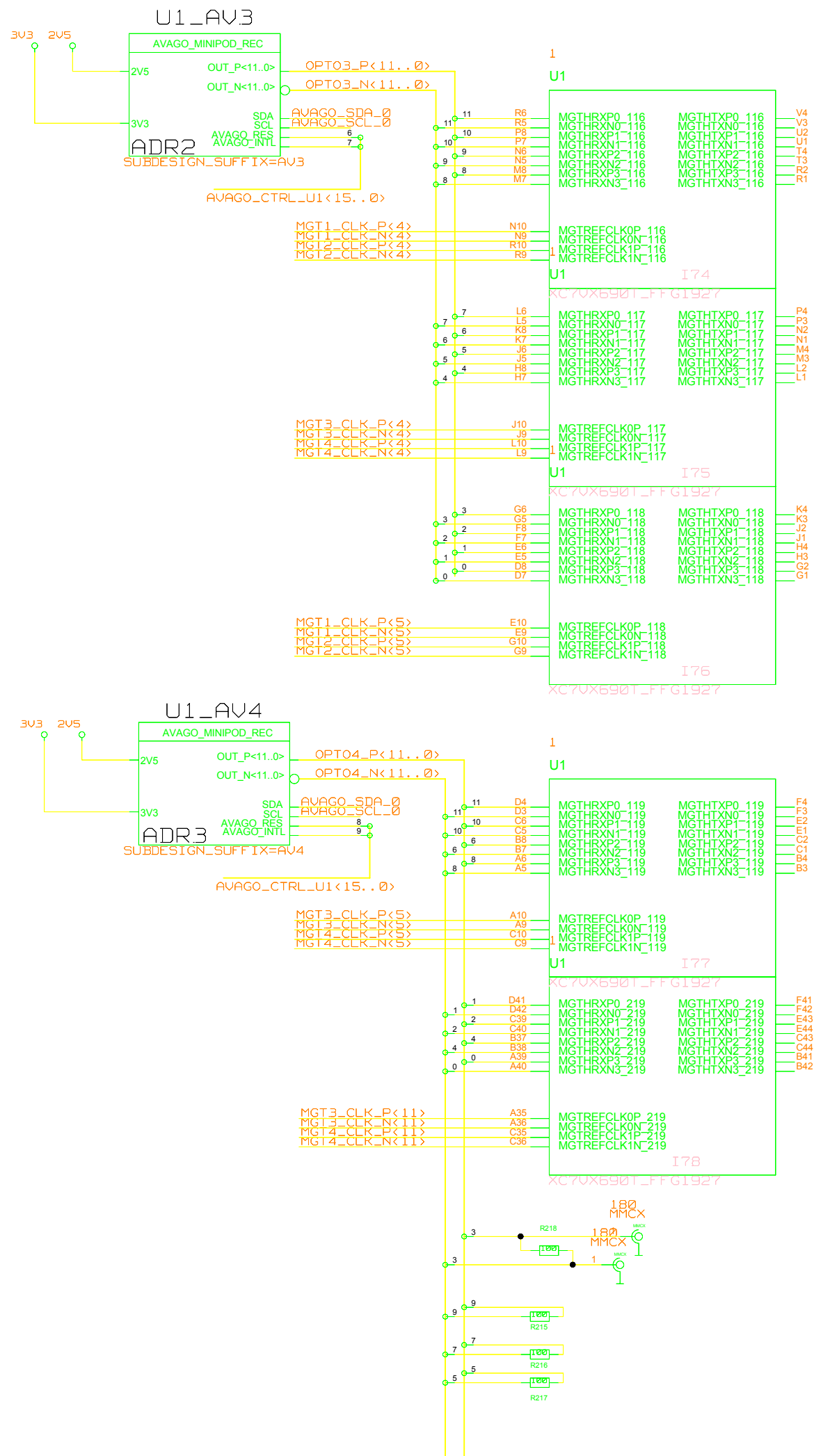
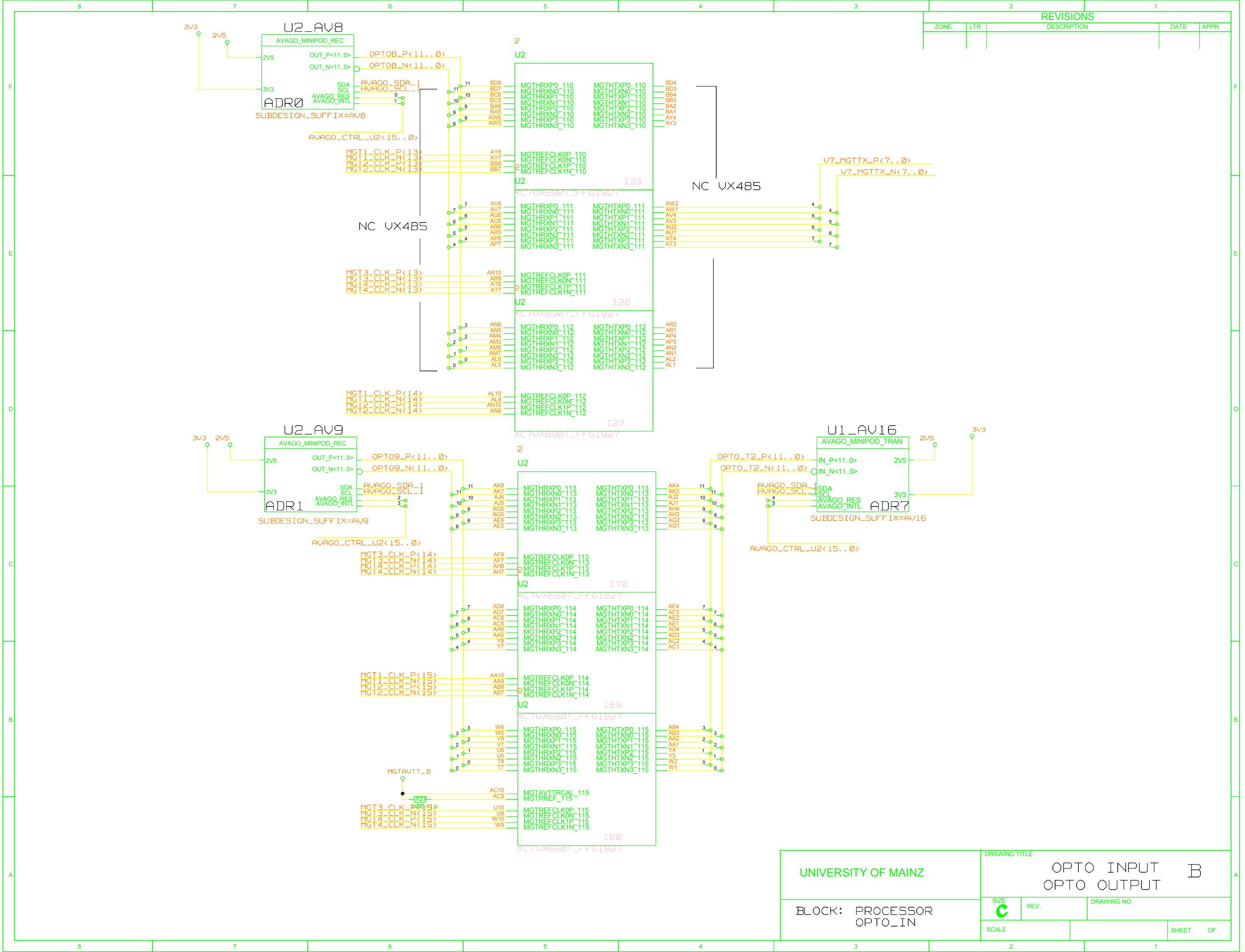


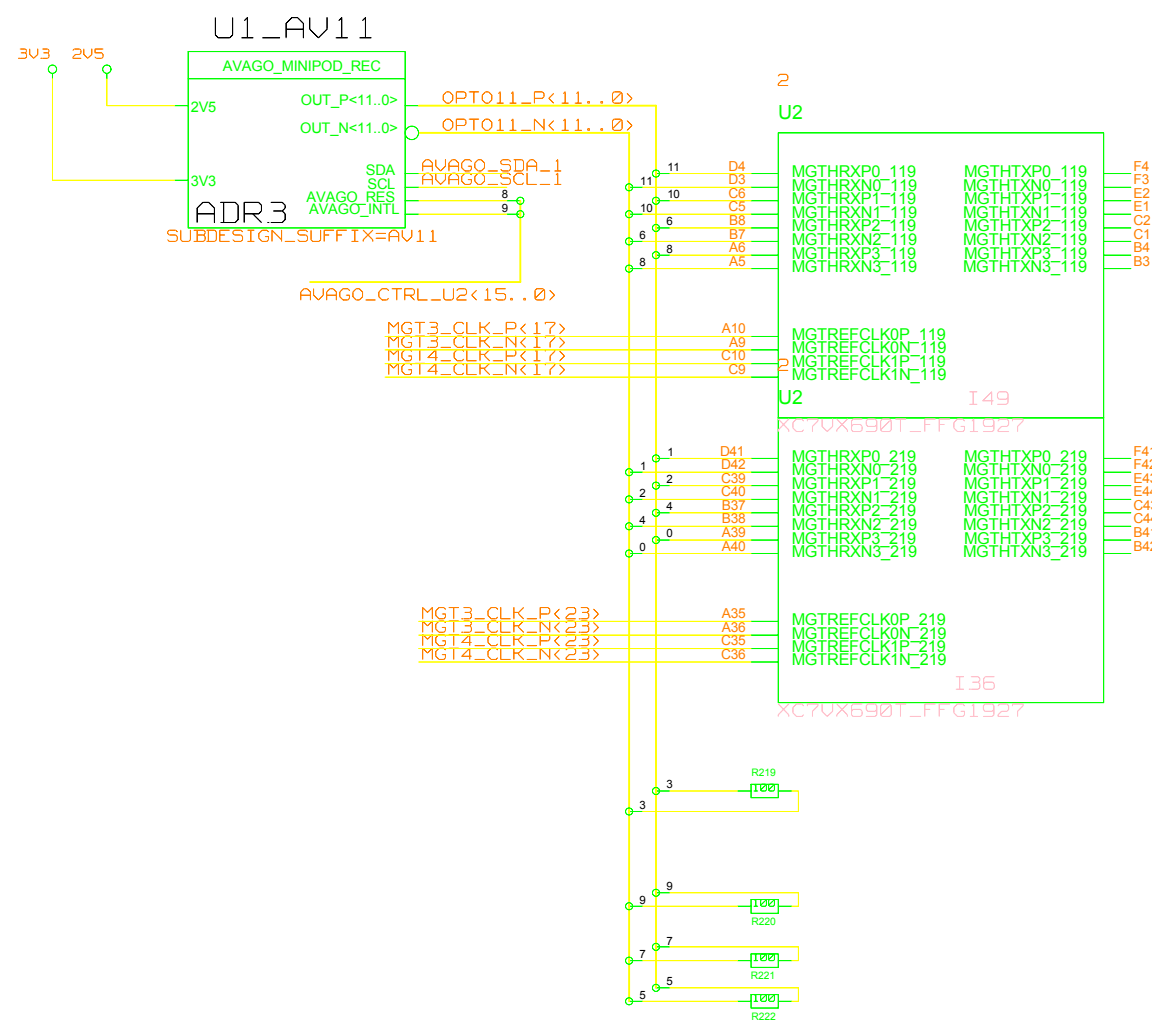
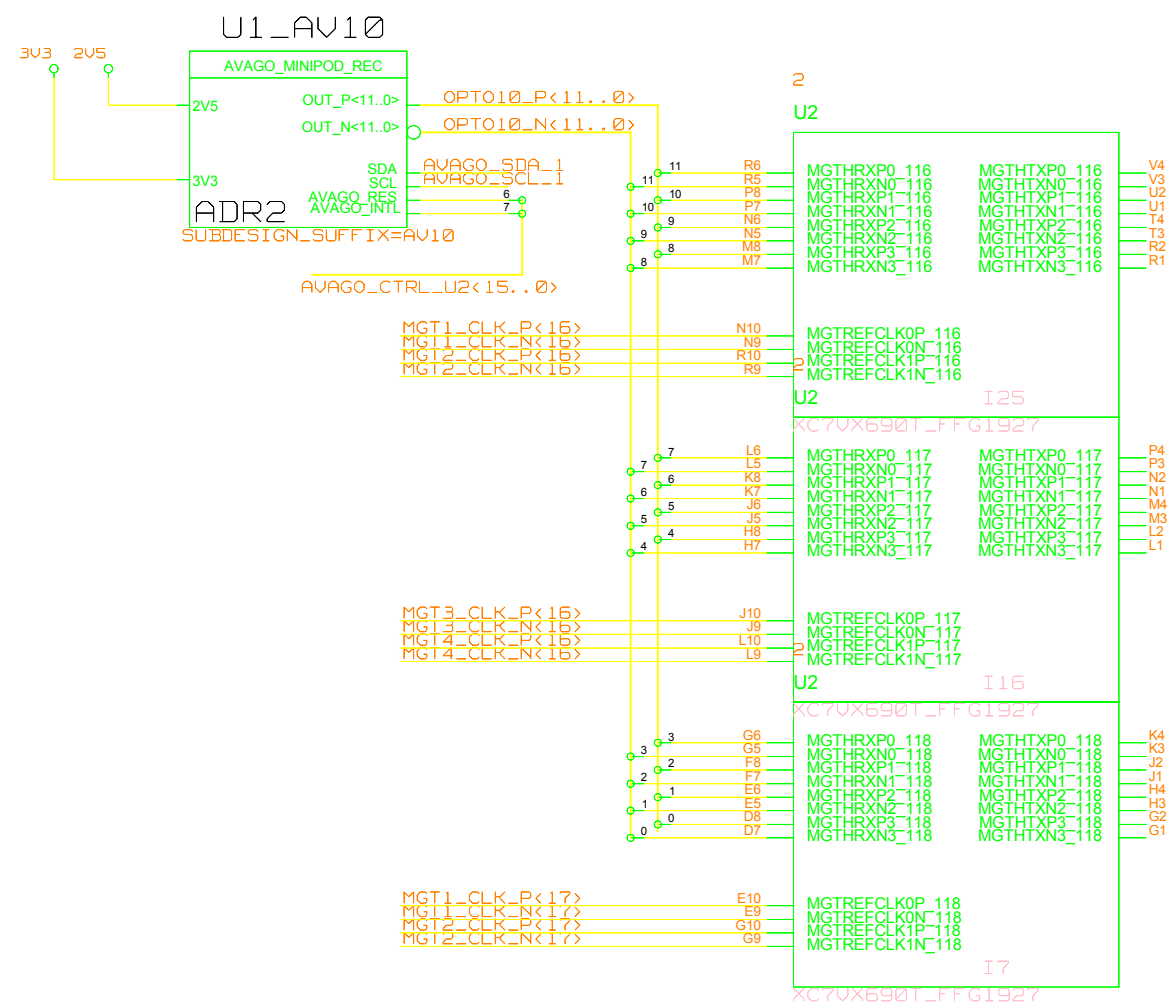




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ZONE	LTR	DESCRIPTION	DATE	APPR.

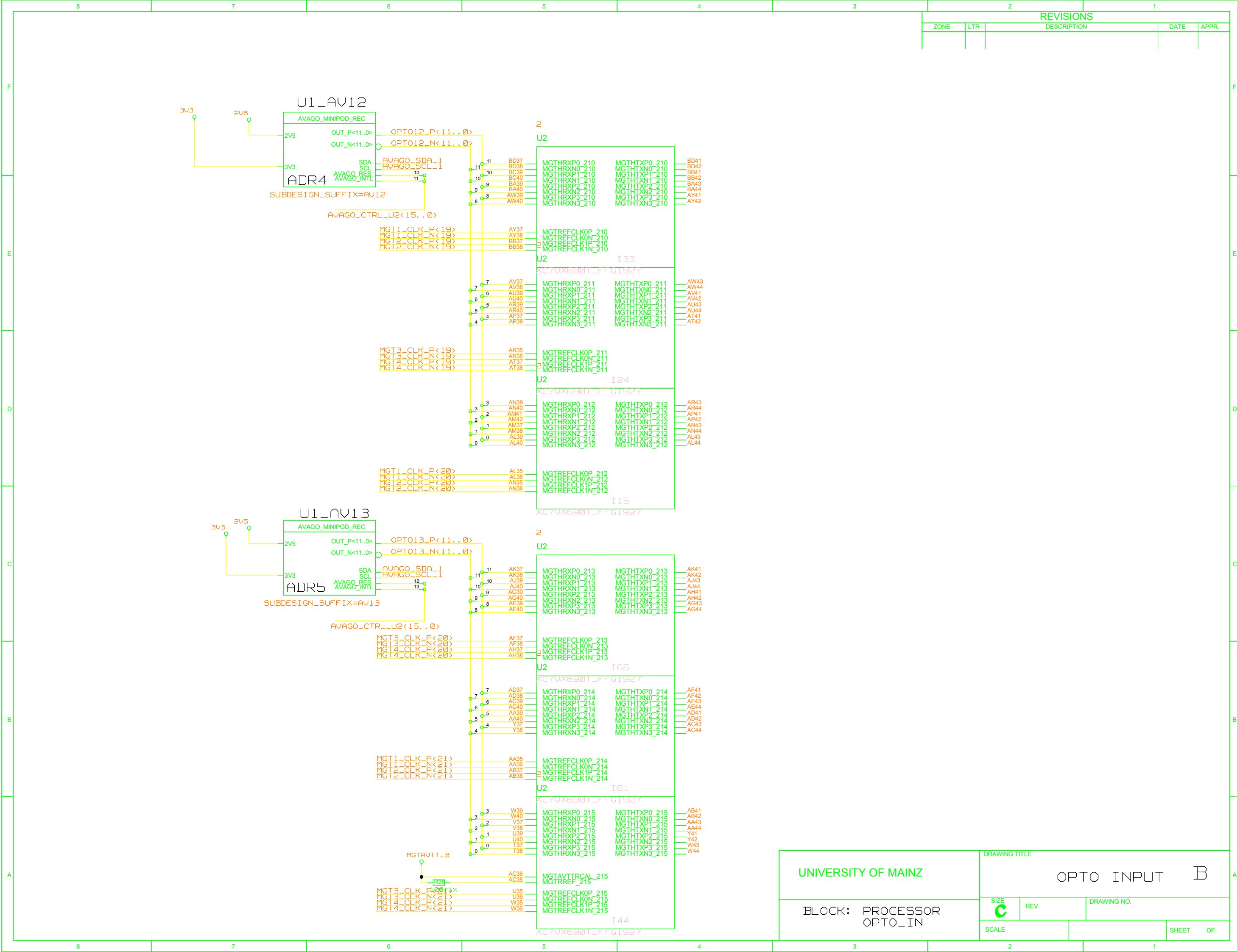
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	SCALE		SHEET OF

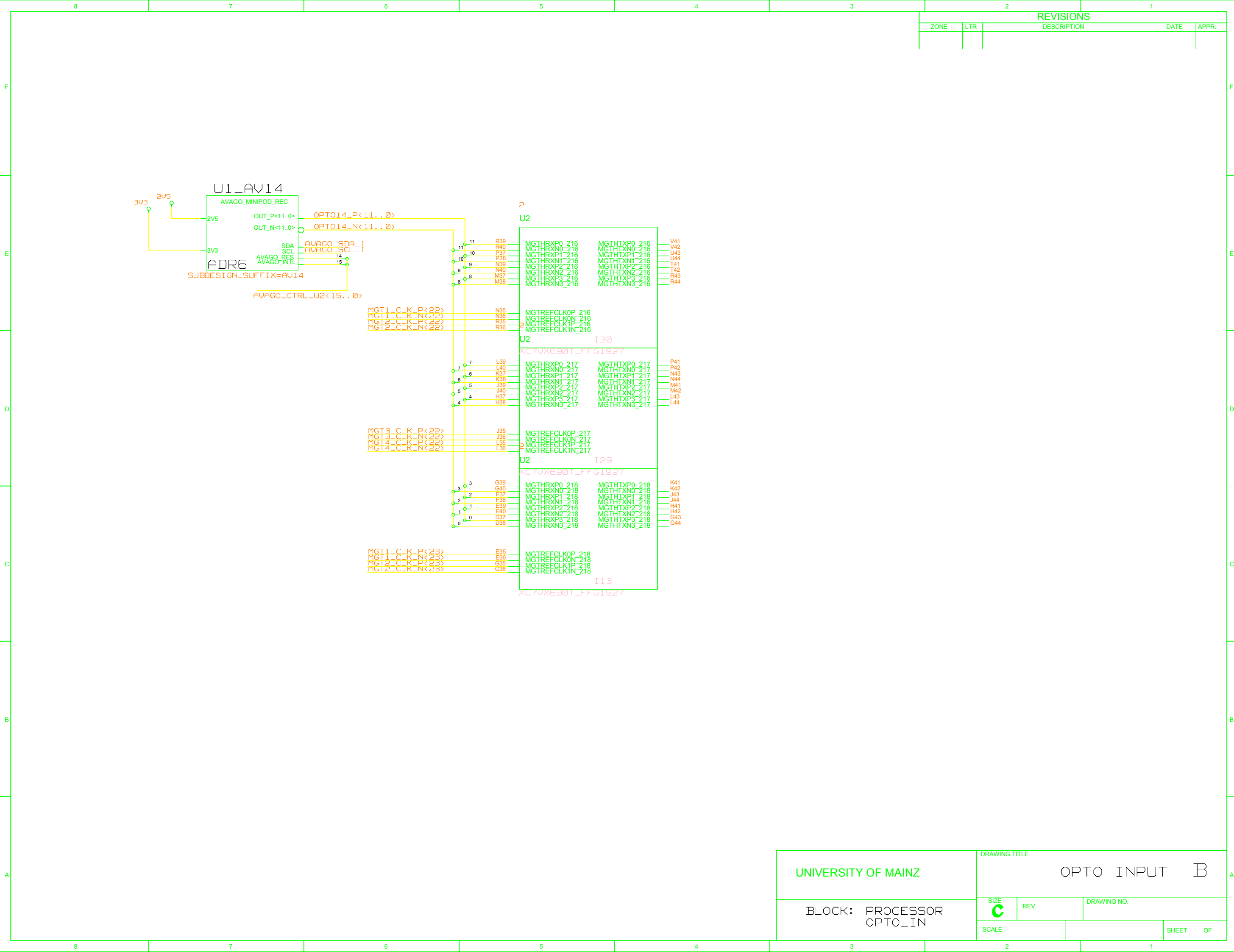


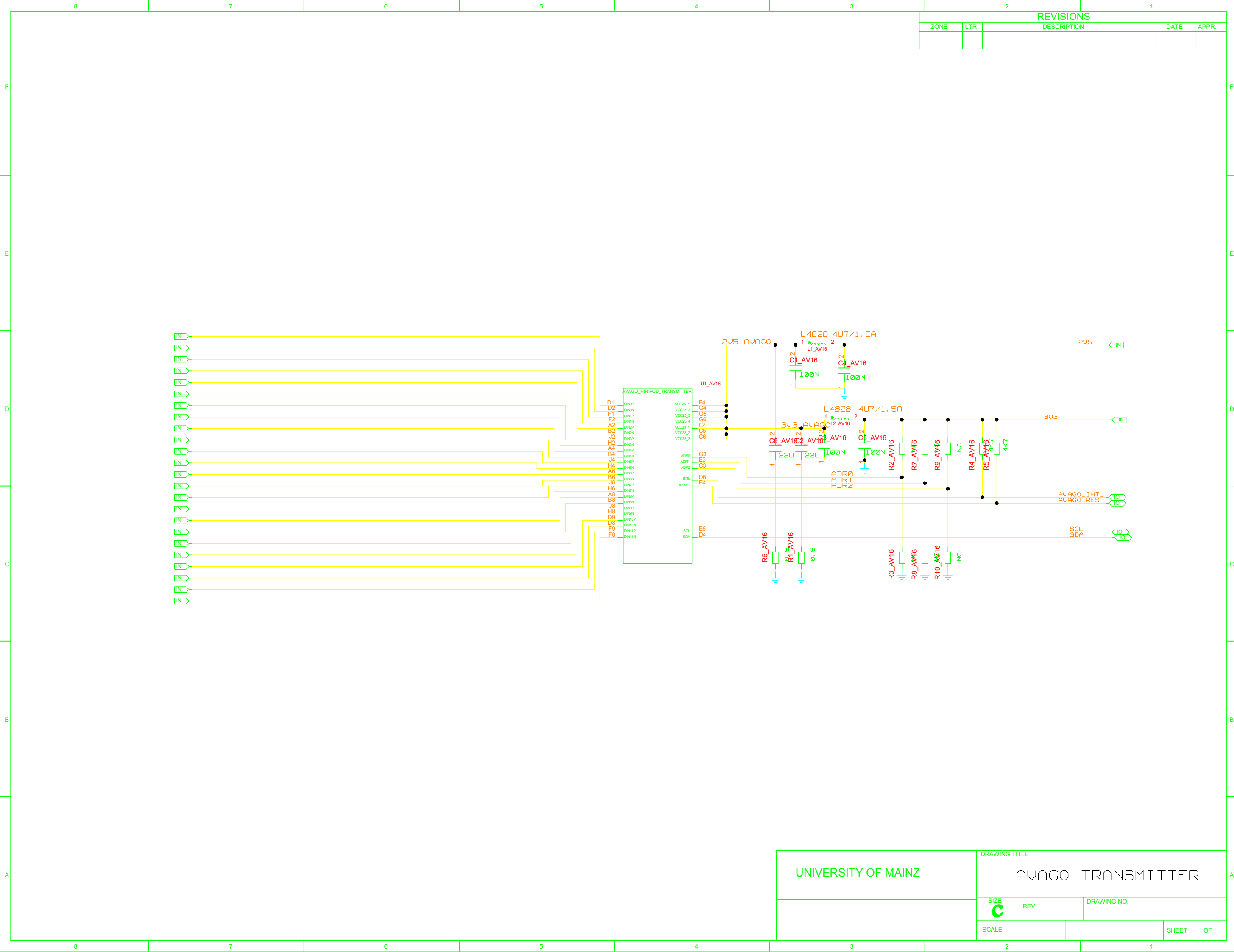


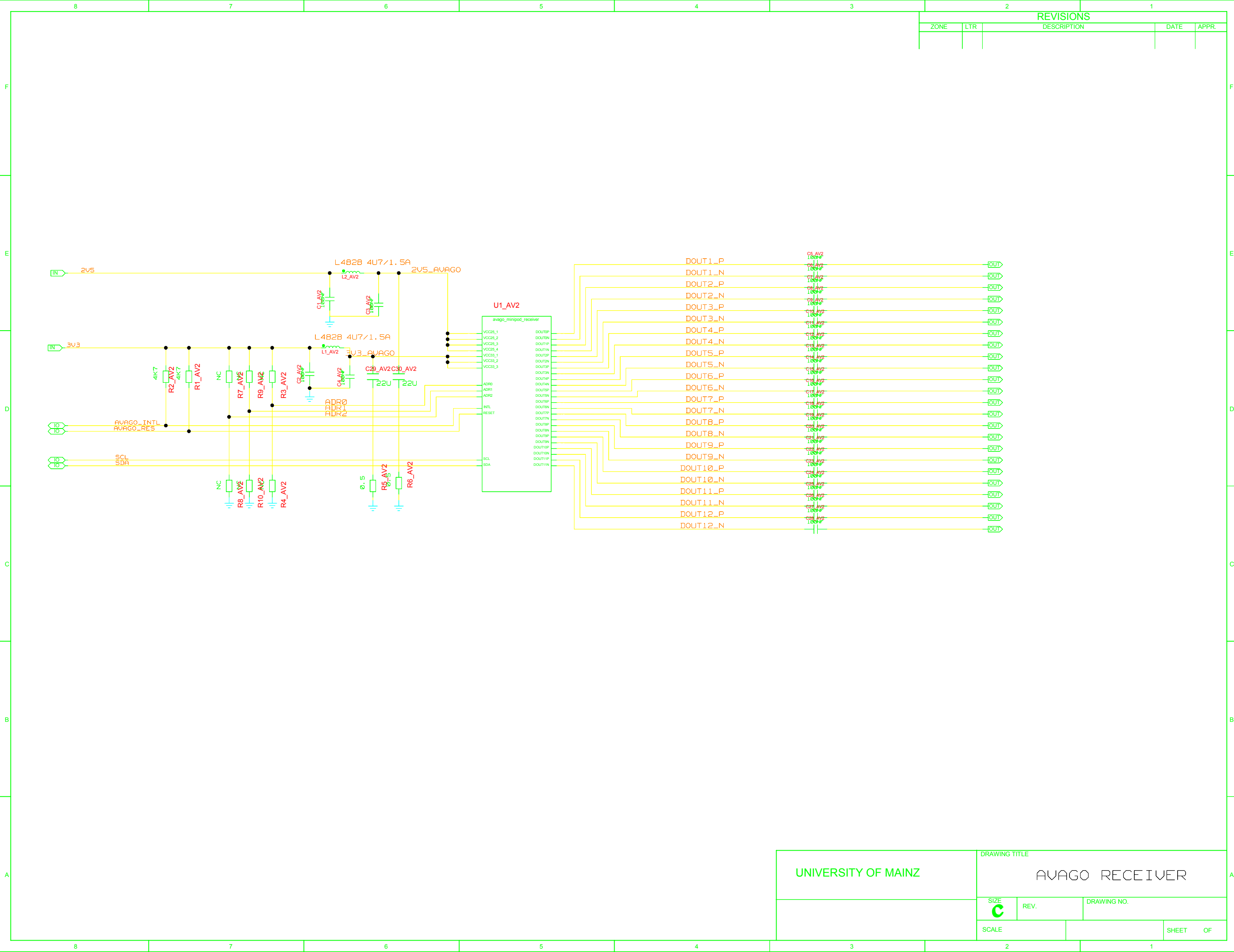
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ZONE	LTR	DESCRIPTION	DATE	APPR.

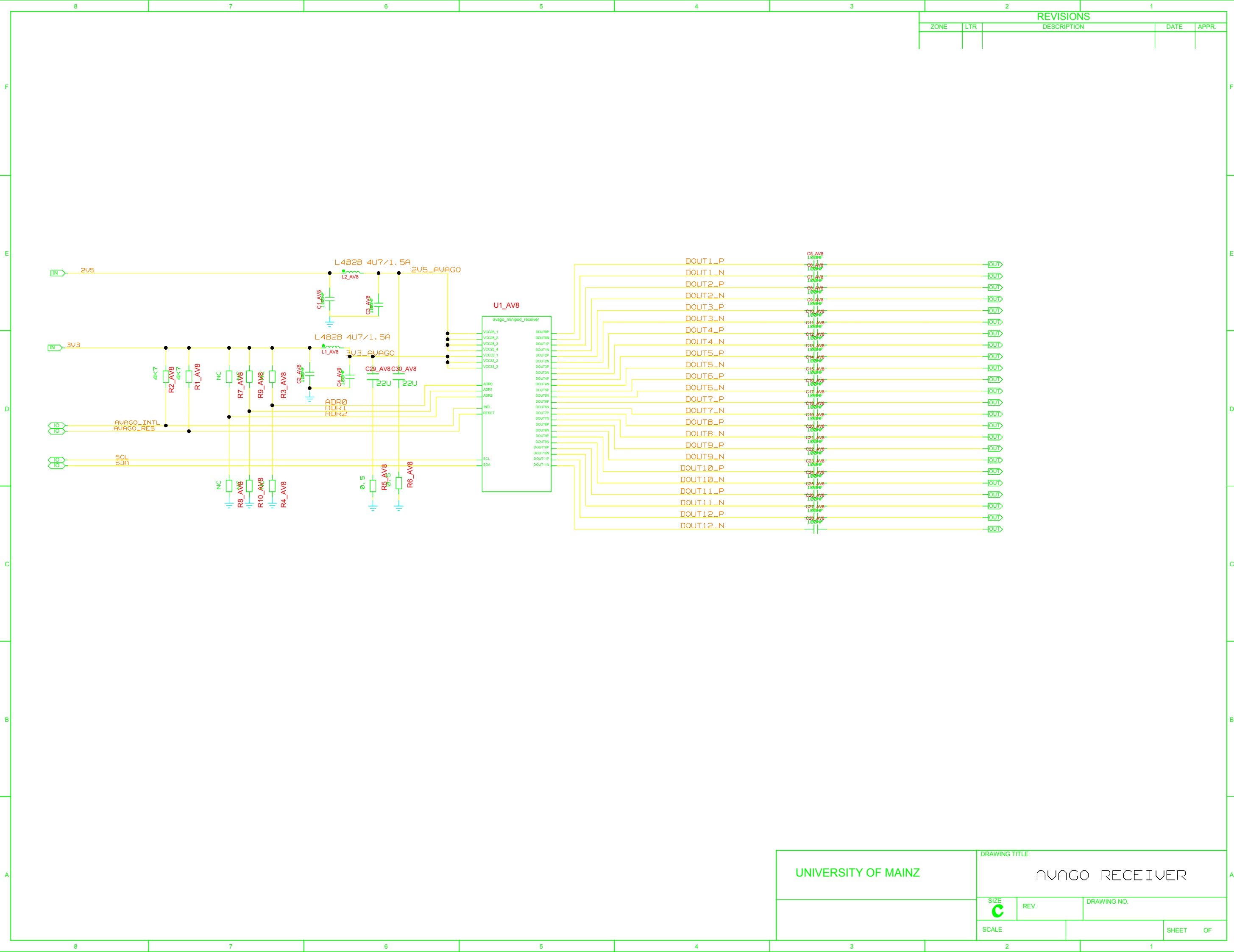
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	SCALE		SHEET OF

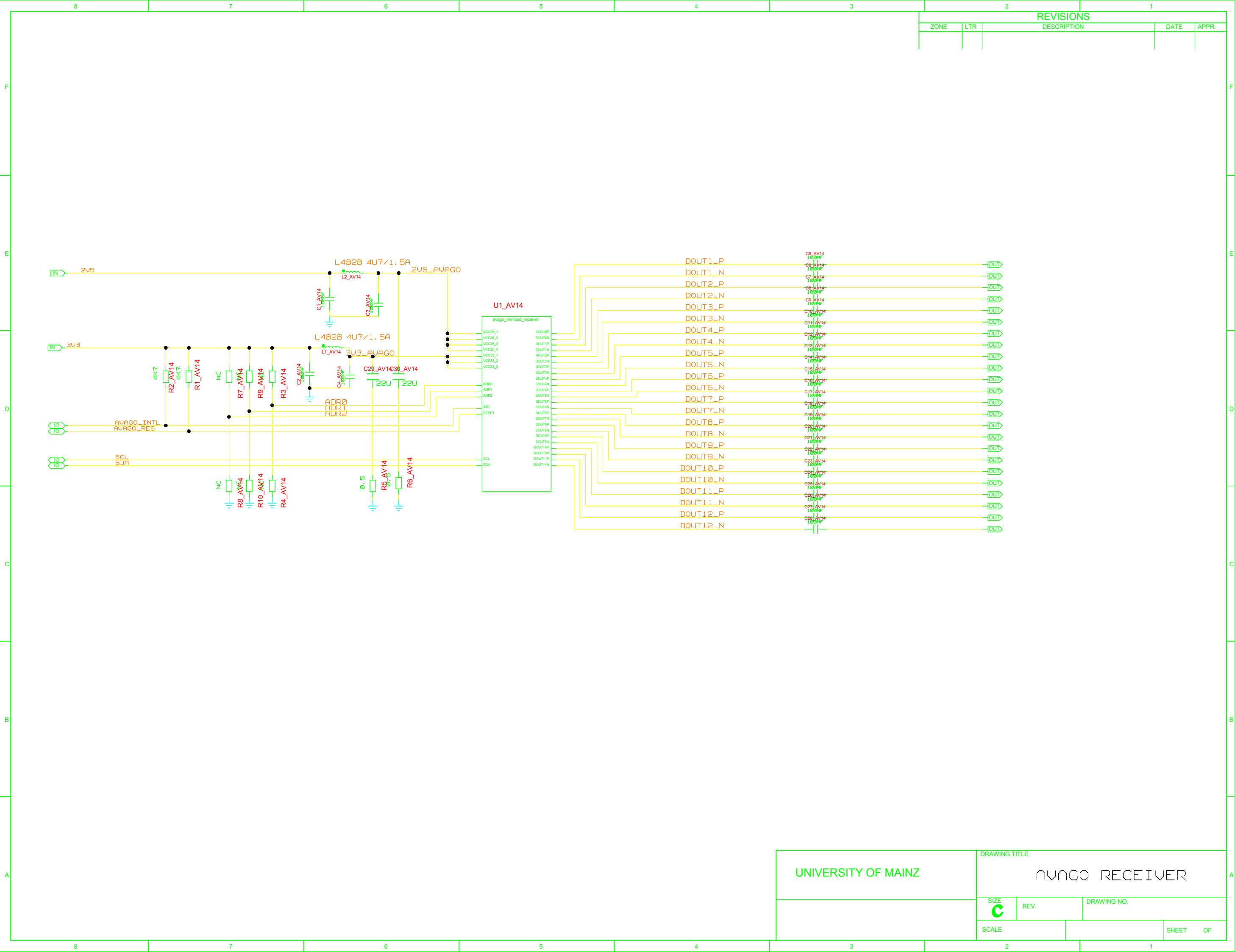


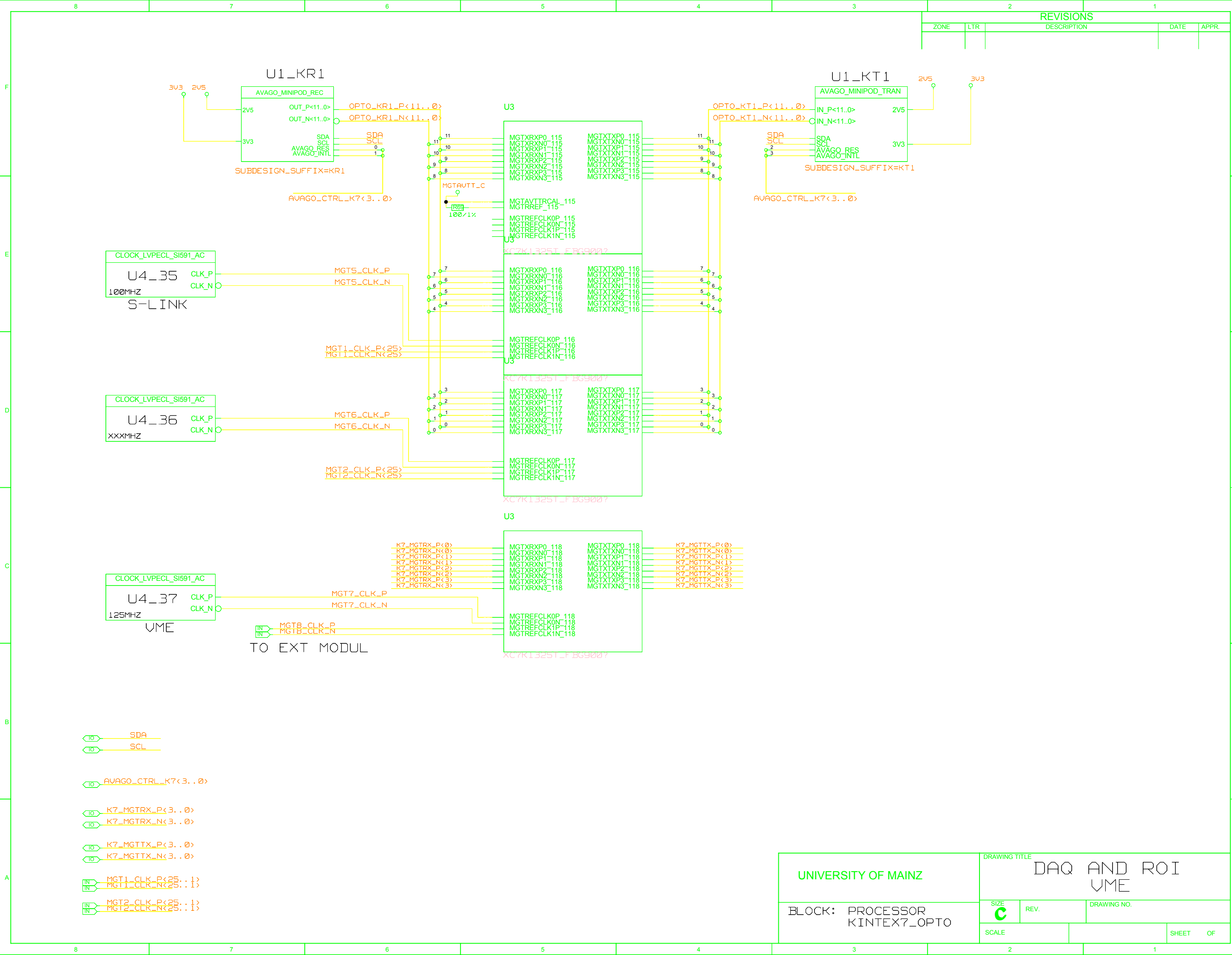


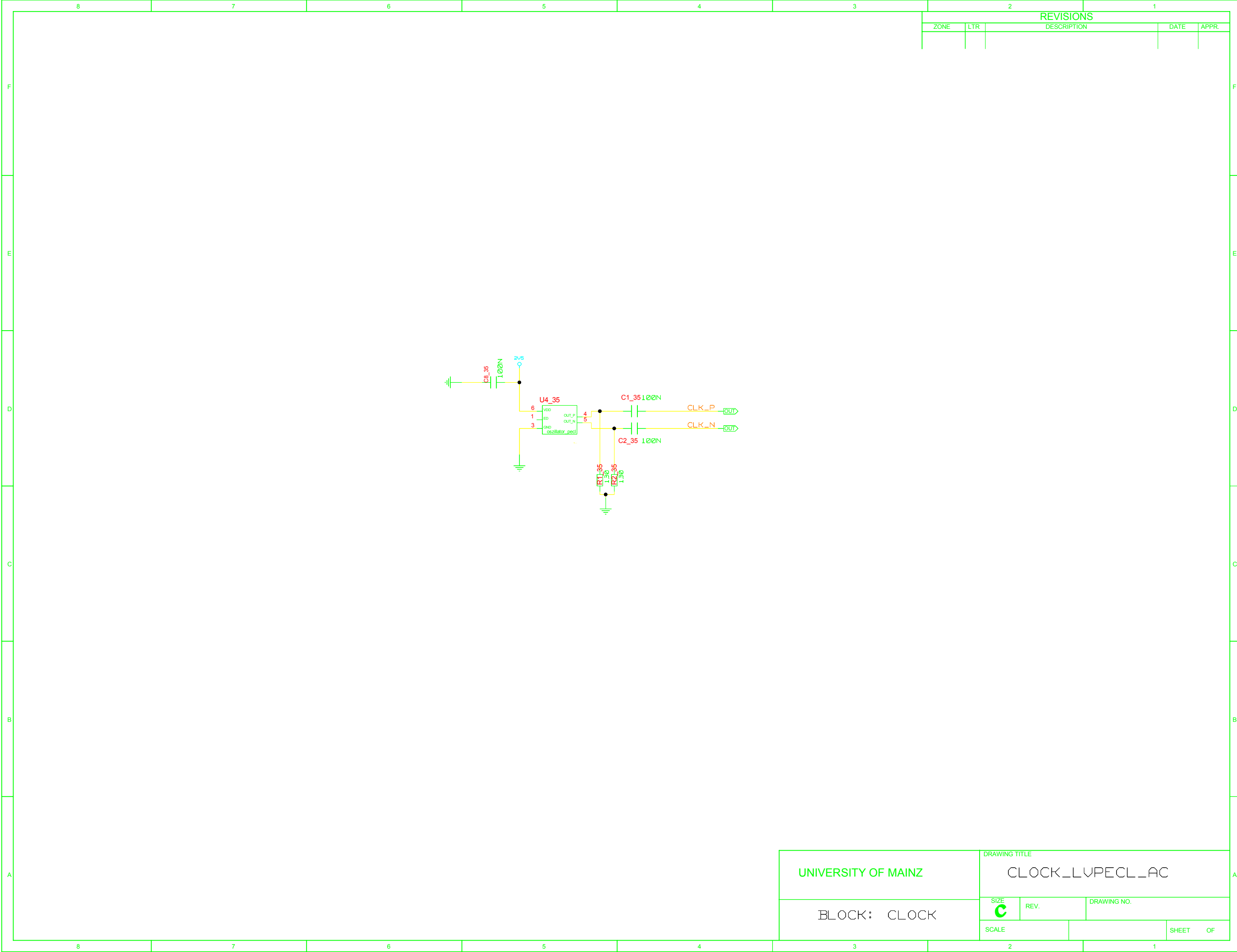


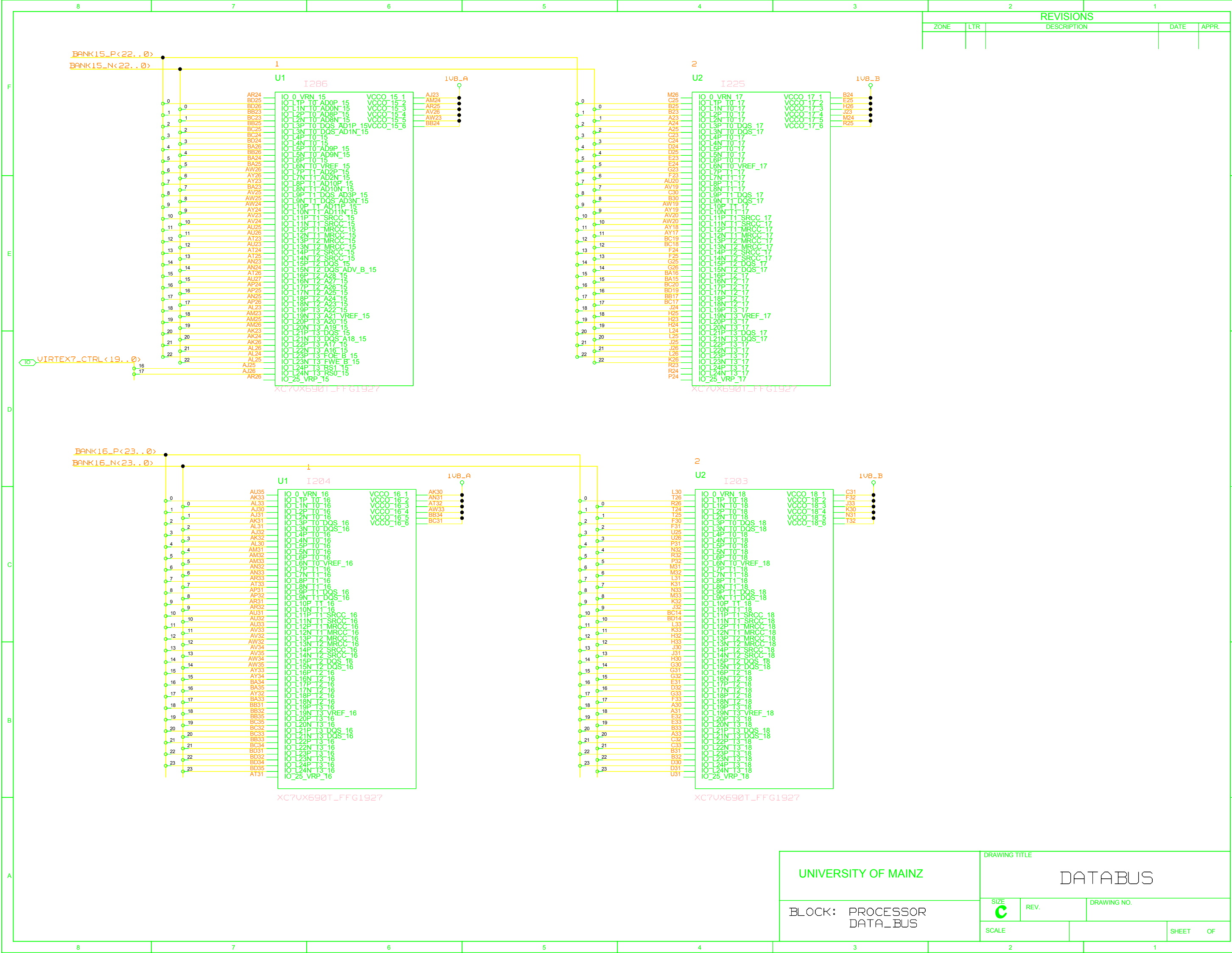






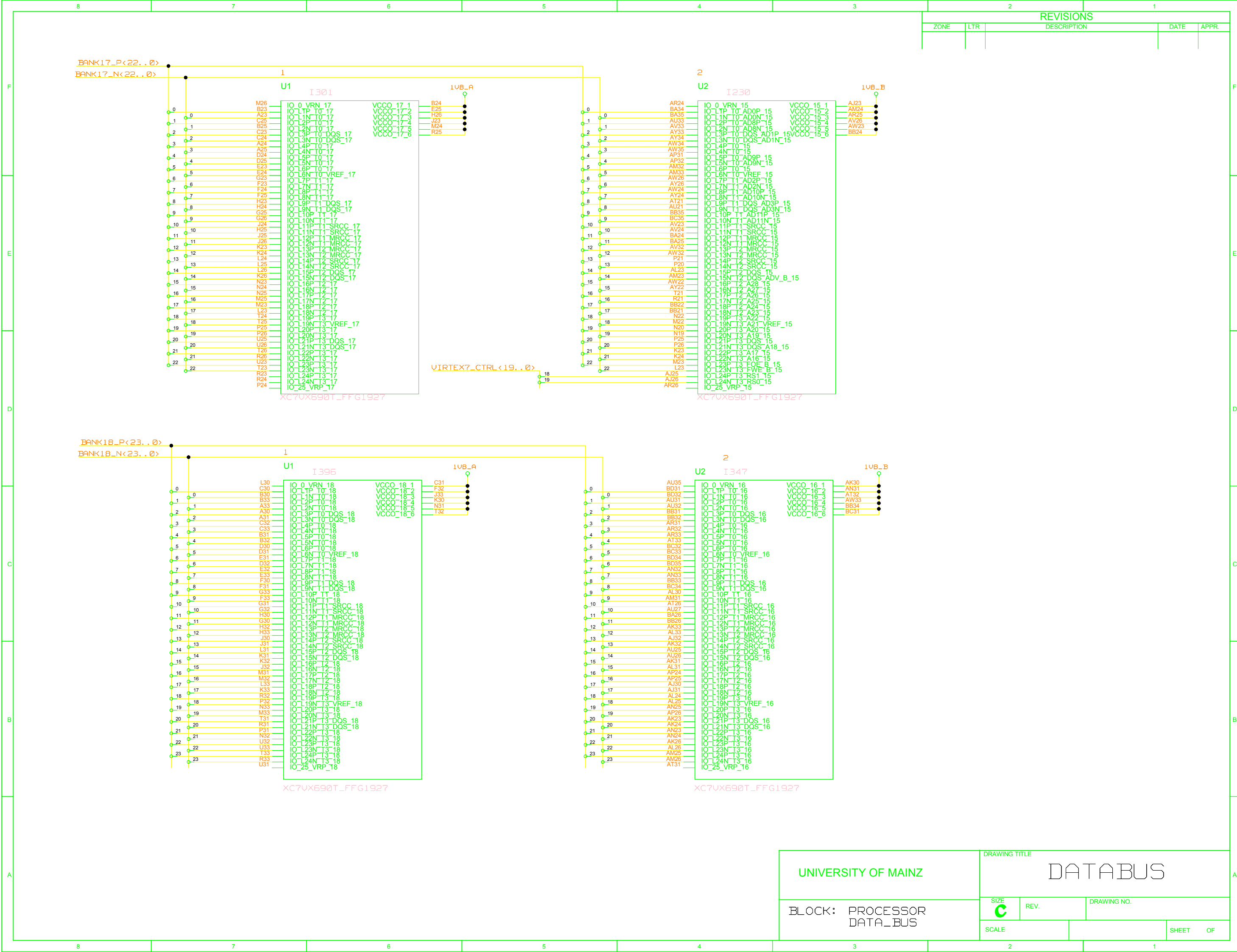


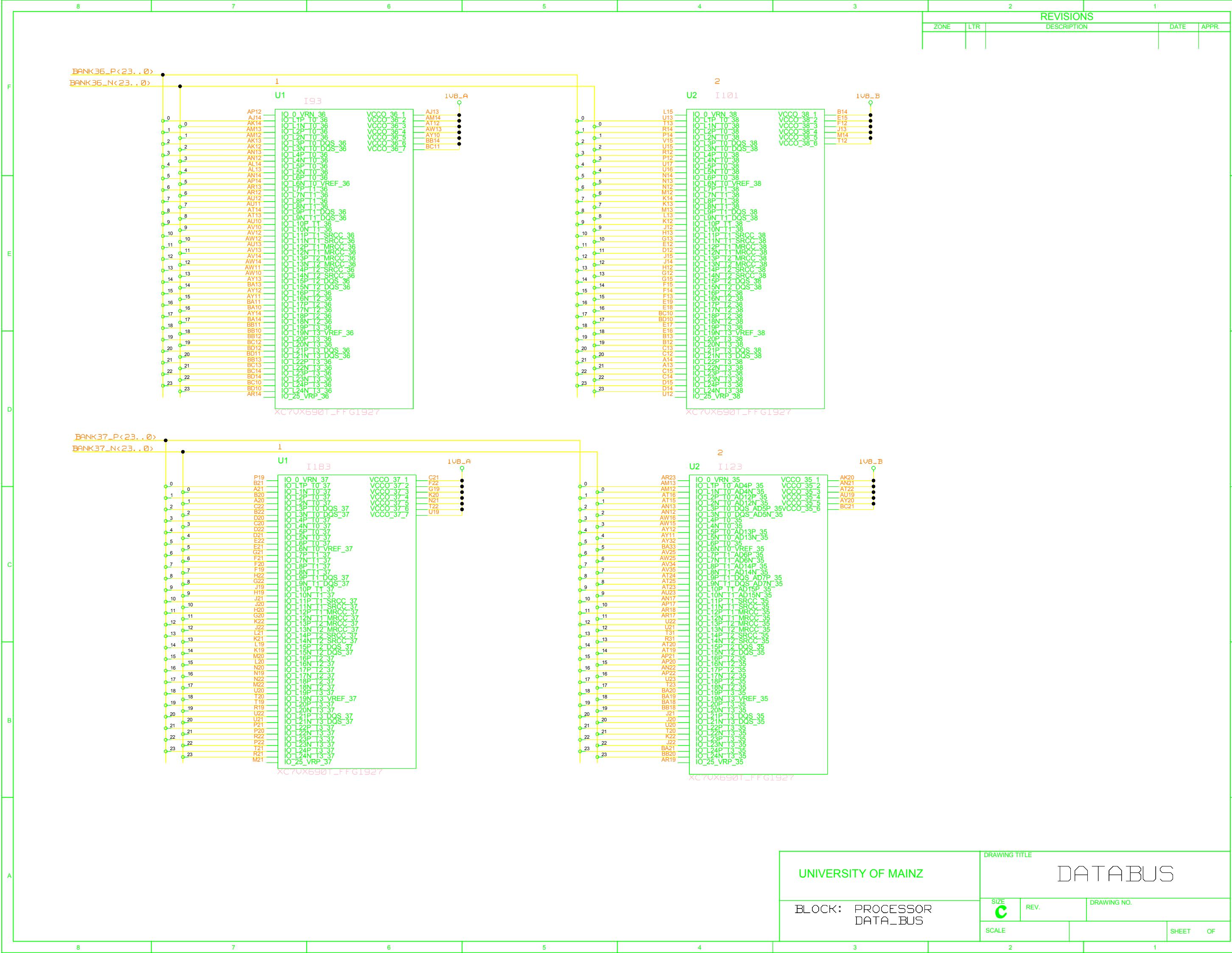




REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

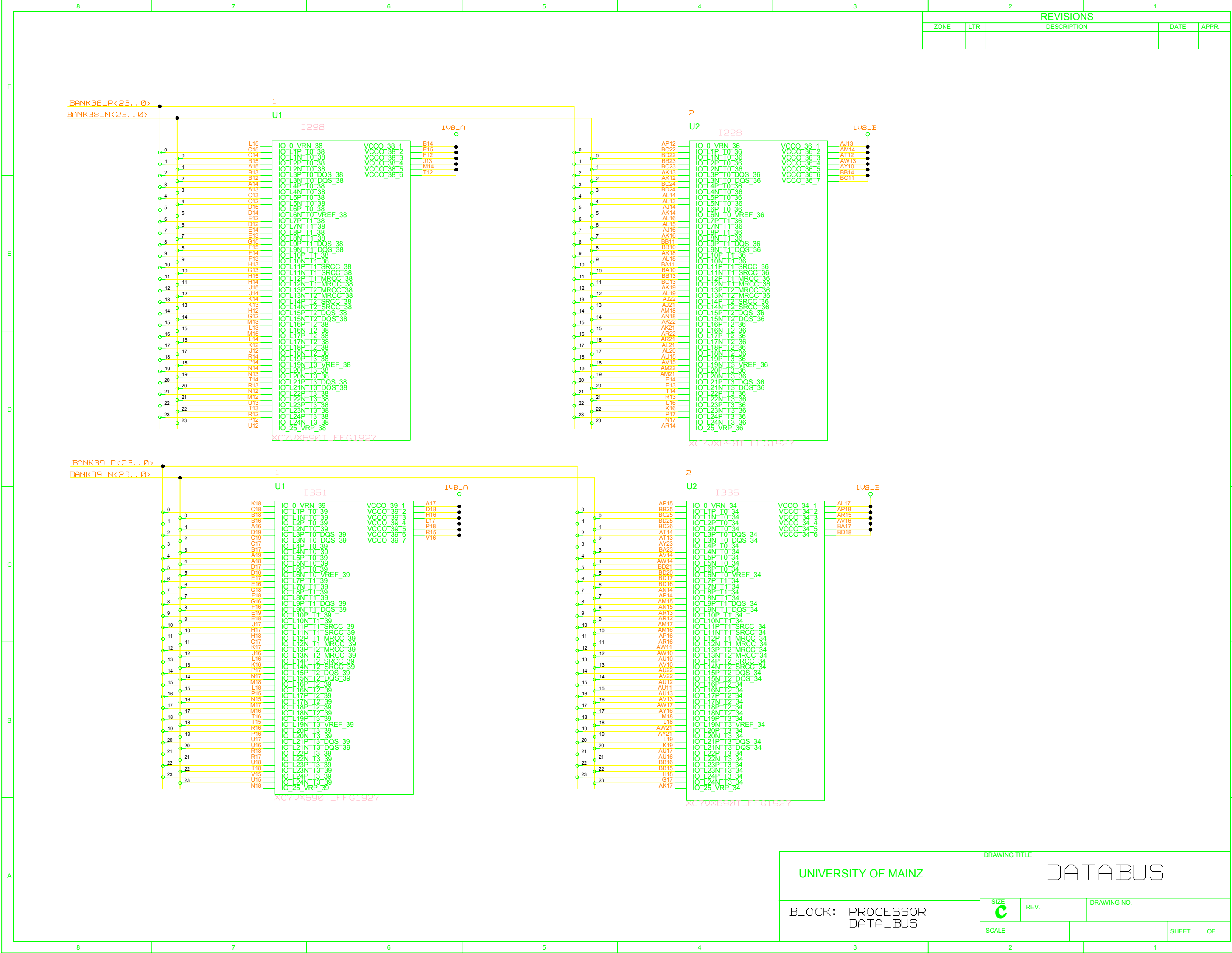
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SIZE	REV.	DRAWING NO.		
SCALE			SHEET	OF





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

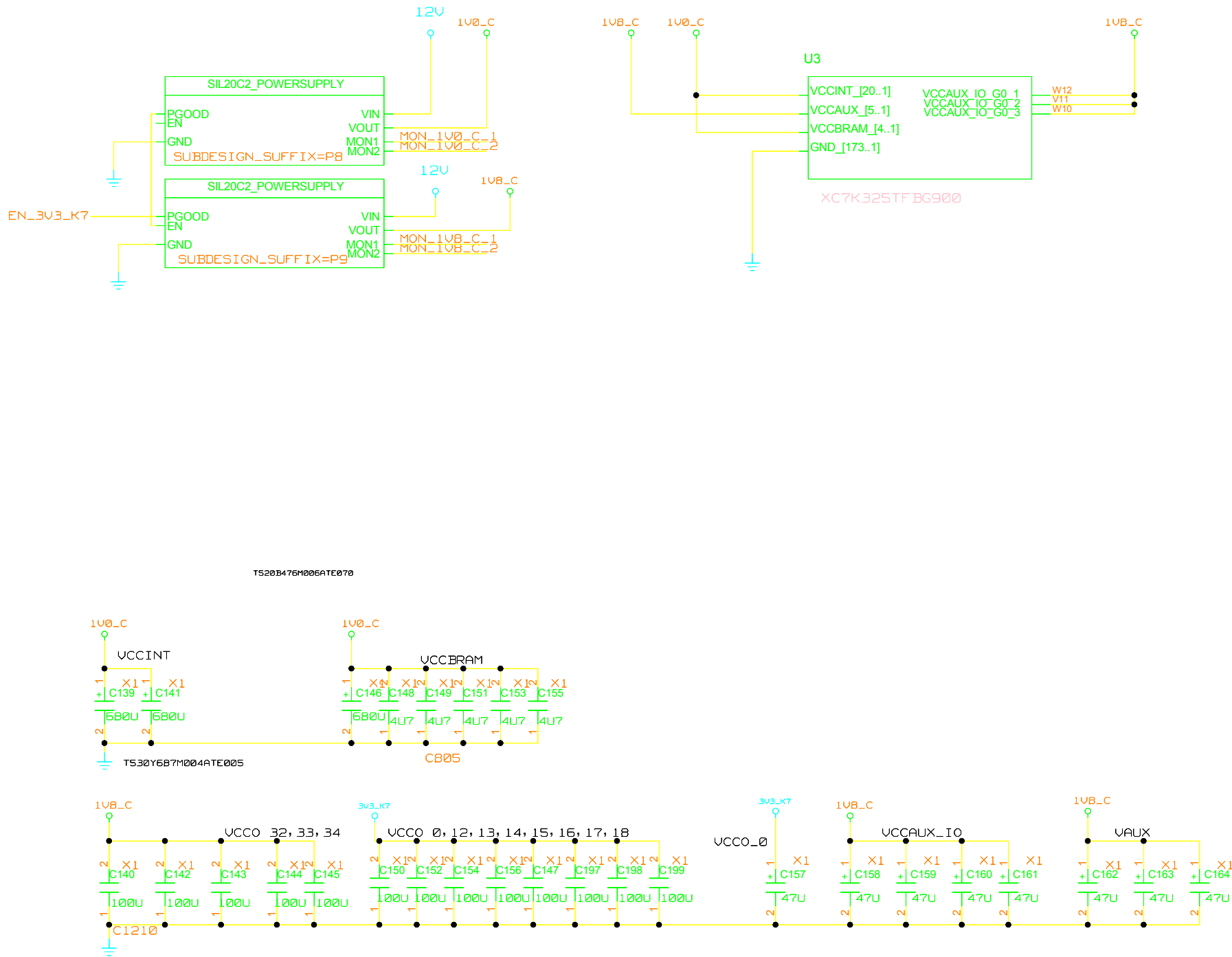
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SIZE	REV.	DRAWING NO.		
SCALE			SHEET	OF



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

UNIVERSITY OF MAINZ		DRAWING TITLE DATABUS		
BLOCK: PROCESSOR DATA_BUS		SIZE C	REV.	DRAWING NO.
SCALE		SHEET		OF

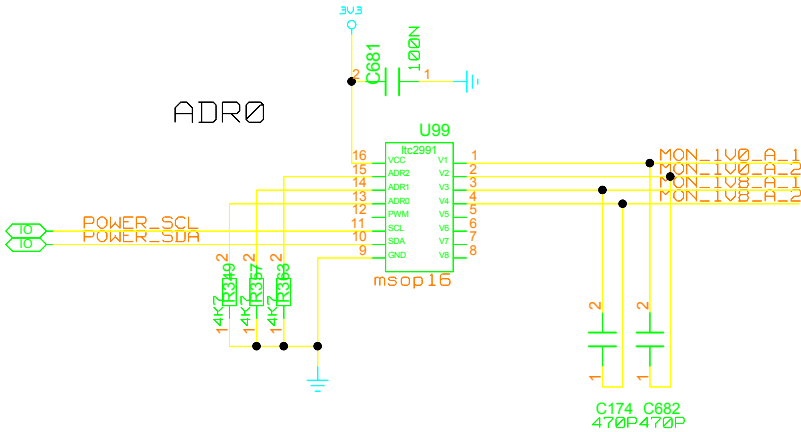
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



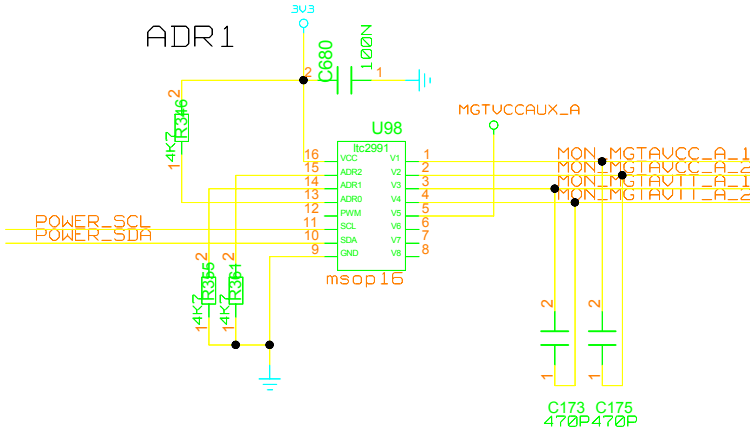
UNIVERSITY OF MAINZ		DRAWING TITLE POWER KINTEX7		
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SCALE		SHEET		OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

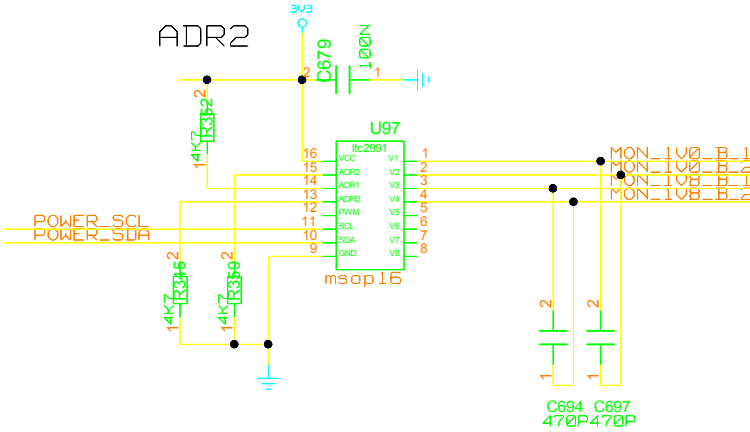
U1 CORE POWER MONITOR



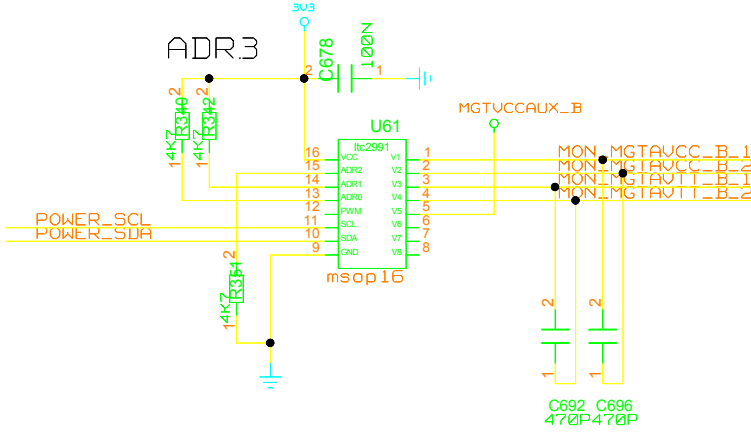
U1 MGT POWER MONITOR



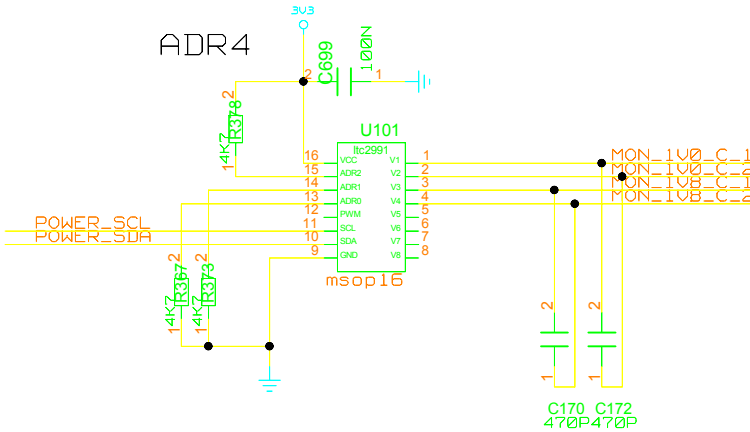
U2 CORE POWER MONITOR



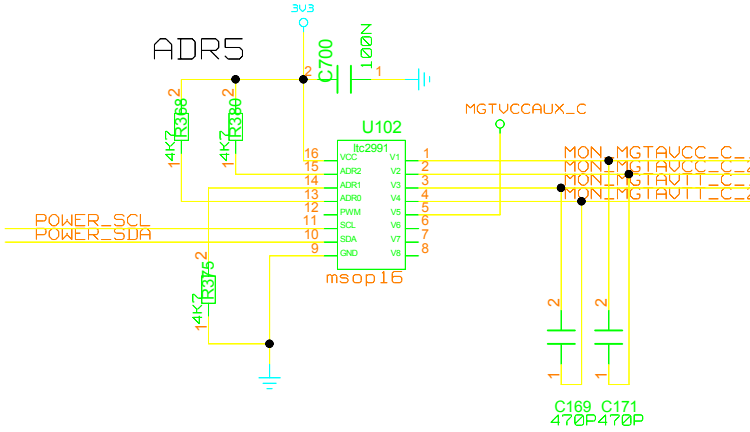
U2 MGT POWER MONITOR



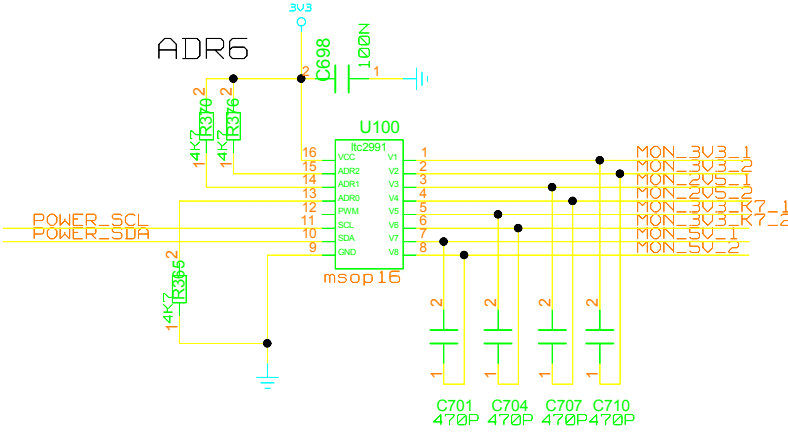
U3 CORE POWER MONITOR



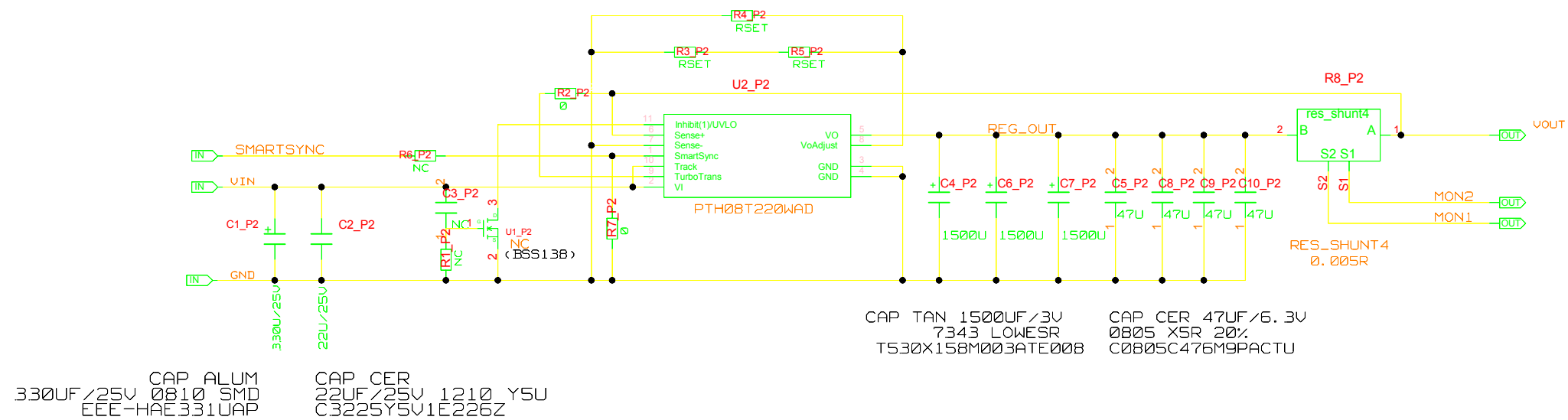
U3 MGT POWER MONITOR



2V5, 3V3 POWER MONITOR



UNIVERSITY OF MAINZ		DRAWING TITLE I2C POWERSUPPLY MONITORING		
SIZE C	REV. 26. 05. 2014	DRAWING NO.		
SCALE			SHEET	OF



$$R_{SET} = 10 \text{ k}\Omega \times \frac{0.69}{V_O - 0.69} = 1.43 \text{ k}\Omega$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V _O (Standard)	R _{SET} (Standard Value)	V _O (Actual)
5.0 V ⁽¹⁾	169 Ω	5.005 V
3.3 V	1.21 kΩ	3.304 V
2.5 V	2.37 kΩ	2.506 V
1.8 V	4.75 kΩ	1.807 V
1.5 V	6.98 kΩ	1.510 V
1.2 V ⁽²⁾	12.1 kΩ	1.200 V
1.0 V ⁽²⁾	20.5 kΩ	1.004 V
0.7 V ⁽²⁾	681 kΩ	0.700 V

UNIVERSITY OF MAINZ

DRAWING TITLE

PTH08T220W_POWER SUPPLY

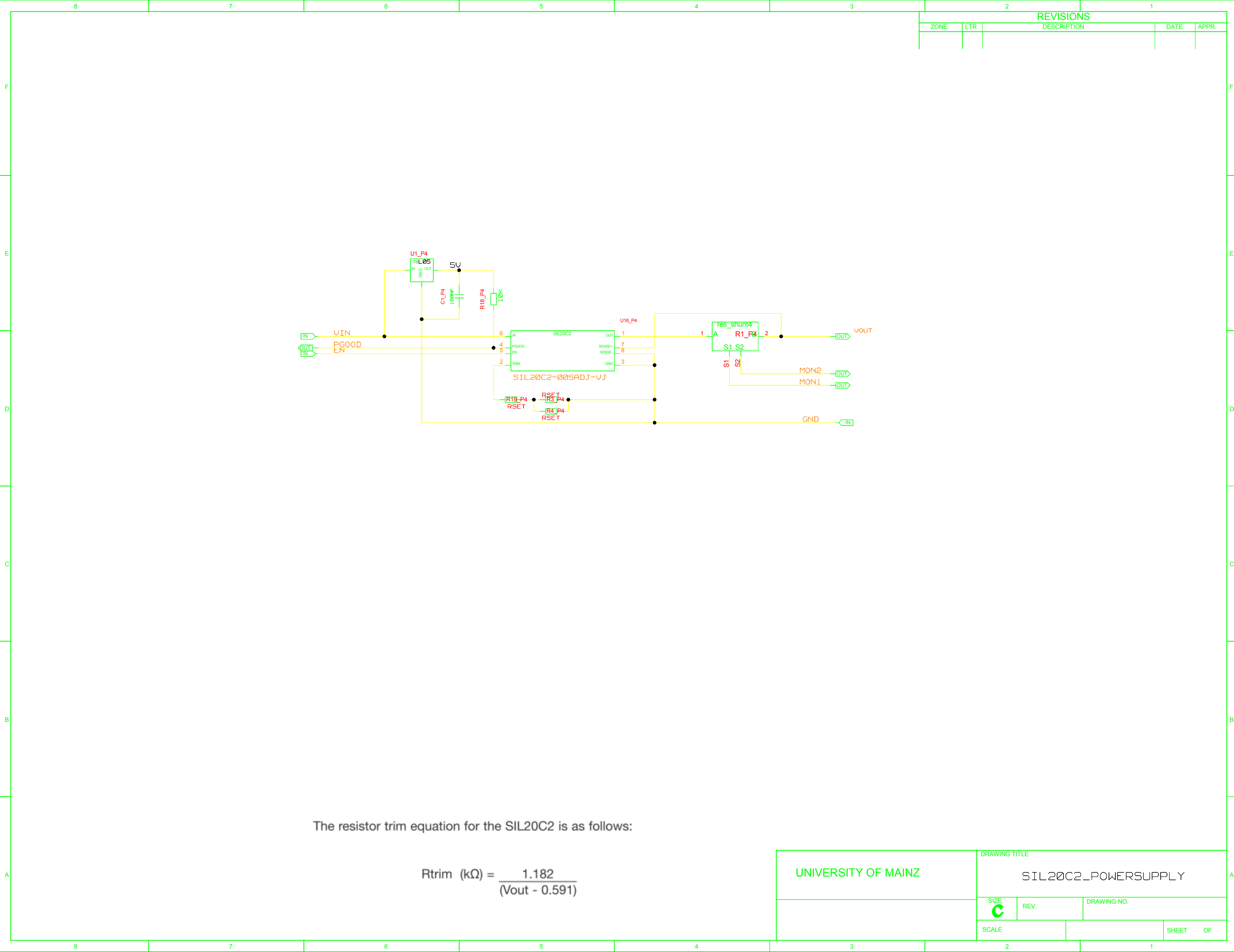
SIZE
C

REV.

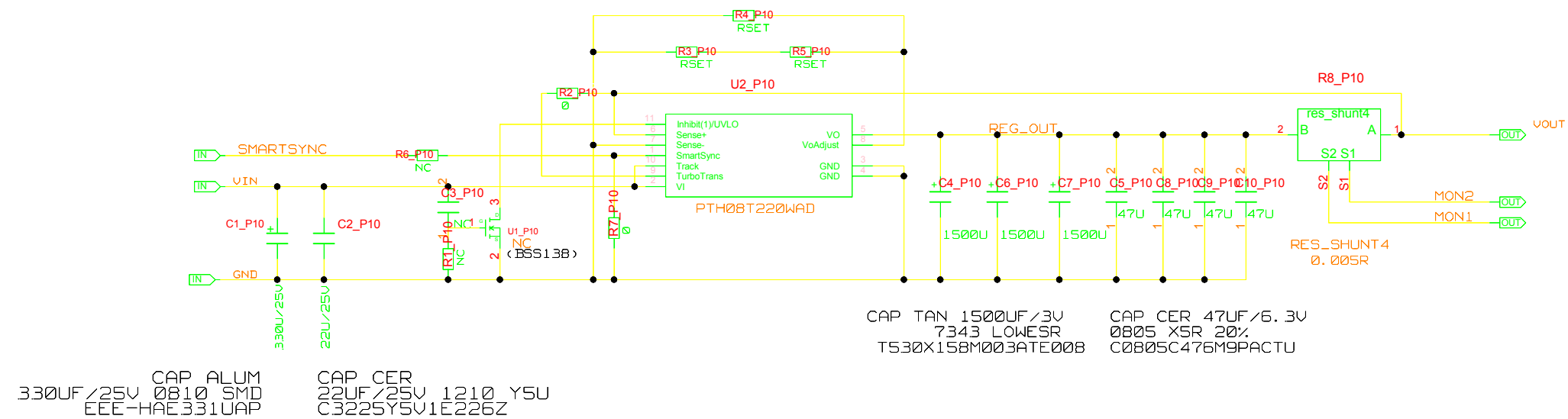
DRAWING NO.

SCALE

SHEET OF







$$R_{SET} = 10 \text{ k}\Omega \times \frac{0.69}{V_O - 0.69} = 1.43 \text{ k}\Omega$$

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1.0 V ⁽²⁾	20.5 kΩ	1.004 V
0.7 V ⁽²⁾	681 kΩ	0.700 V

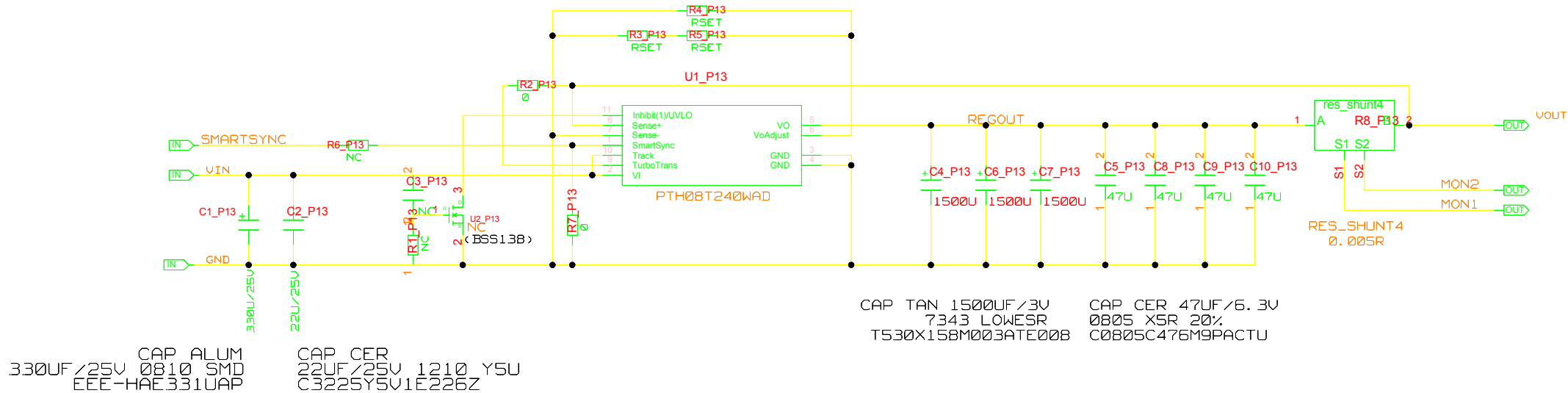


Table 2. Output Voltage Set-Point Resistor Values (Standard Values)			
V _O Required (V)	R _{SET} (kΩ)	V _O Required (V)	R _{SET} (Ω)
0.70 ⁽¹⁾	681	2.50	2.37 k
0.75 ⁽¹⁾	113	2.60	2.15 k
0.80 ⁽¹⁾	61.9	2.70	2.00 k
0.85 ⁽¹⁾	41.2	2.80	1.82 k
0.90 ⁽¹⁾	31.8	2.90	1.69 k
0.95 ⁽¹⁾	24.9	3.00	1.54 k
1.00 ⁽¹⁾	20.5	3.10	1.43 k
1.05 ⁽¹⁾	17.8	3.20	1.33 k
1.10 ⁽¹⁾	15.4	3.30	1.21 k
1.15 ⁽¹⁾	13.3	3.40	1.10 k
1.20 ⁽¹⁾	12.1	3.50	1.02 k
1.25	10.7	3.60	931
1.30	9.88	3.70 ⁽²⁾	866
1.35	9.09	3.80 ⁽²⁾	787
1.40	8.25	3.90 ⁽²⁾	715
1.45	7.68	4.00 ⁽²⁾	649
1.50	6.98	4.10 ⁽²⁾	590
1.55	6.49	4.20 ⁽²⁾	536
1.60	6.04	4.30 ⁽²⁾	475
1.65	5.78	4.40 ⁽²⁾	432
1.70	5.36	4.50 ⁽²⁾	383
1.75	5.11	4.60 ⁽²⁾	332
1.80	4.75	4.70 ⁽²⁾	287
1.85	4.53	4.80 ⁽²⁾	249
1.90	4.22	4.90 ⁽²⁾	210
1.95	4.02	5.00 ⁽²⁾	169
2.00	3.83	5.10 ⁽²⁾	133
2.10	3.40	5.20 ⁽²⁾	100
2.20	3.09	5.30 ⁽²⁾	66.5
2.30	2.67	5.40 ⁽²⁾	34.8
2.40	2.61	5.50 ⁽²⁾	4.99

(1) For output voltages ≤ 1.2V, at nominal operating frequency, the output ripple may increase (typically 2x) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature, review the SmartSync application section for further guidance.

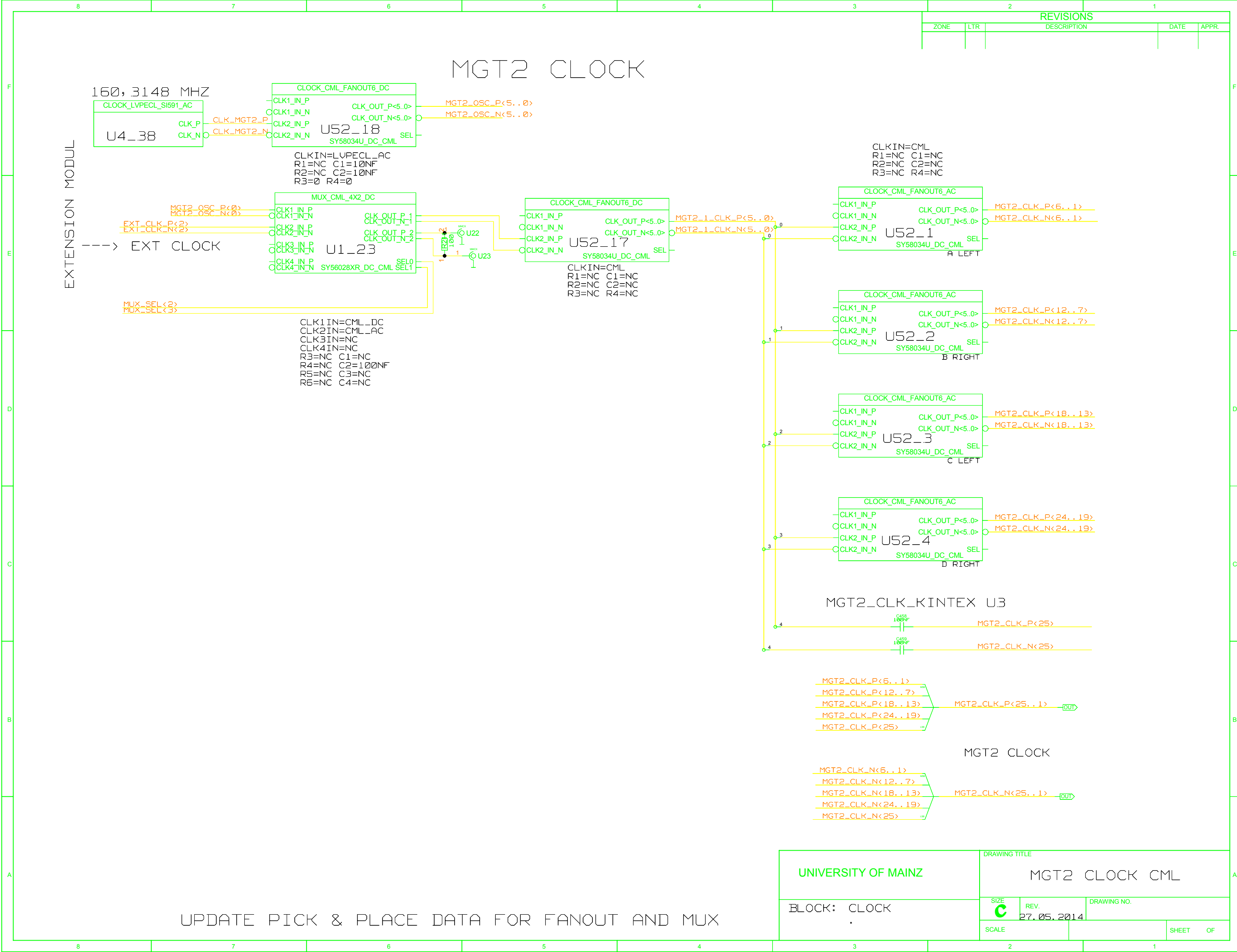
(2) For V_O > 3.6 V, the minimum input voltage is (V_O + 2) V.

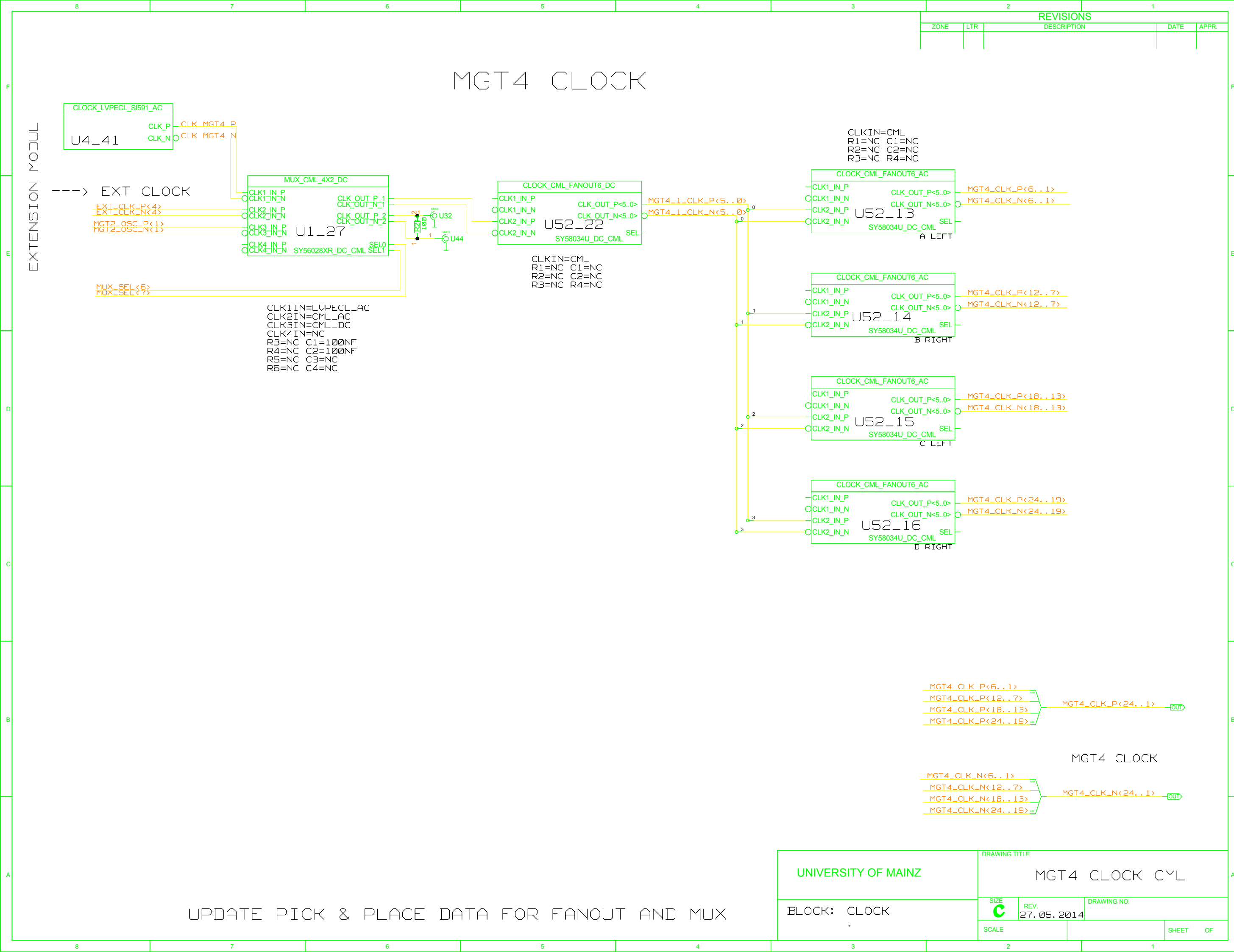
UNIVERSITY OF MAINZ

DRAWING TITLE

PTH08T240W_POWER SUPPLY

SIZE C	REV.	DRAWING NO.
SCALE		SHEET OF





8

7

6

5

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3

2

1

A

B

C

D

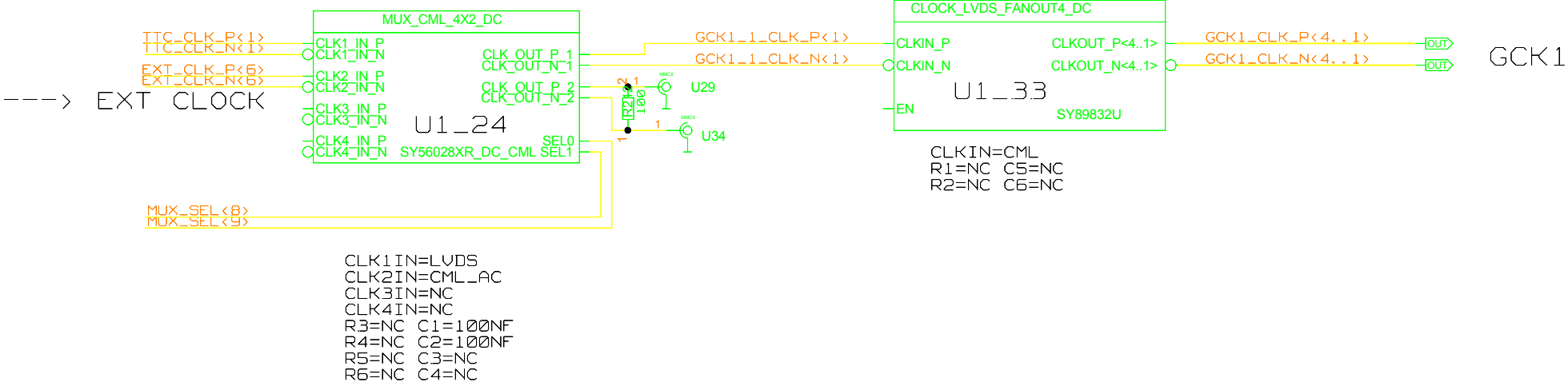
E

F

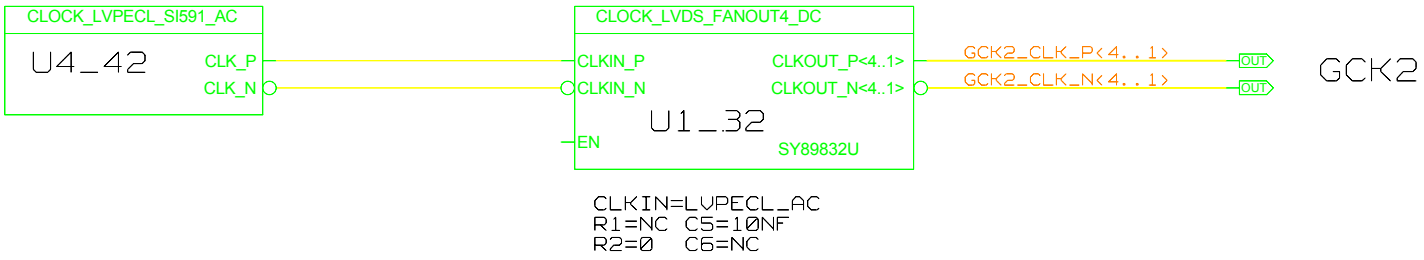
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ZONE	LTR	DESCRIPTION	DATE	APPR.

GCK1 + GCK2 CLOCK

EXTENSION MODUL



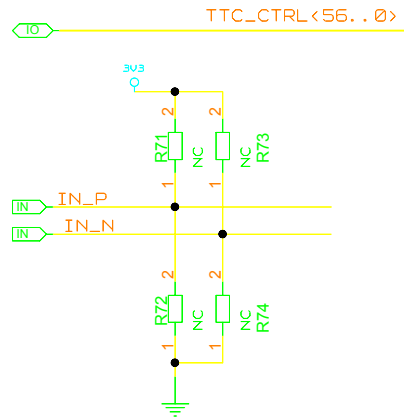
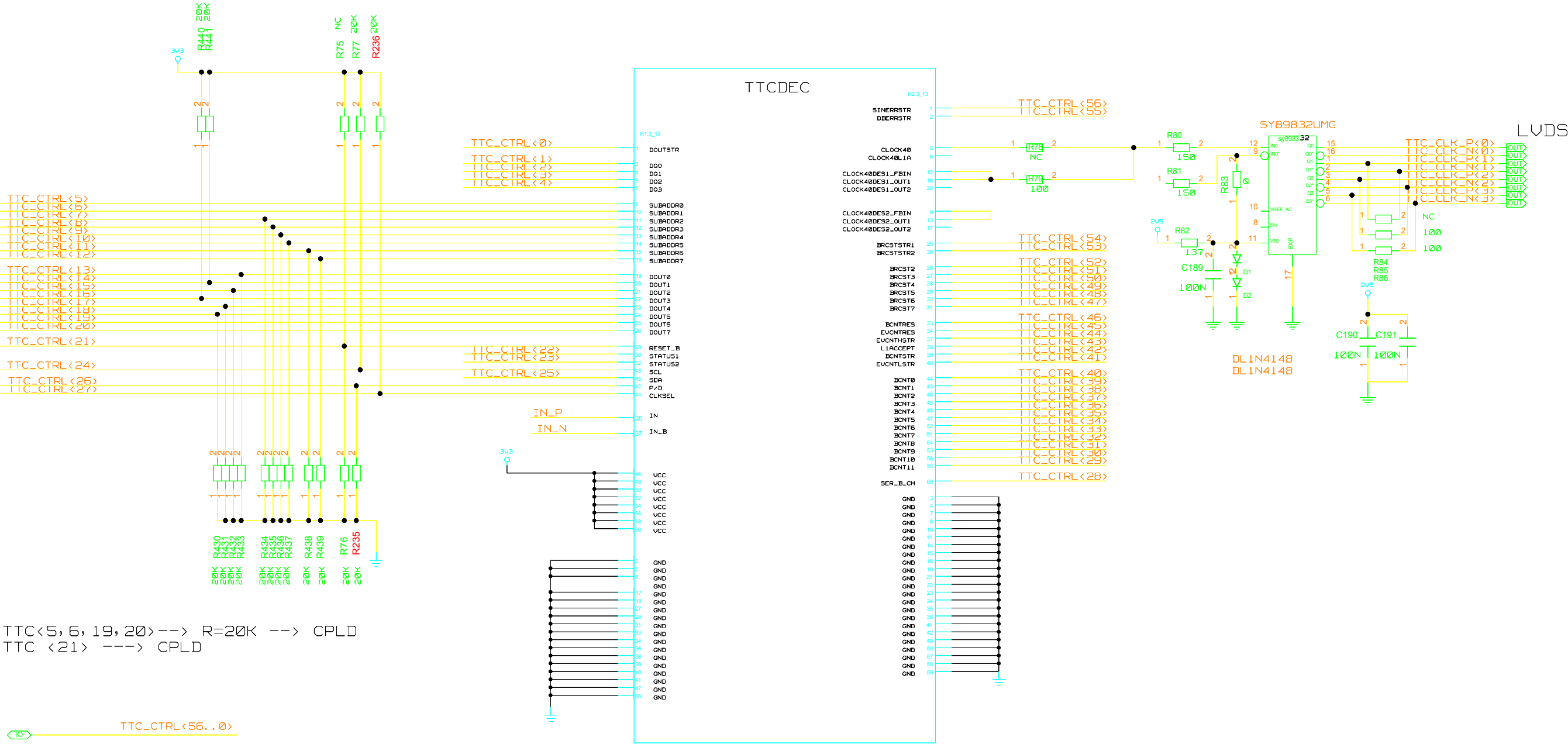
40,0787 MHZ



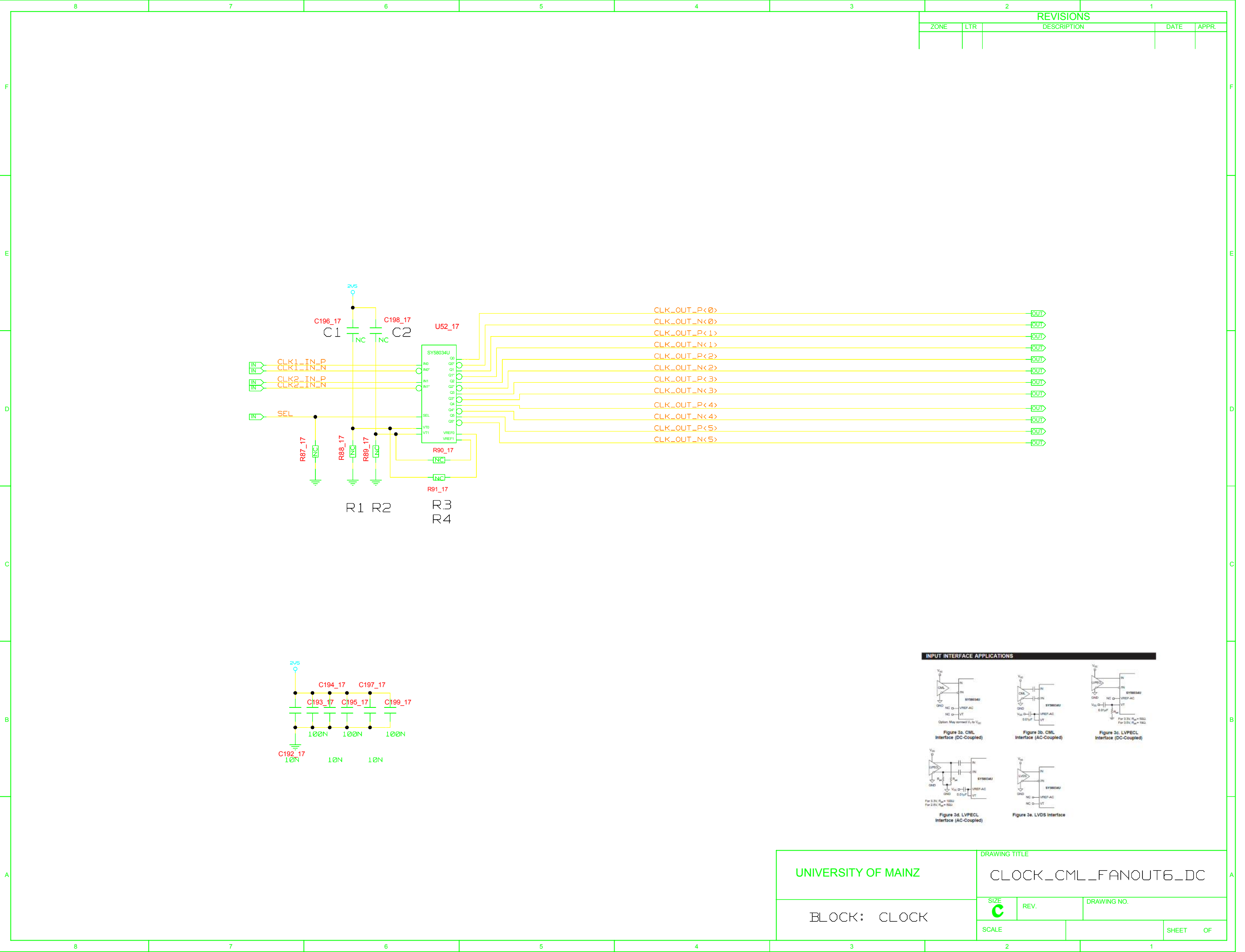
UPDATE PICK & PLACE DATA FOR FANOUT AND MUX

UNIVERSITY OF MAINZ		DRAWING TITLE		
BLOCK: CLOCK		GCK1+2 CLOCK LVDS		
SIZE	REV.	DRAWING NO.		
C	27.05.2014			
SCALE			SHEET	OF

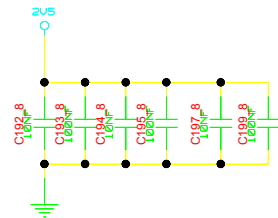
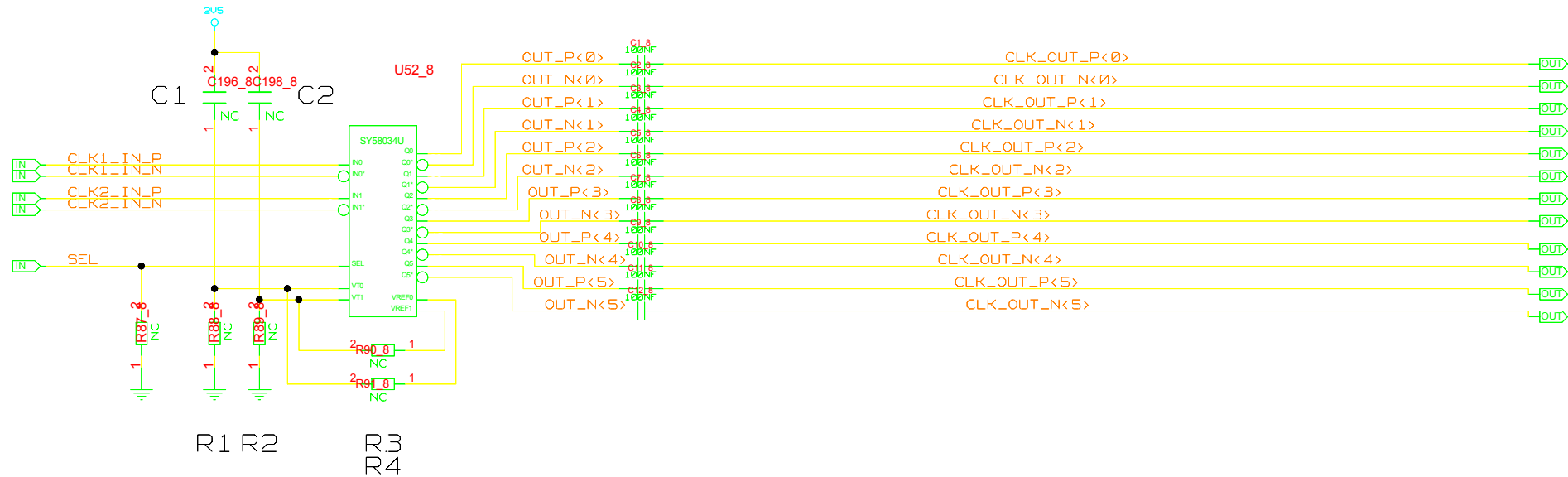
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



UNIVERSITY OF MAINZ		30.05.2014 U. SCHAEFFER	
		DRAWING TITLE TTC	
SCALE	SIZE C	REV. 30.05.2014	DRAWING NO.
	SHEET		OF



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

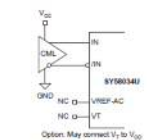


Figure 3a. CML Interface (DC-Coupled)

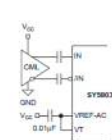


Figure 3b. CML Interface (AC-Coupled)

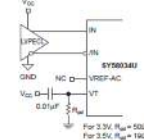


Figure 3c. LVPECL Interface (DC-Coupled)

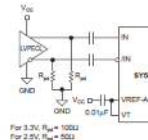


Figure 3d. LVPECL Interface (AC-Coupled)

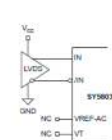


Figure 3e. LVDS Interface

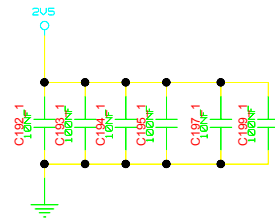
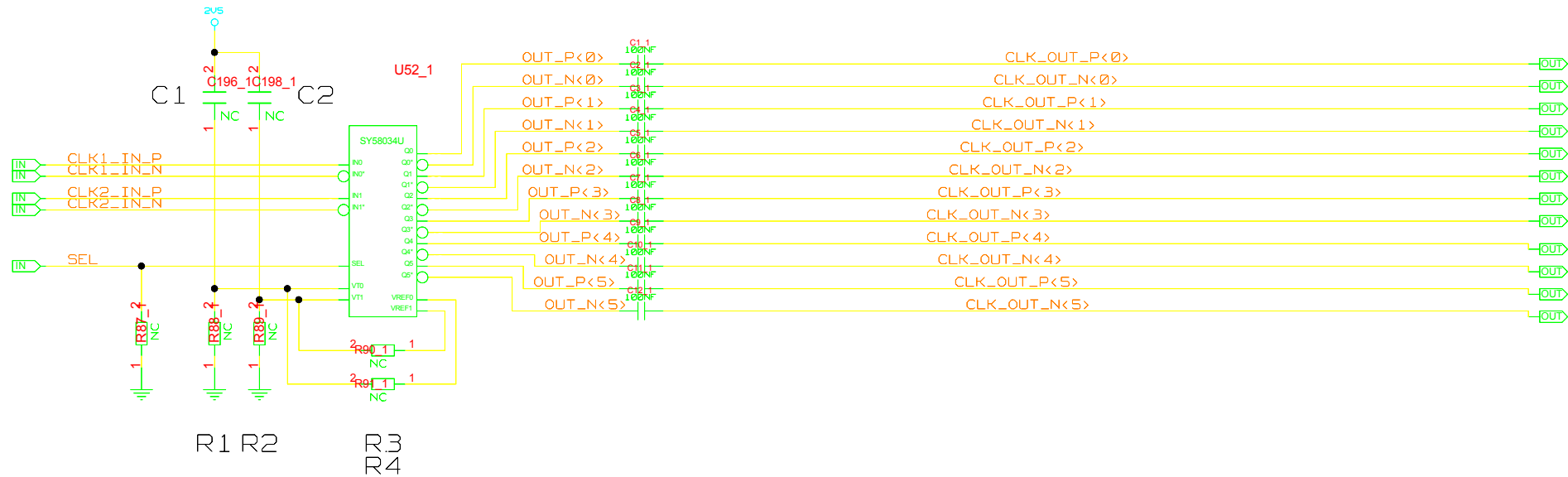
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

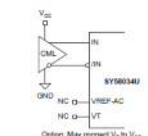


Figure 3a. CML Interface (DC-Coupled)

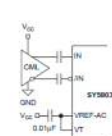


Figure 3b. CML Interface (AC-Coupled)

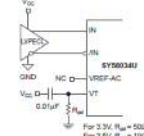


Figure 3c. LVPECL Interface (DC-Coupled)

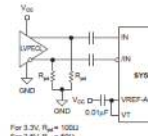


Figure 3d. LVPECL Interface (AC-Coupled)

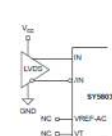


Figure 3e. LVDS Interface

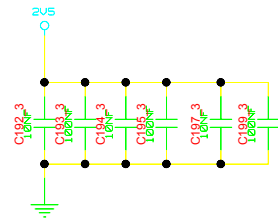
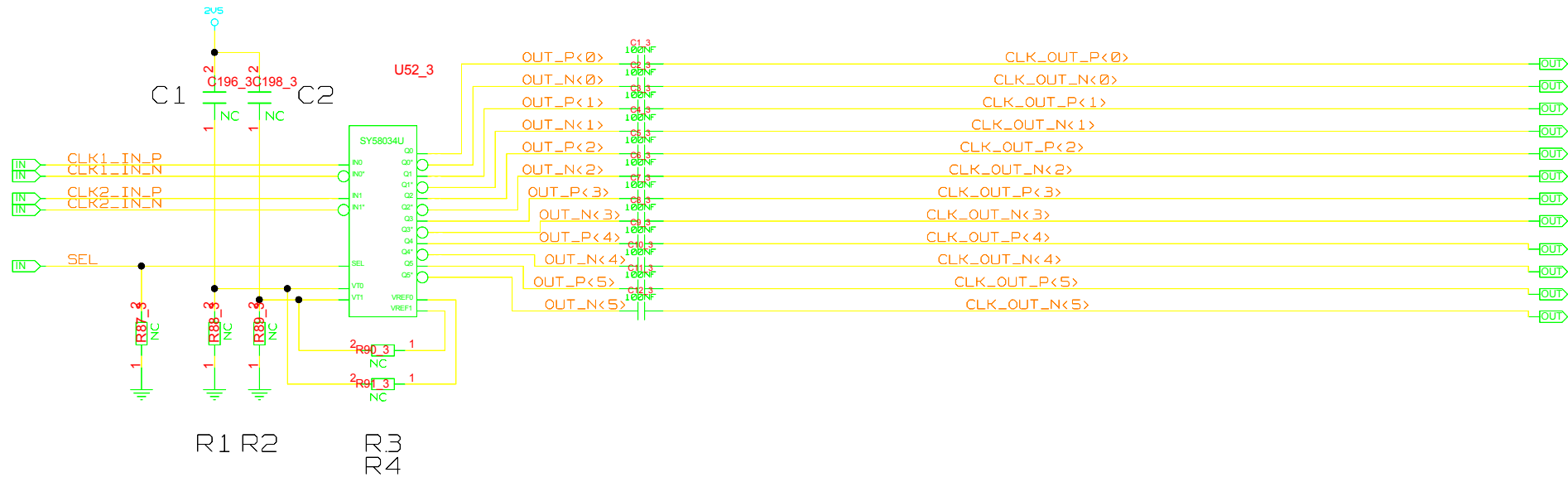
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

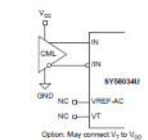


Figure 3a. CML Interface (DC-Coupled)

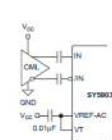


Figure 3b. CML Interface (AC-Coupled)

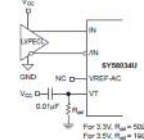


Figure 3c. LVPECL Interface (DC-Coupled)

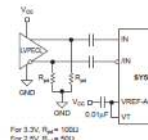


Figure 3d. LVPECL Interface (AC-Coupled)

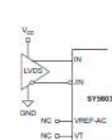


Figure 3e. LVDS Interface

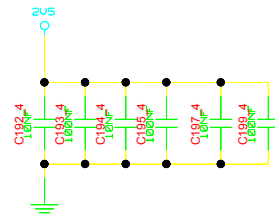
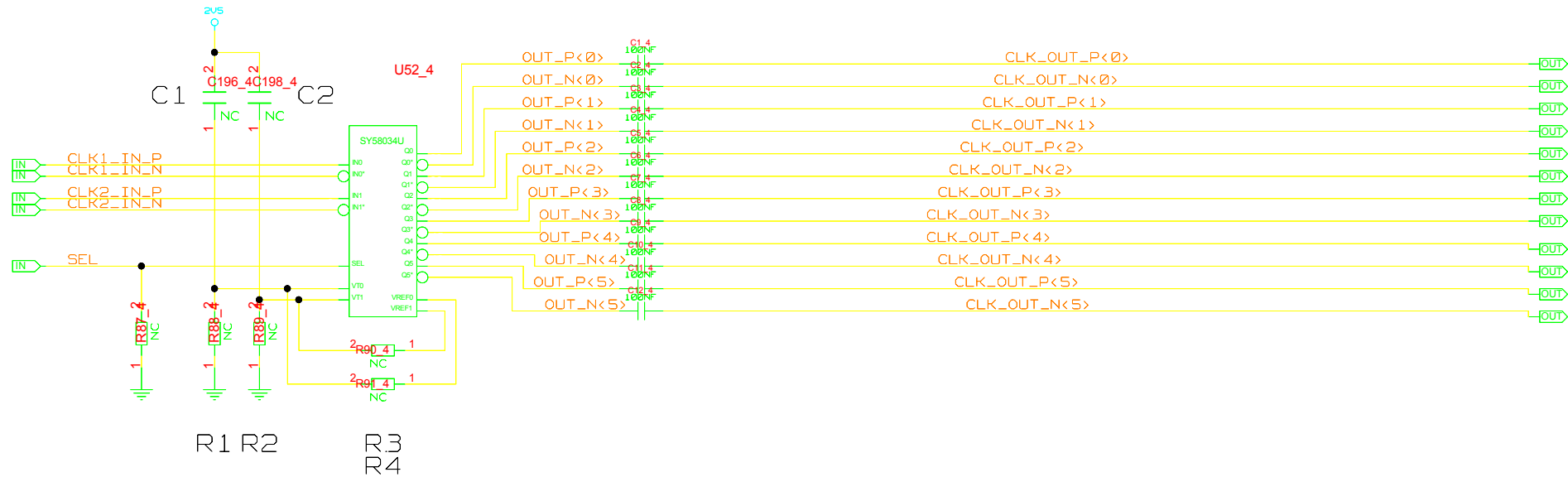
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

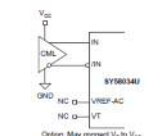


Figure 3a. CML Interface (DC-Coupled)

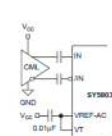


Figure 3b. CML Interface (AC-Coupled)

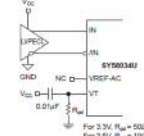


Figure 3c. LVPECL Interface (DC-Coupled)

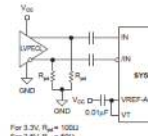


Figure 3d. LVPECL Interface (AC-Coupled)

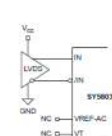


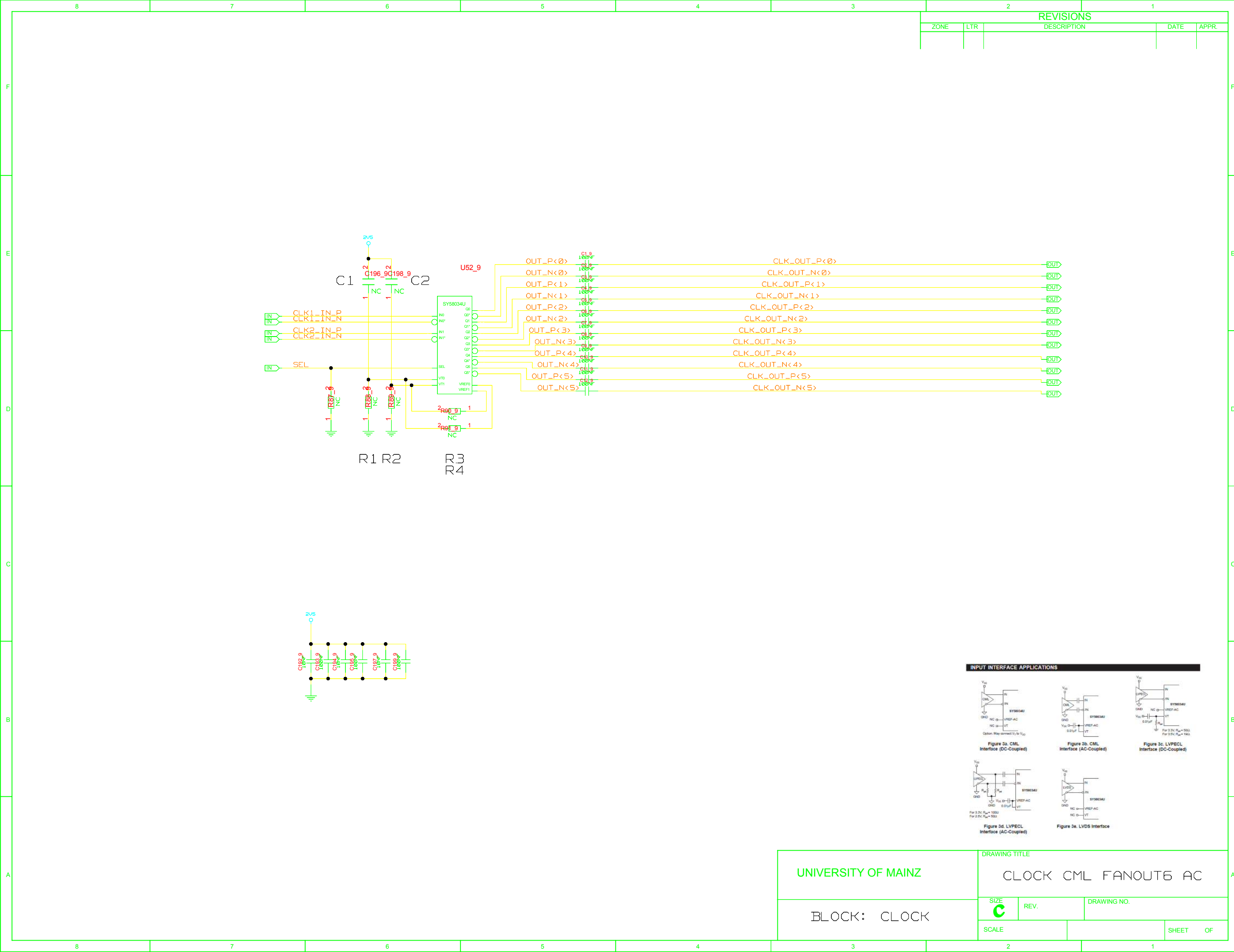
Figure 3e. LVDS Interface

UNIVERSITY OF MAINZ

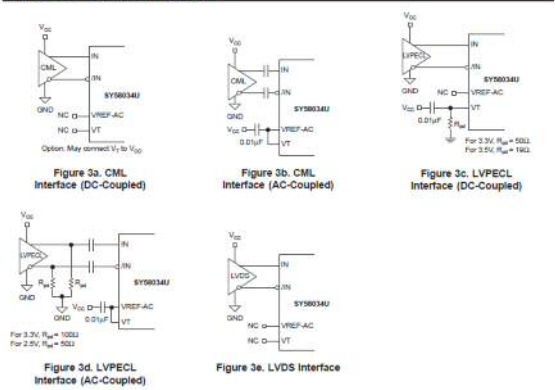
DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

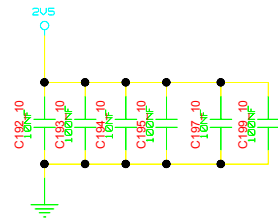
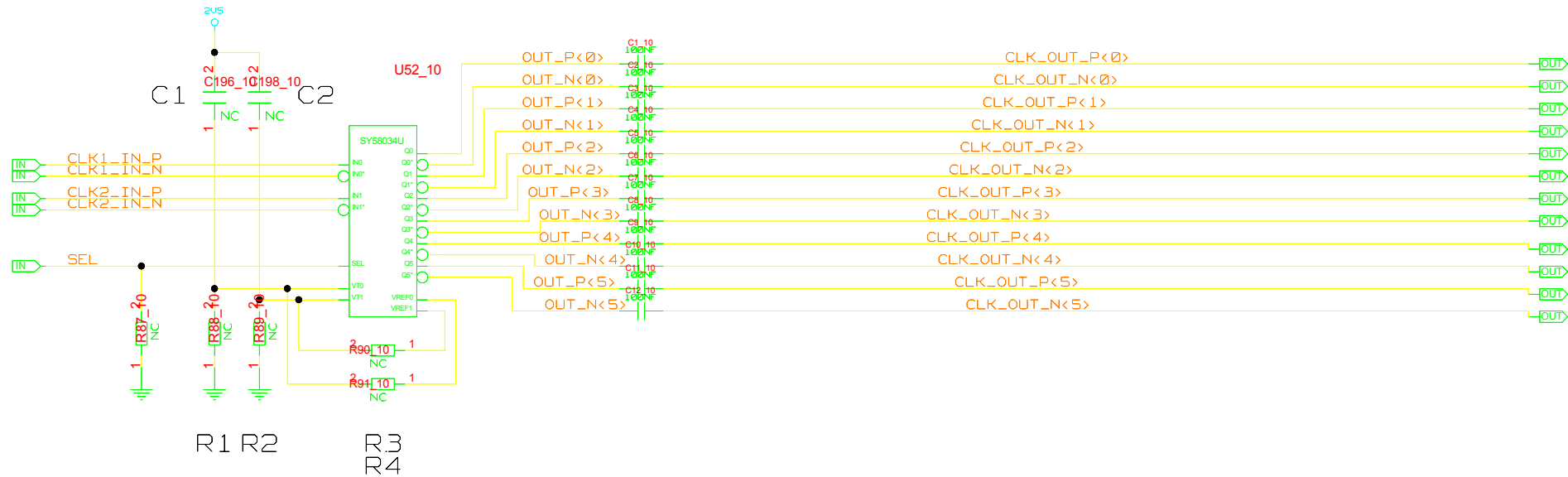


INPUT INTERFACE APPLICATIONS



UNIVERSITY OF MAINZ		DRAWING TITLE		
BLOCK: CLOCK		CLOCK CML FANOUT6 AC		
SIZE	REV.	DRAWING NO.		
SCALE			SHEET	OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

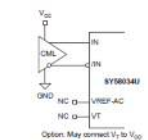


Figure 3a. CML Interface (DC-Coupled)

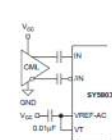


Figure 3b. CML Interface (AC-Coupled)

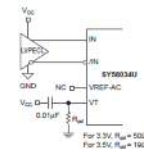


Figure 3c. LVPECL Interface (DC-Coupled)

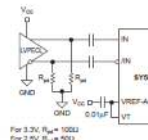


Figure 3d. LVPECL Interface (AC-Coupled)

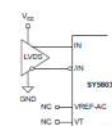


Figure 3e. LVDS Interface

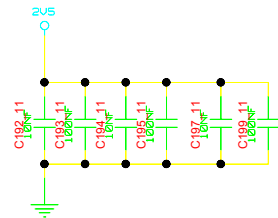
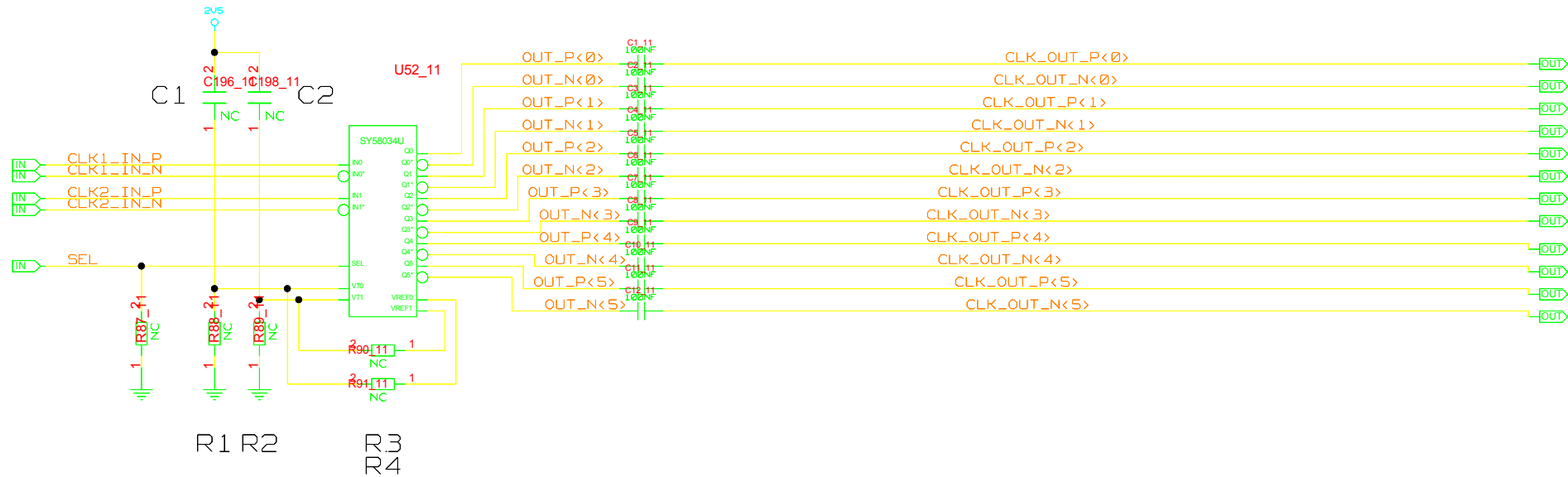
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DRAWING TITLE
CLOCK CML FANOUT6 AC

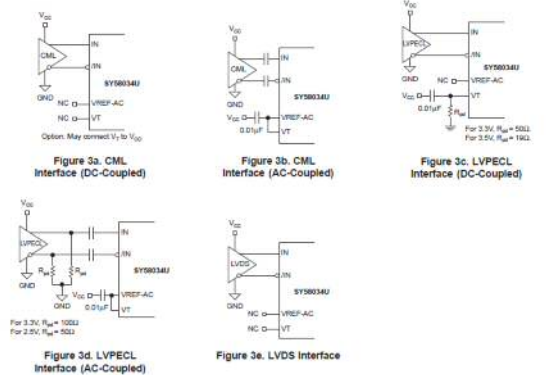
BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
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SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS



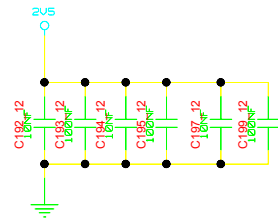
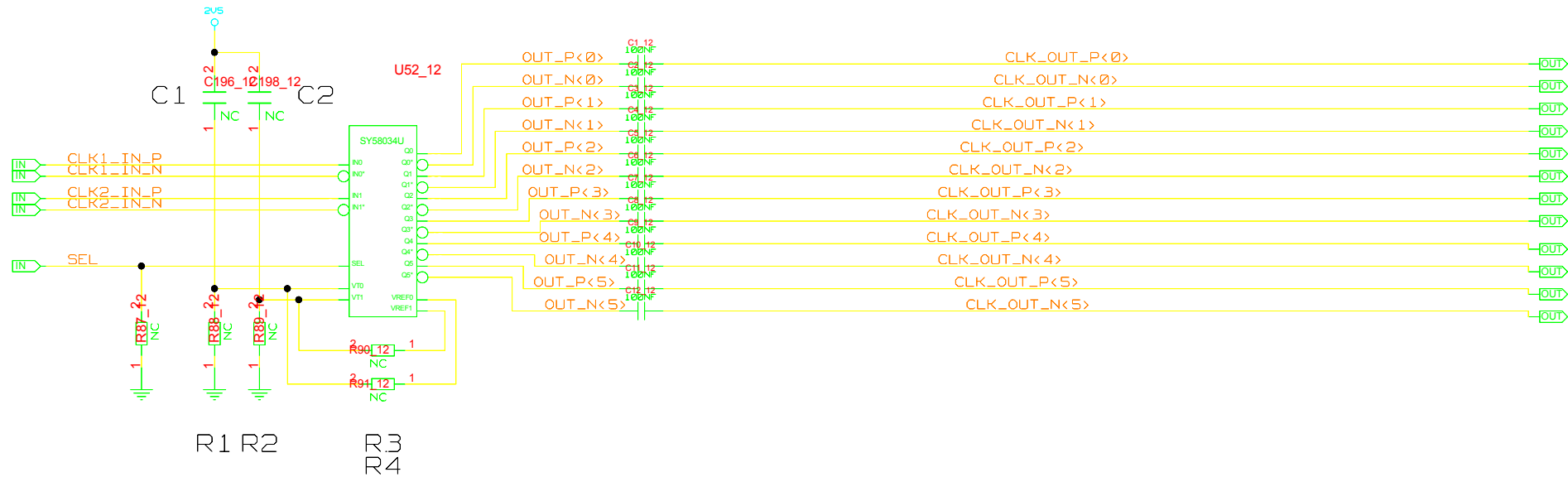
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

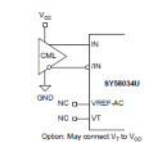


Figure 3a. CML Interface (DC-Coupled)

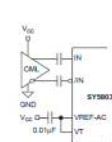


Figure 3b. CML Interface (AC-Coupled)

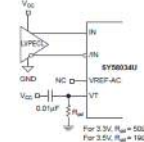


Figure 3c. LVPECL Interface (DC-Coupled)

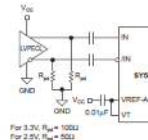


Figure 3d. LVPECL Interface (AC-Coupled)

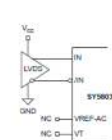


Figure 3e. LVDS Interface

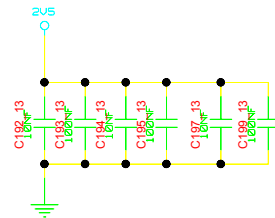
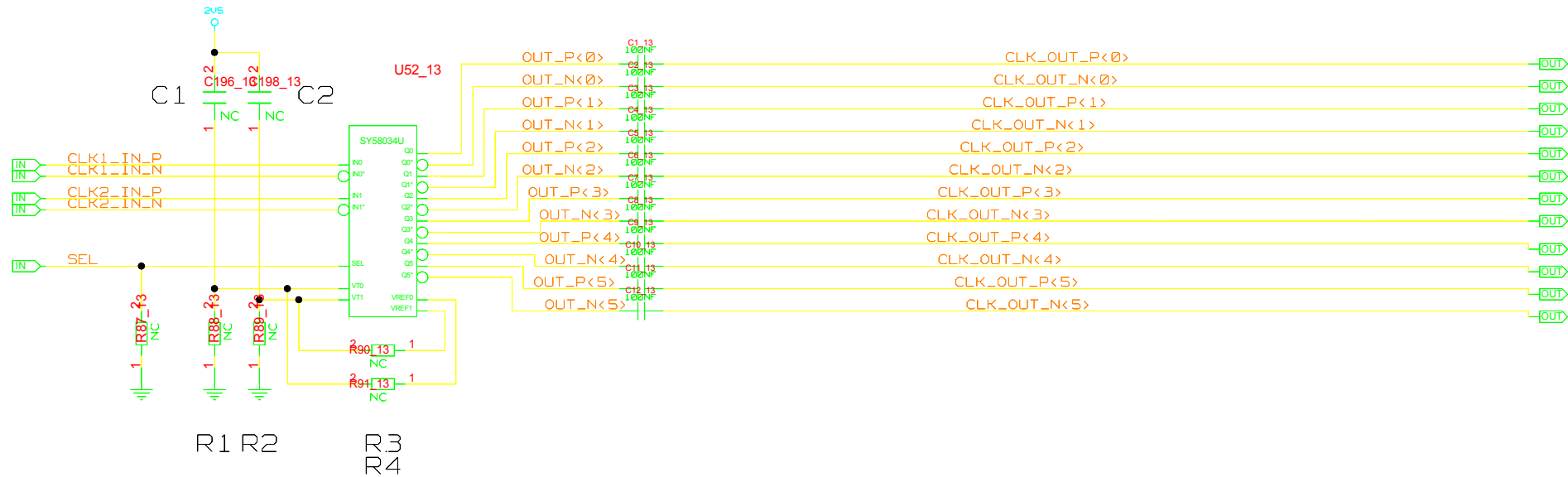
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

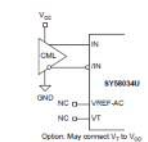


Figure 3a. CML Interface (DC-Coupled)

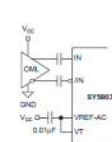


Figure 3b. CML Interface (AC-Coupled)

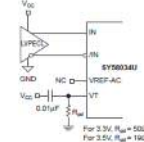


Figure 3c. LVPECL Interface (DC-Coupled)

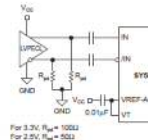


Figure 3d. LVPECL Interface (AC-Coupled)

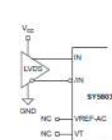


Figure 3e. LVDS Interface

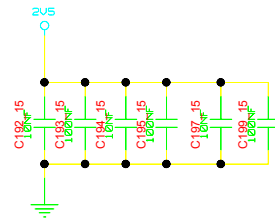
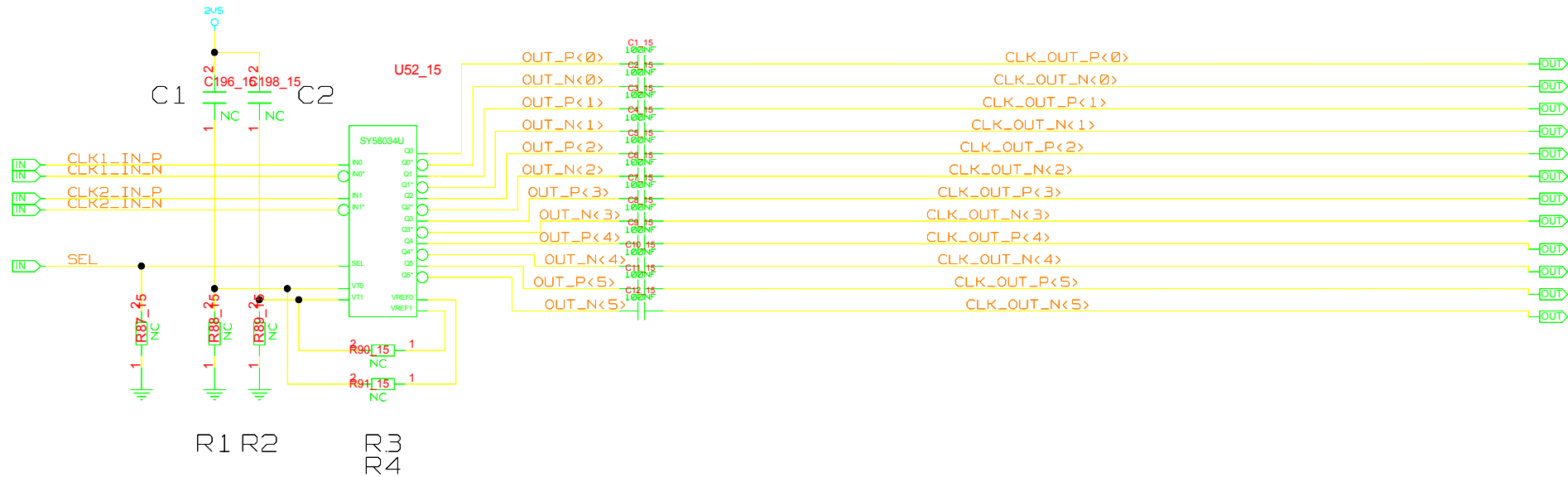
UNIVERSITY OF MAINZ

DRAWING TITLE
CLOCK CML FANOUT6 AC

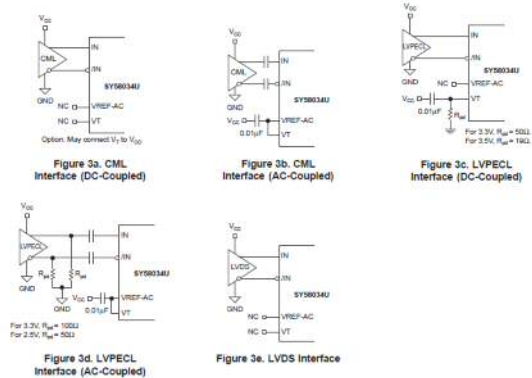
BLOCK: CLOCK

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



INPUT INTERFACE APPLICATIONS

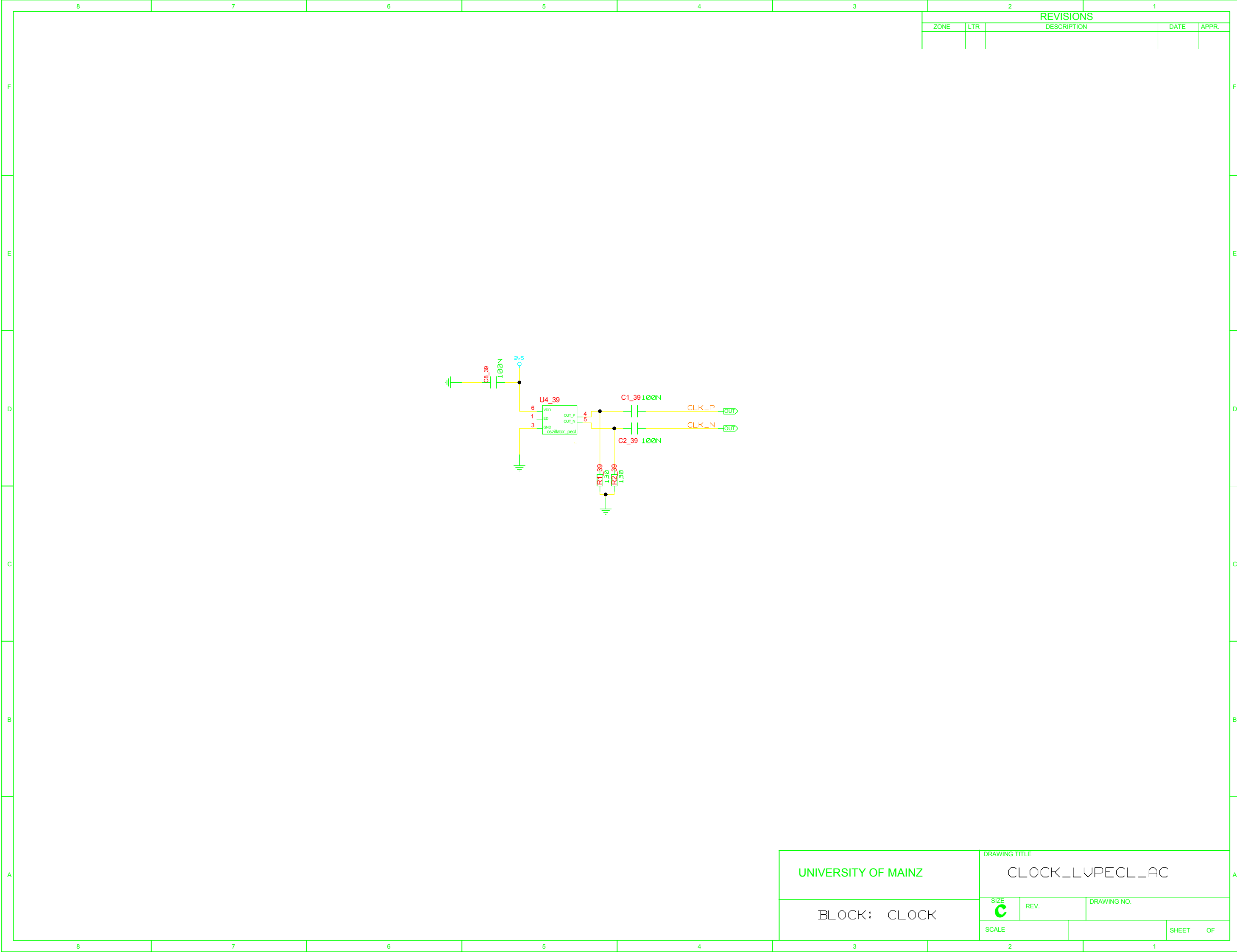


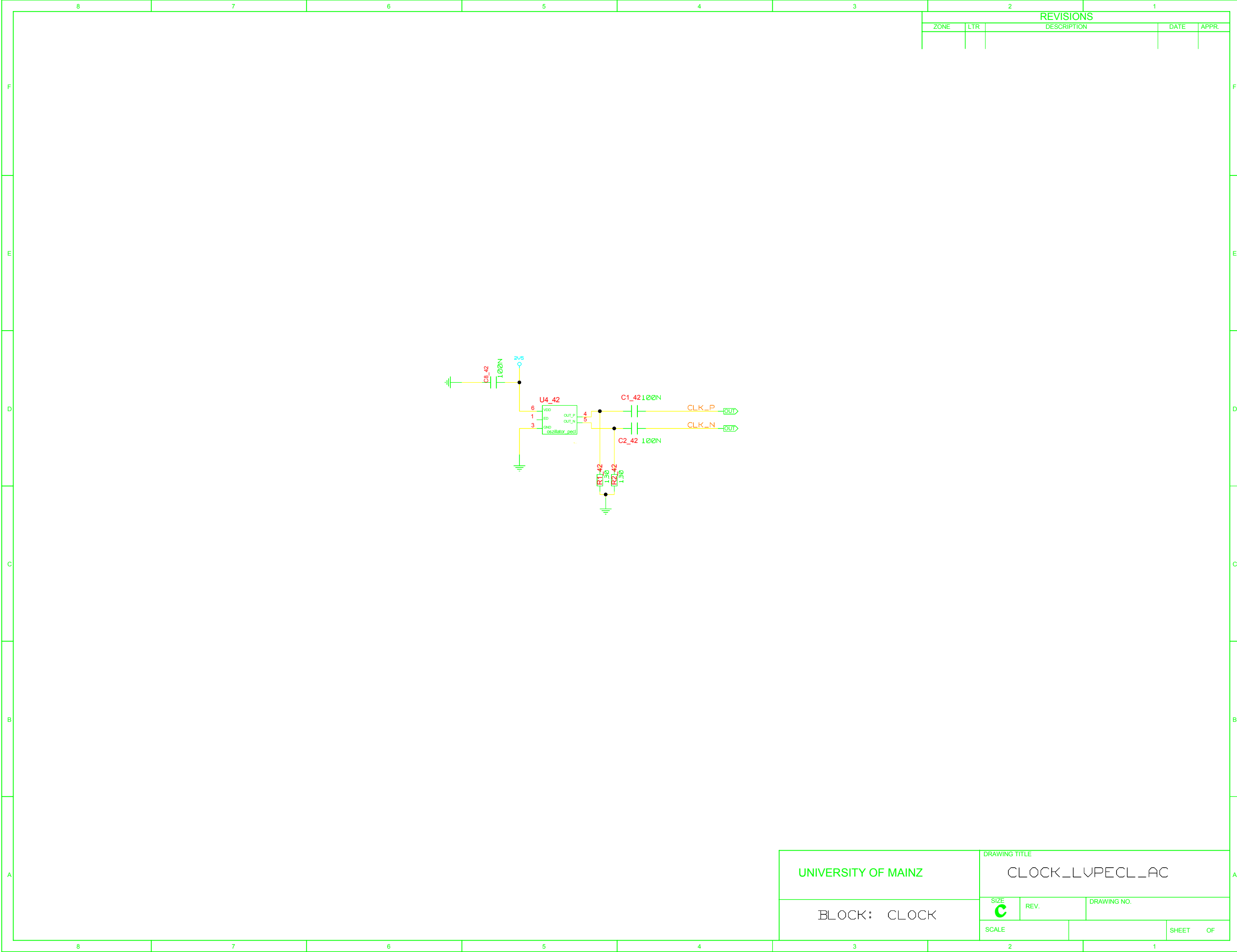
UNIVERSITY OF MAINZ

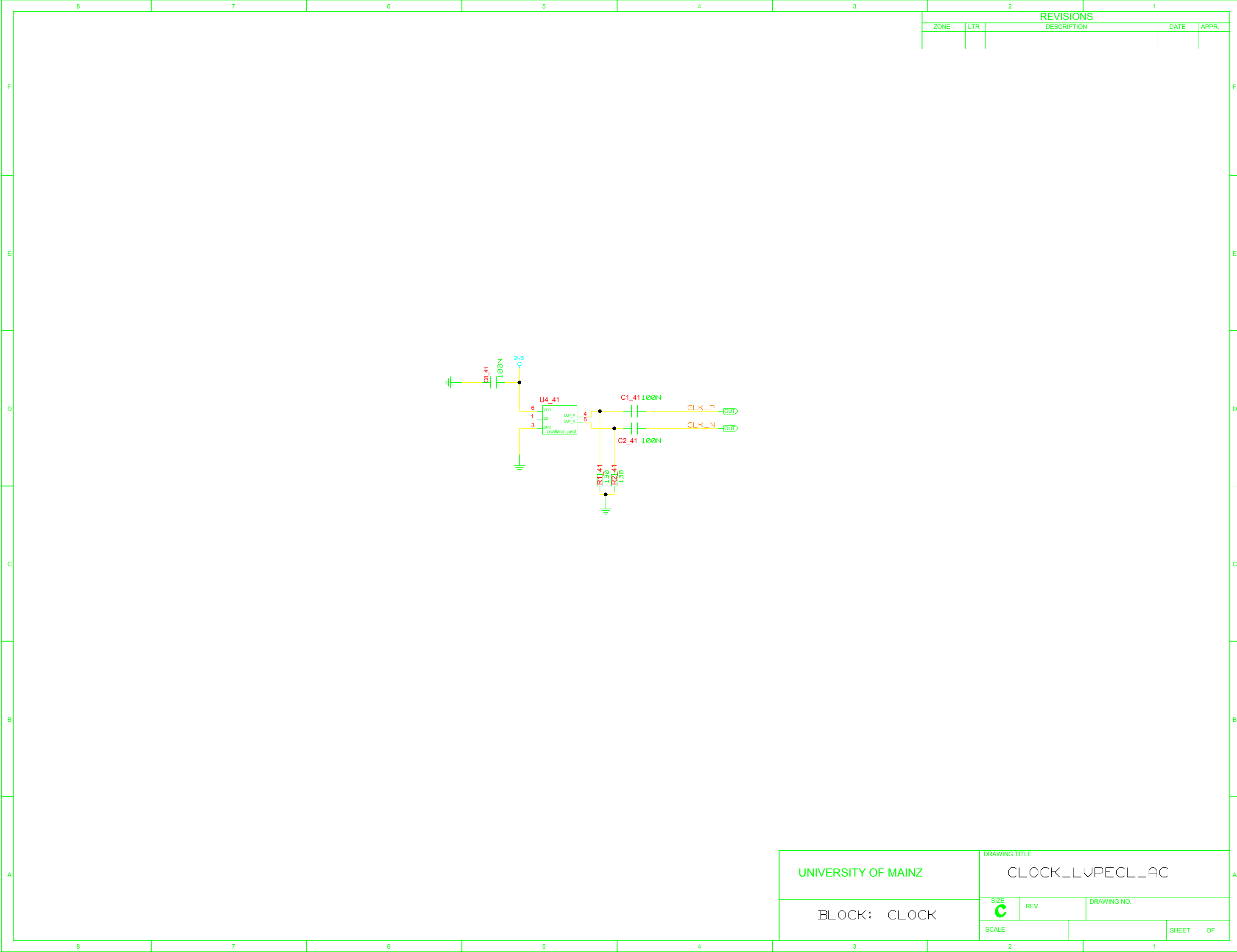
DRAWING TITLE
CLOCK CML FANOUT6 AC

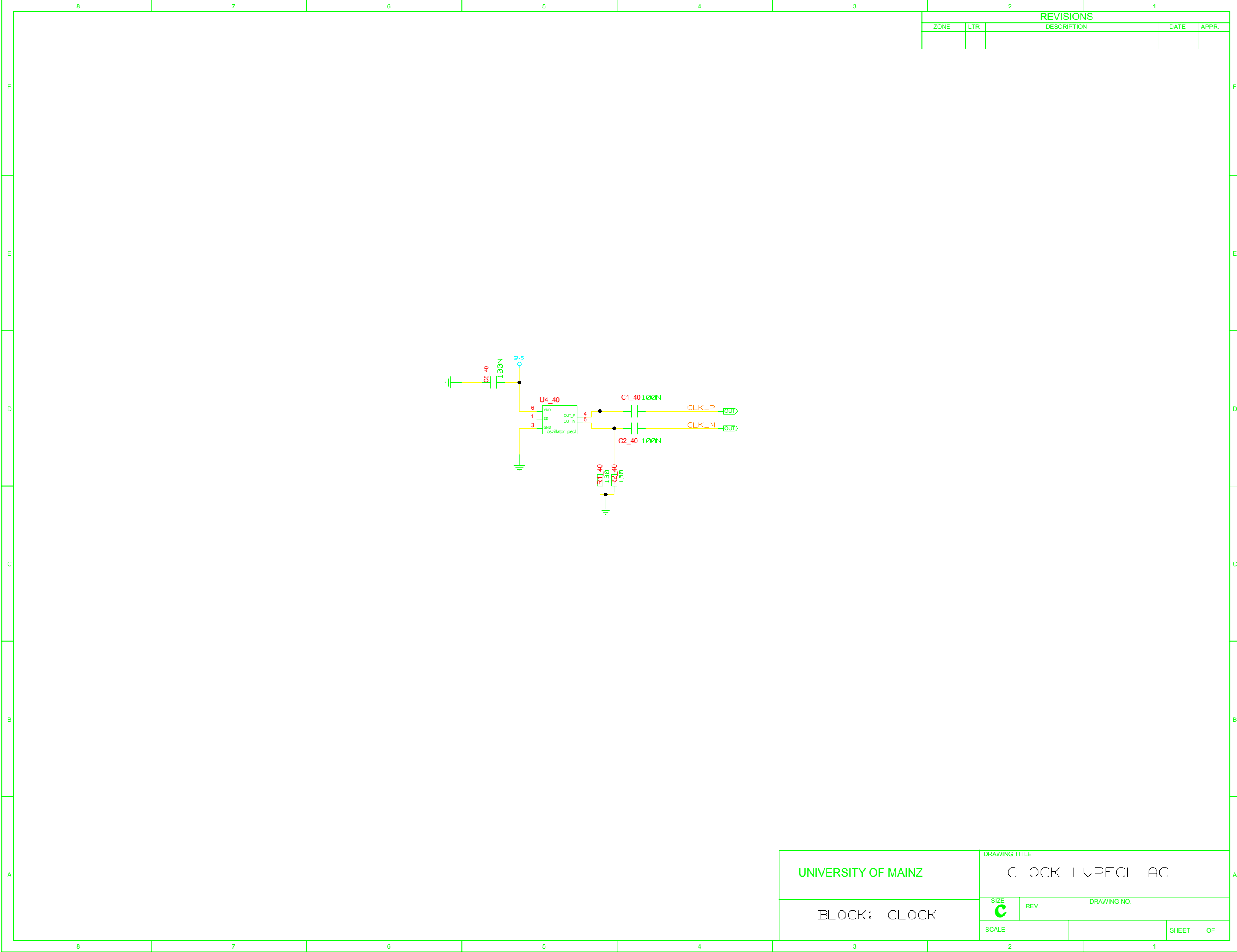
BLOCK: CLOCK

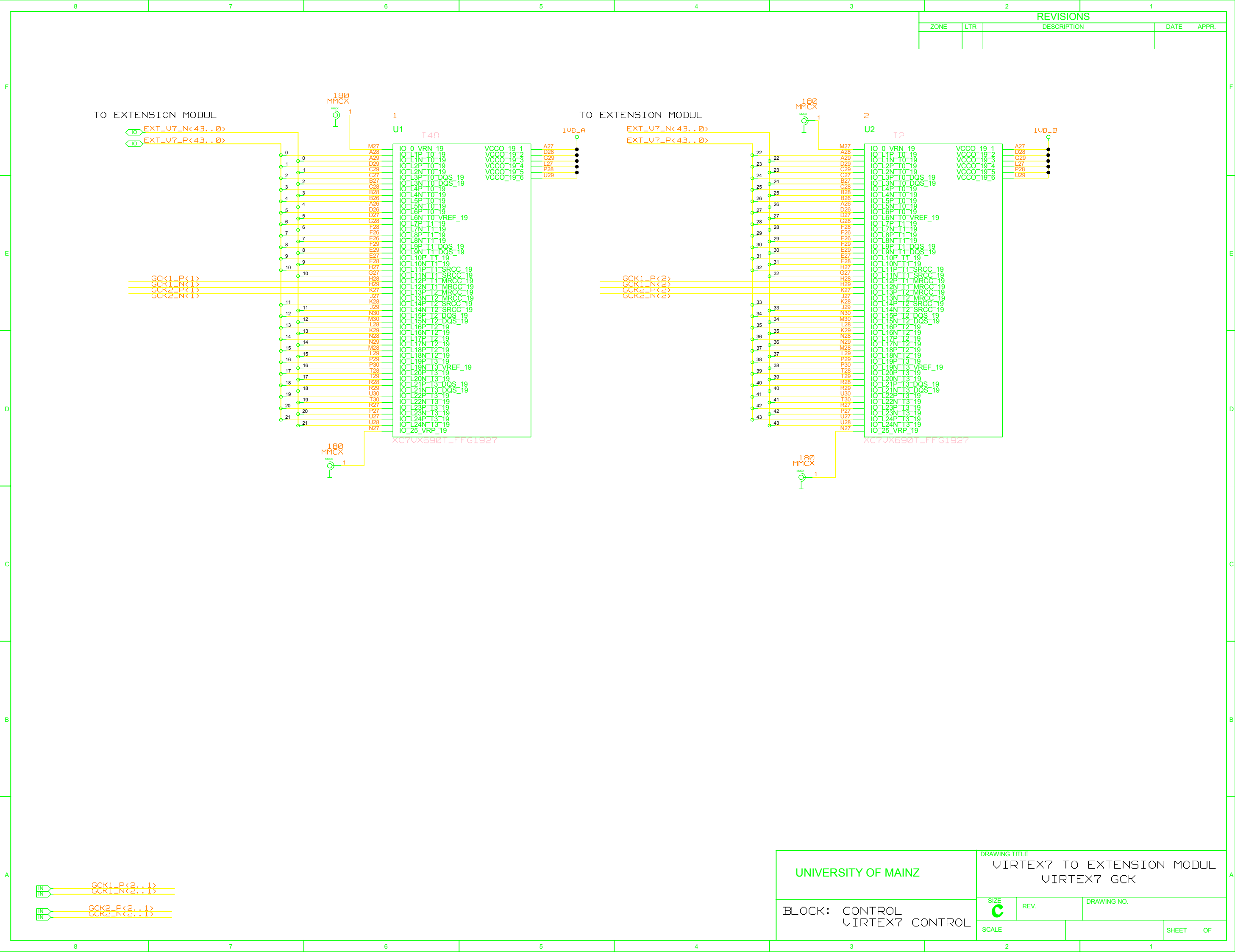
SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

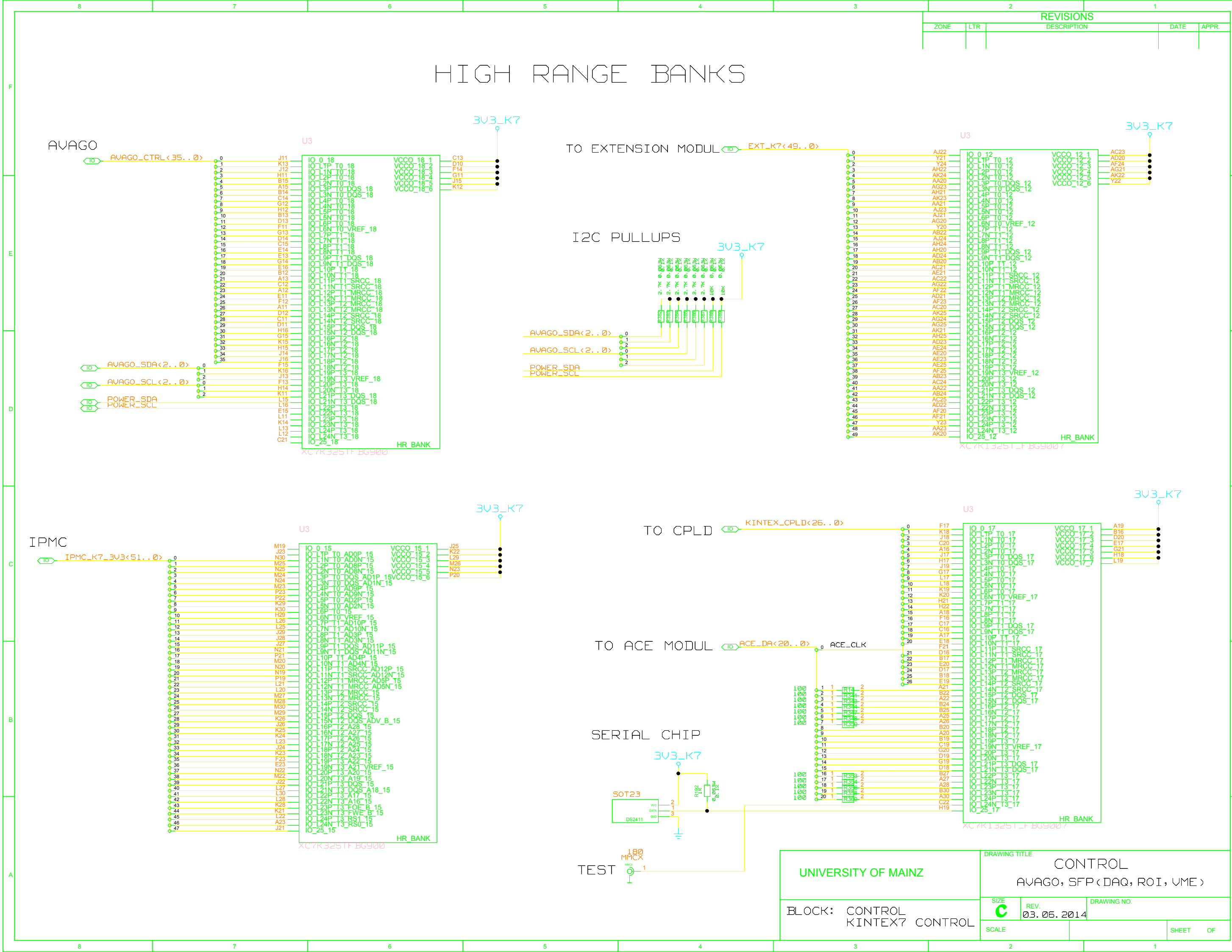




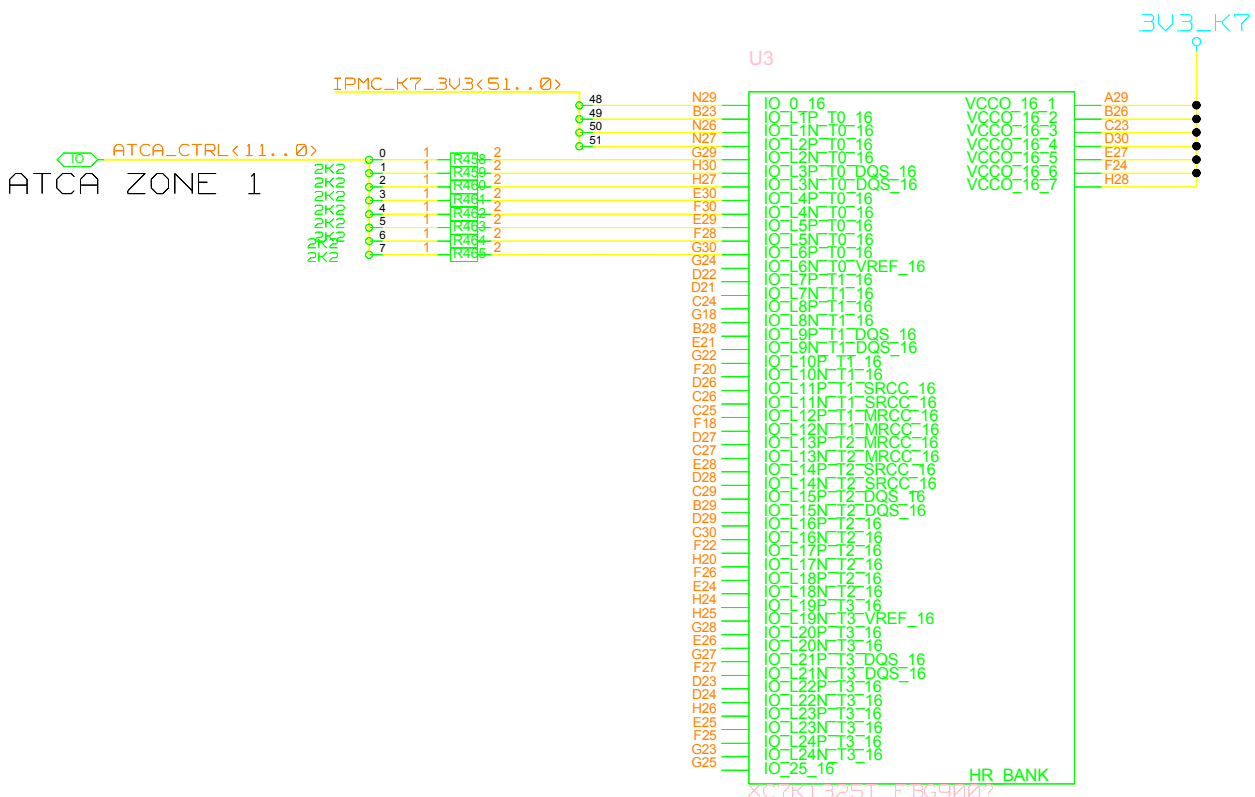








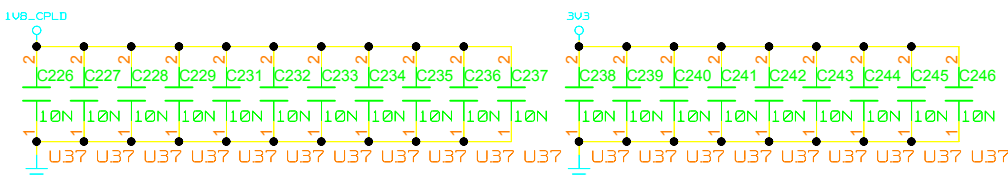
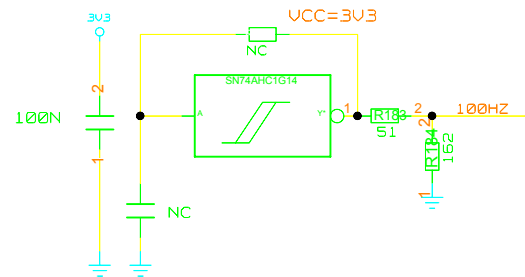
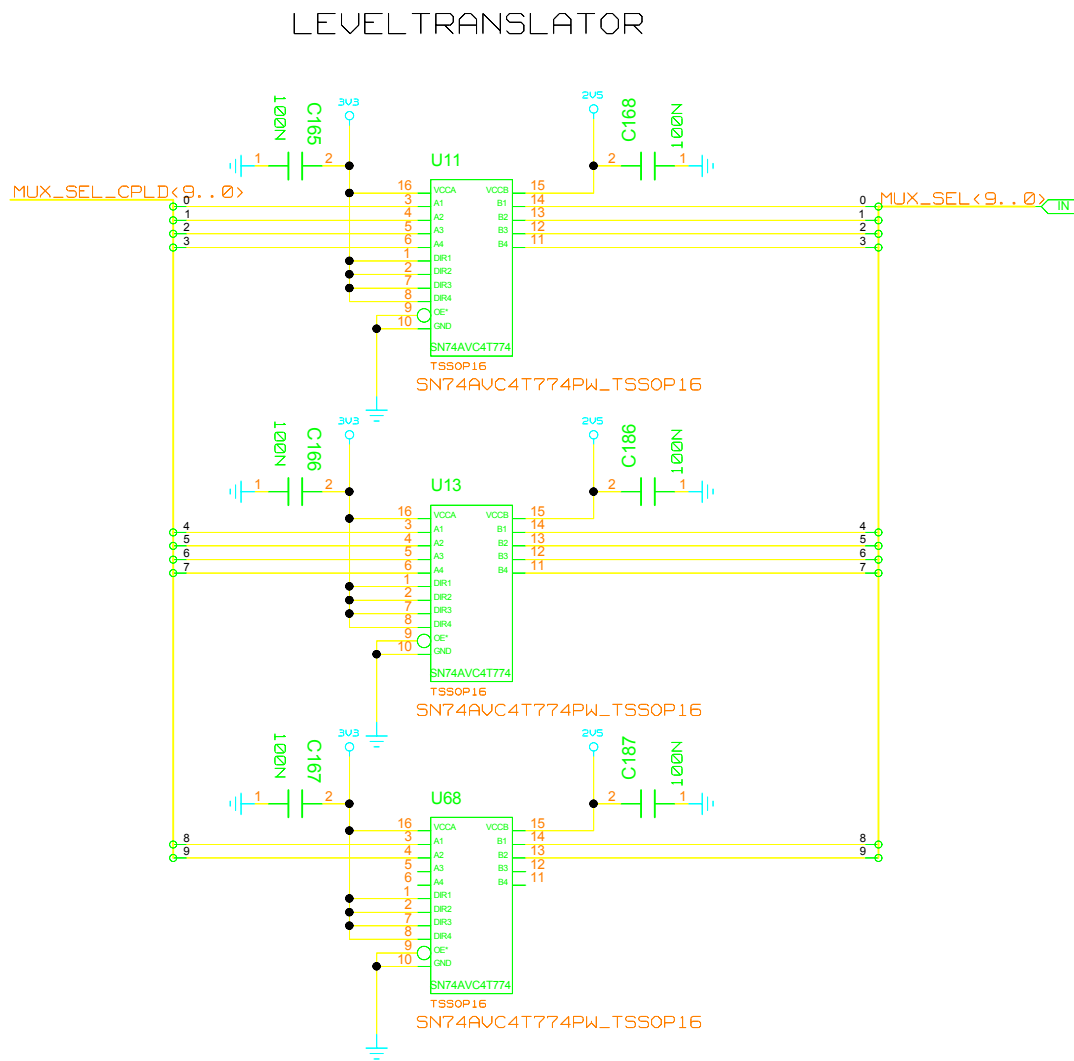
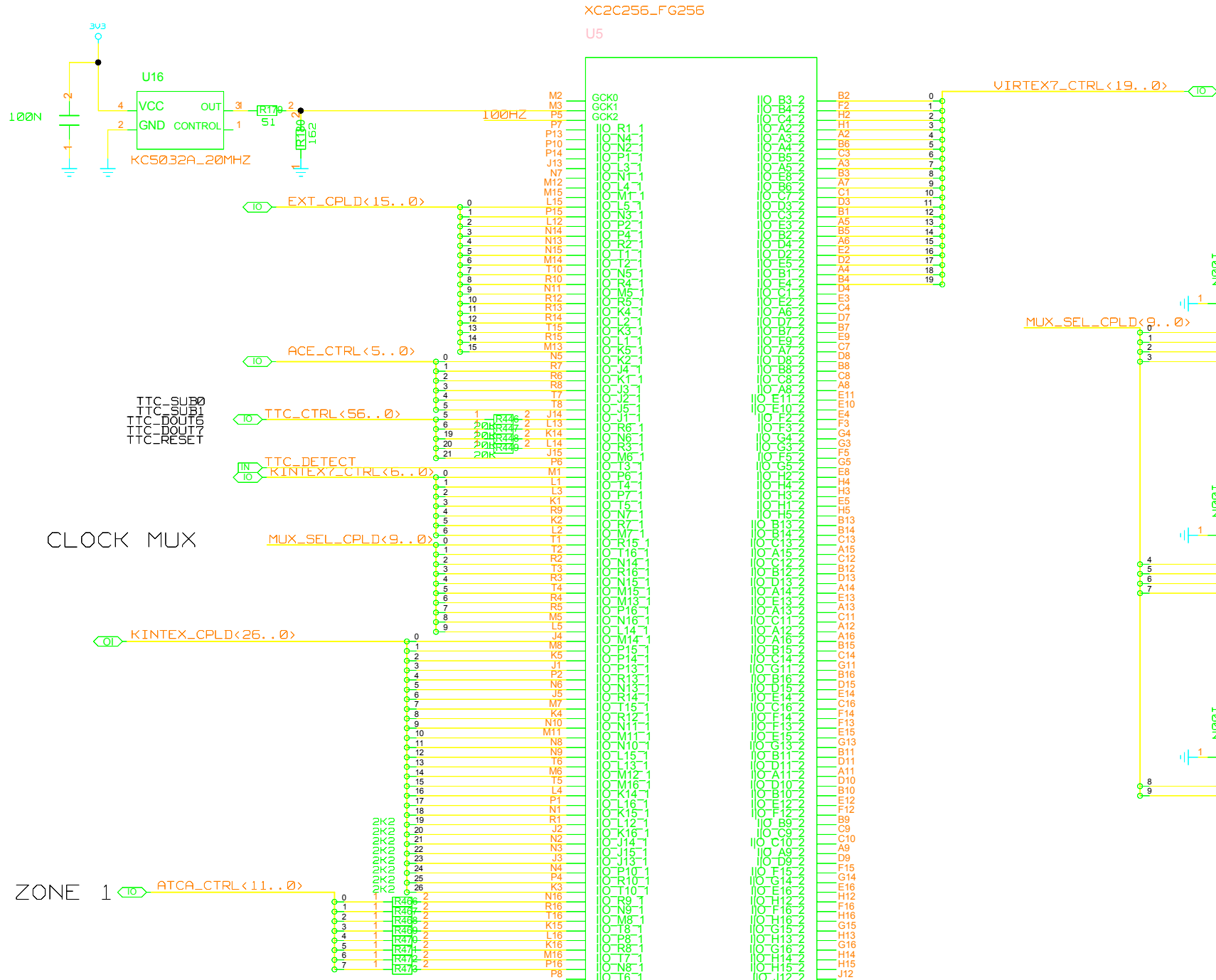
HIGH RANGE BANKS



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

UNIVERSITY OF MAINZ		DRAWING TITLE		
BLOCK: CONTROL KINTEX7 CONTROL		SIZE	REV.	DRAWING NO.
		SCALE		SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



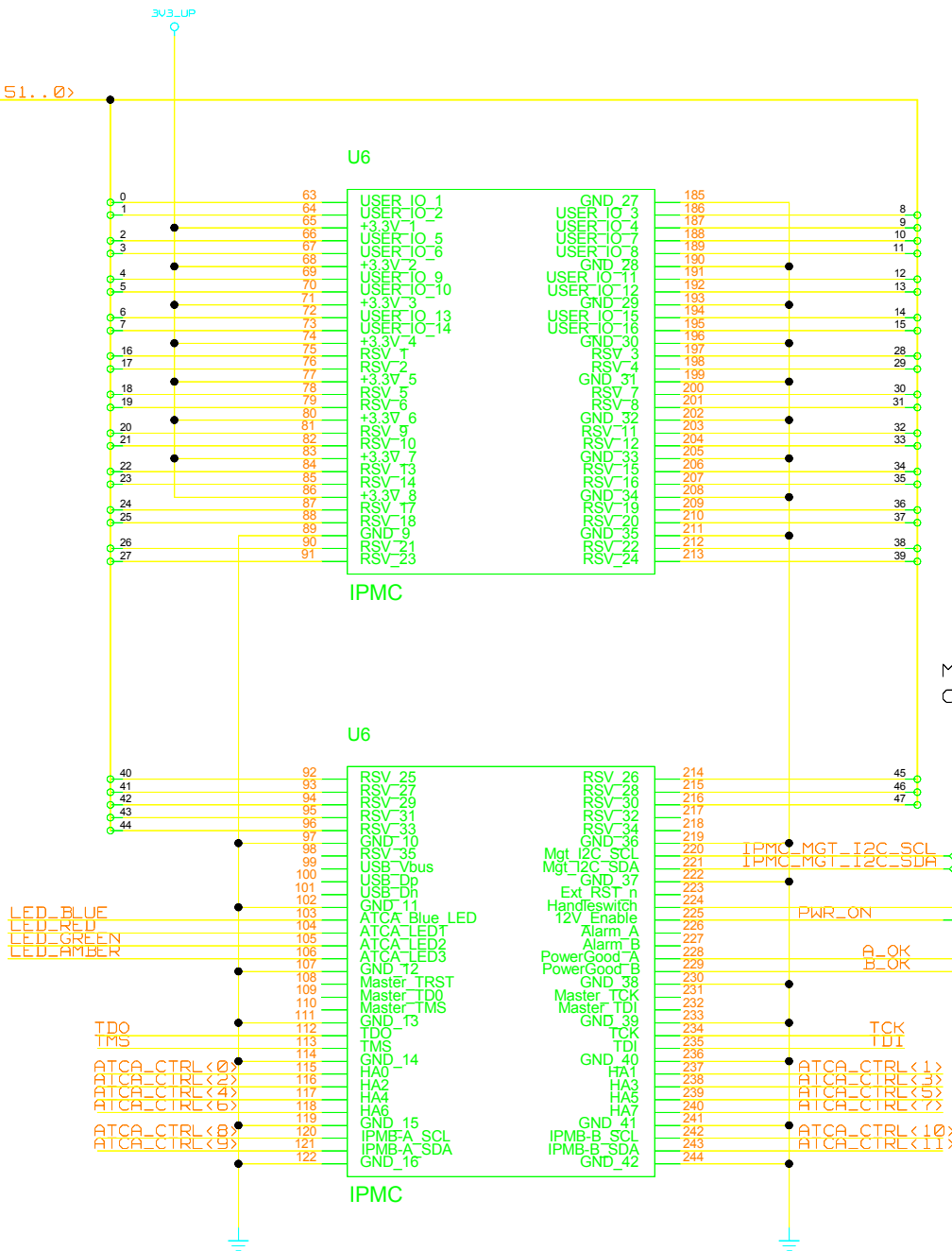
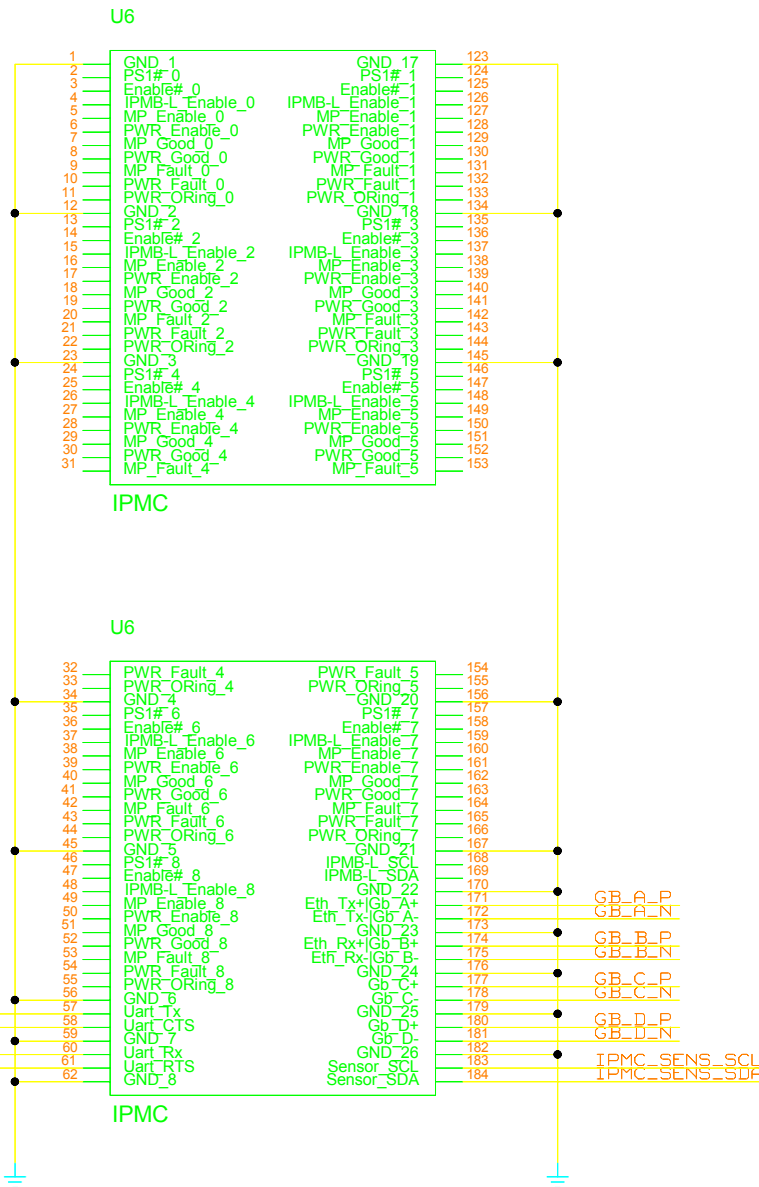
UNIVERSITY OF MAINZ		DRAWING TITLE	
BLOCK: CONTROL CPLD		CPLD	
SIZE	REV.	DRAWING NO.	
C	28.05.2014		
SCALE		SHEET	OF

IPMC MOLEX_87782-3003

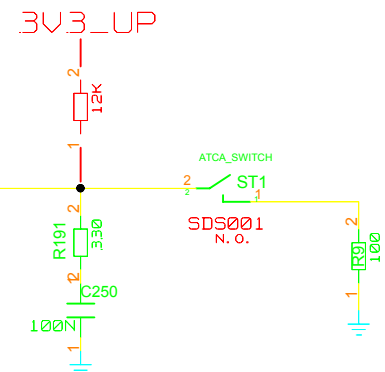
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
			APPR.

ATCA_CTRL<11..0>

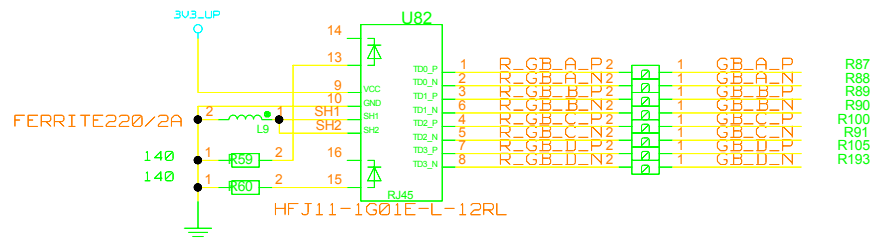
IPMC_K7_3V3<51..0>



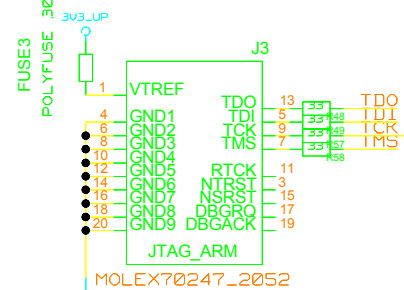
MOUNT RESISTOR NEAR TO IPMC
CHANGE ATCA SWITCH TO SDS001



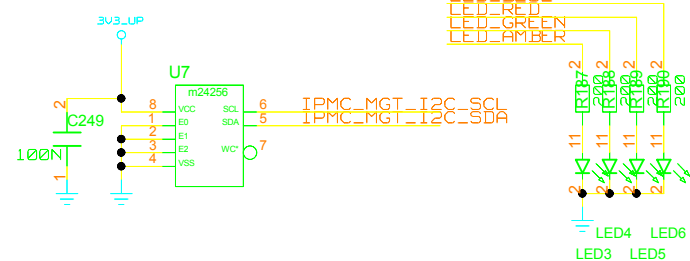
RJ45 FRONTPANEL



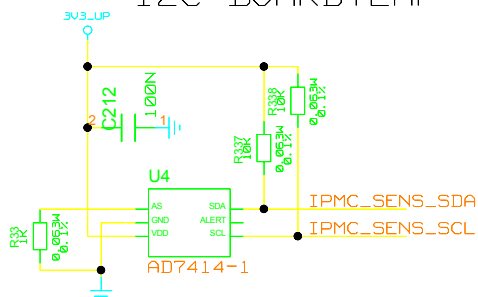
IPMC JTAG PORT FRONTPANEL



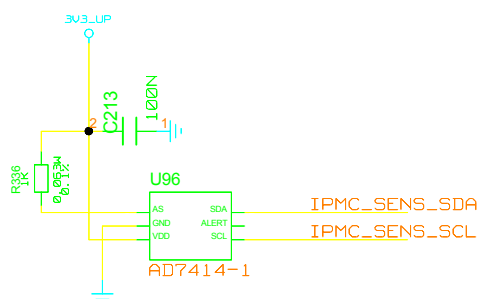
MEMORY



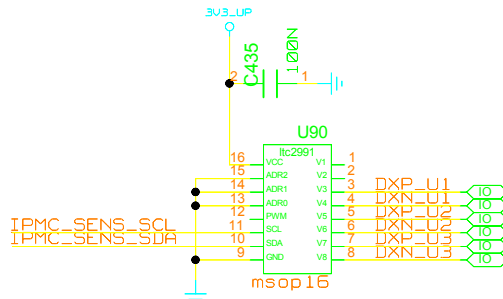
I2C BOARDTEMP



I2C BOARDTEMP



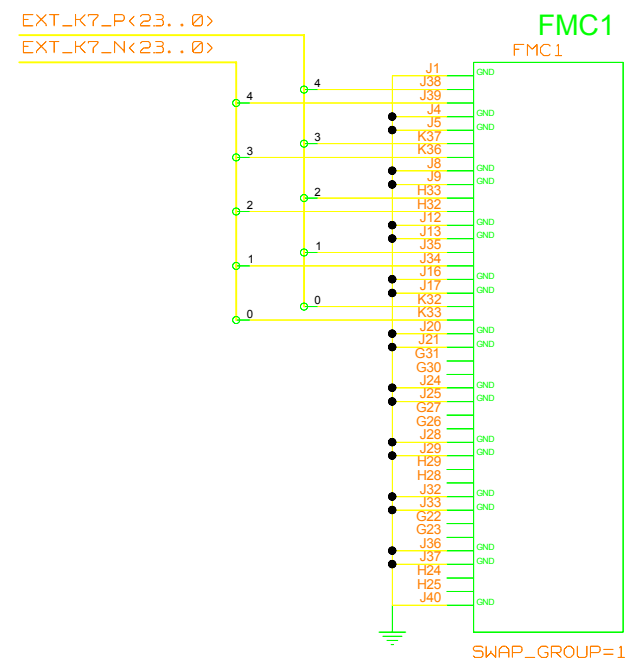
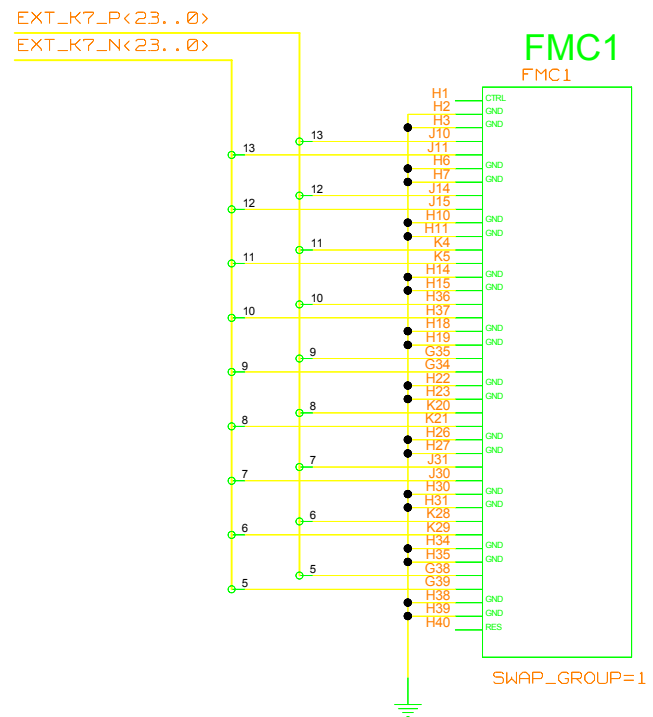
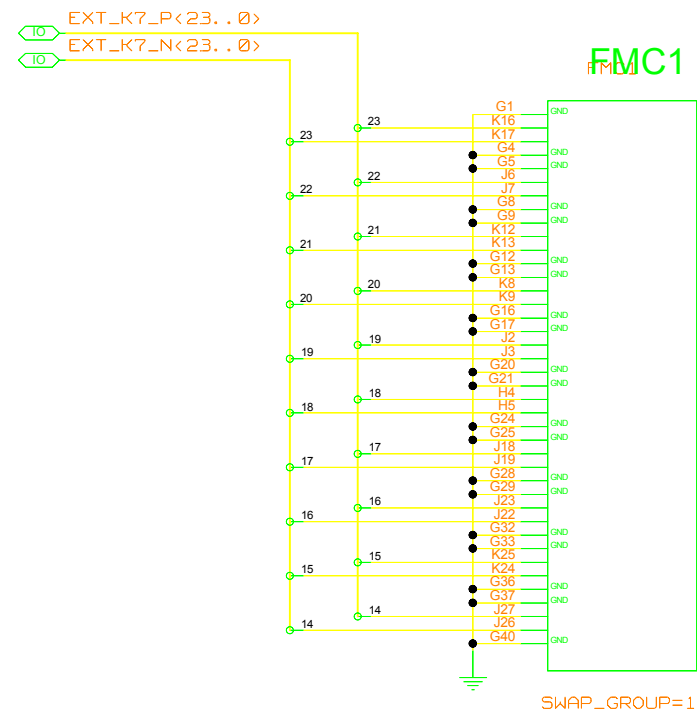
I2C FPGA TEMPERATURE

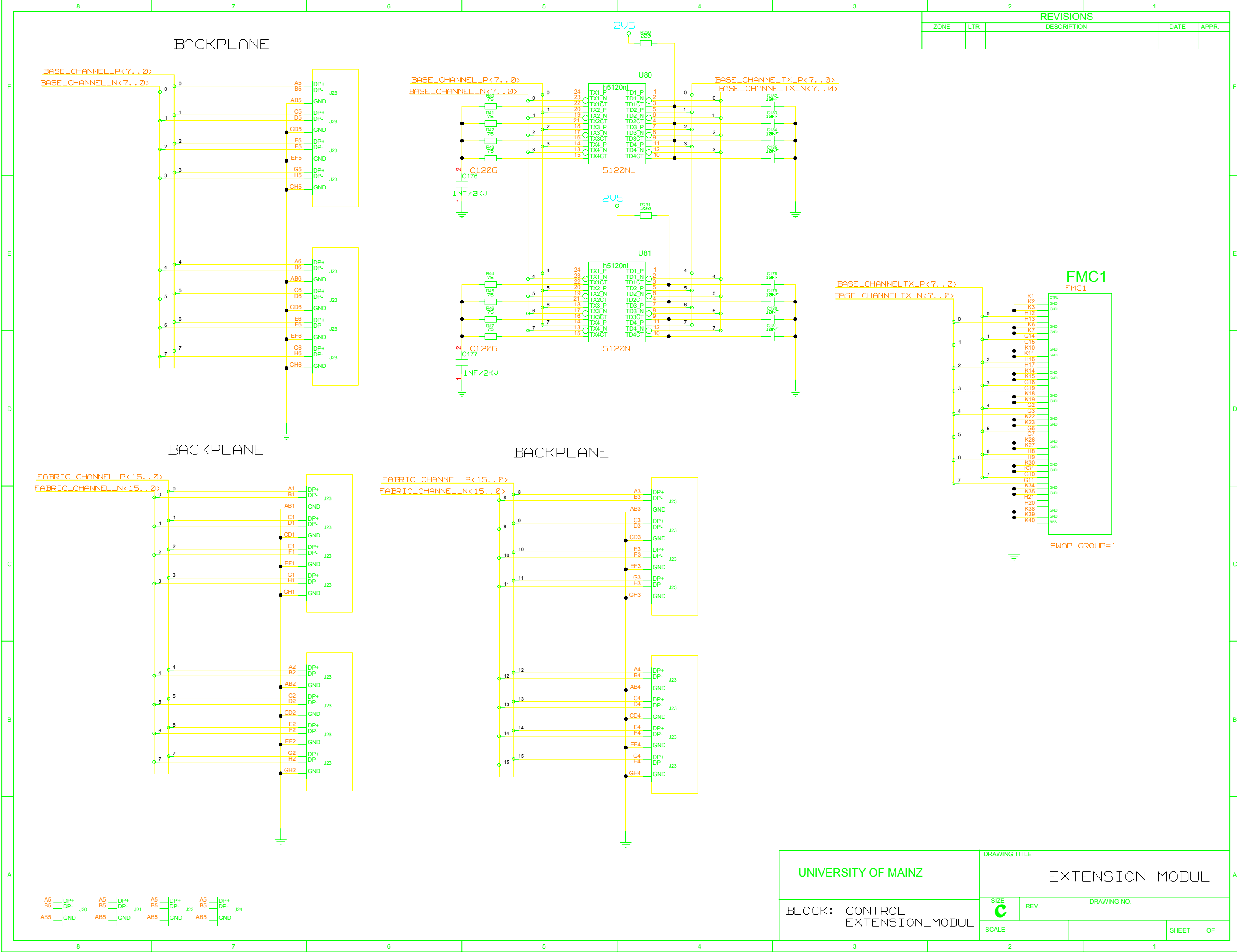


CABLE LOOP TO BACKPLANE
JTAG CONNECTOR

UNIVERSITY OF MAINZ		DRAWING TITLE	
BLOCK: CONTROL IPMC		ATCA CONTROL	
SIZE	REV.	DRAWING NO.	
SCALE		SHEET OF	

		2	1	
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.





BACKPLANE

FABRIC_CHANNEL_P<15..0>
FABRIC_CHANNEL_N<15..0>

A3
B3

DP+
DP-

J23

AB3

GND

J23

C3
D3

DP+
DP-

J23

CD3

GND

J23

E3
F3

DP+
DP-

J23

EF3

GND

J23

G3
H3

DP+
DP-

J23

GH3

GND

J23

12

13

14

15

A4
B4

DP+
DP-

J23

AB4

GND

J23

C4
D4

DP+
DP-

J23

CD4

GND

J23

E4
F4

DP+
DP-

J23

EF4

GND

J23

G4
H4

DP+
DP-

J23

GH4

GND

J23

2V5

U80

h5120nl

2V5

U81

h5120nl

BASE_CHANNEL_TX_P<7..0>
BASE_CHANNEL_TX_N<7..0>

BASE_CHANNEL_TX_P<7..0>
BASE_CHANNEL_TX_N<7..0>

U80

h5120nl

U81

h5120nl

BASE_CHANNEL_TX_P<7..0>
BASE_CHANNEL_TX_N<7..0>

FMC1

FMC1

SWAP_GROUP=1

UNIVERSITY OF MAINZ

EXTENSION MODUL

BLOCK: CONTROL
EXTENSION_MODUL

DRAWING TITLE

SIZE
C

REV.

DRAWING NO.

SCALE

SHEET OF

