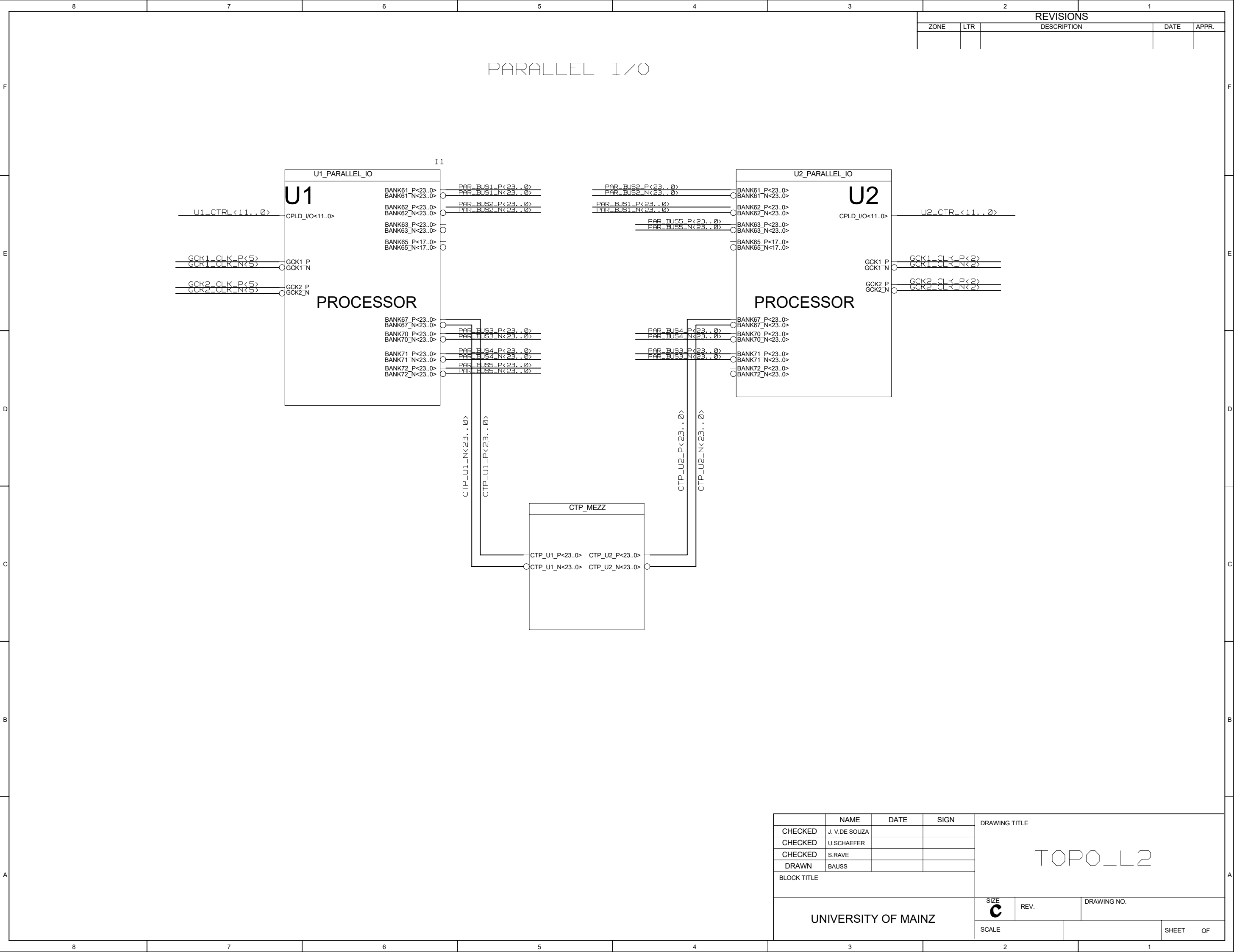
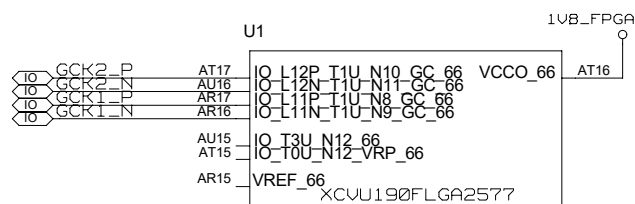
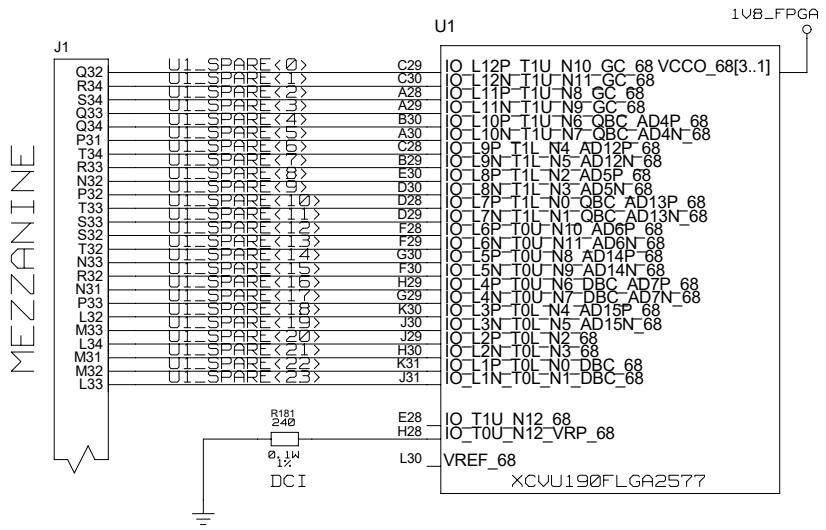


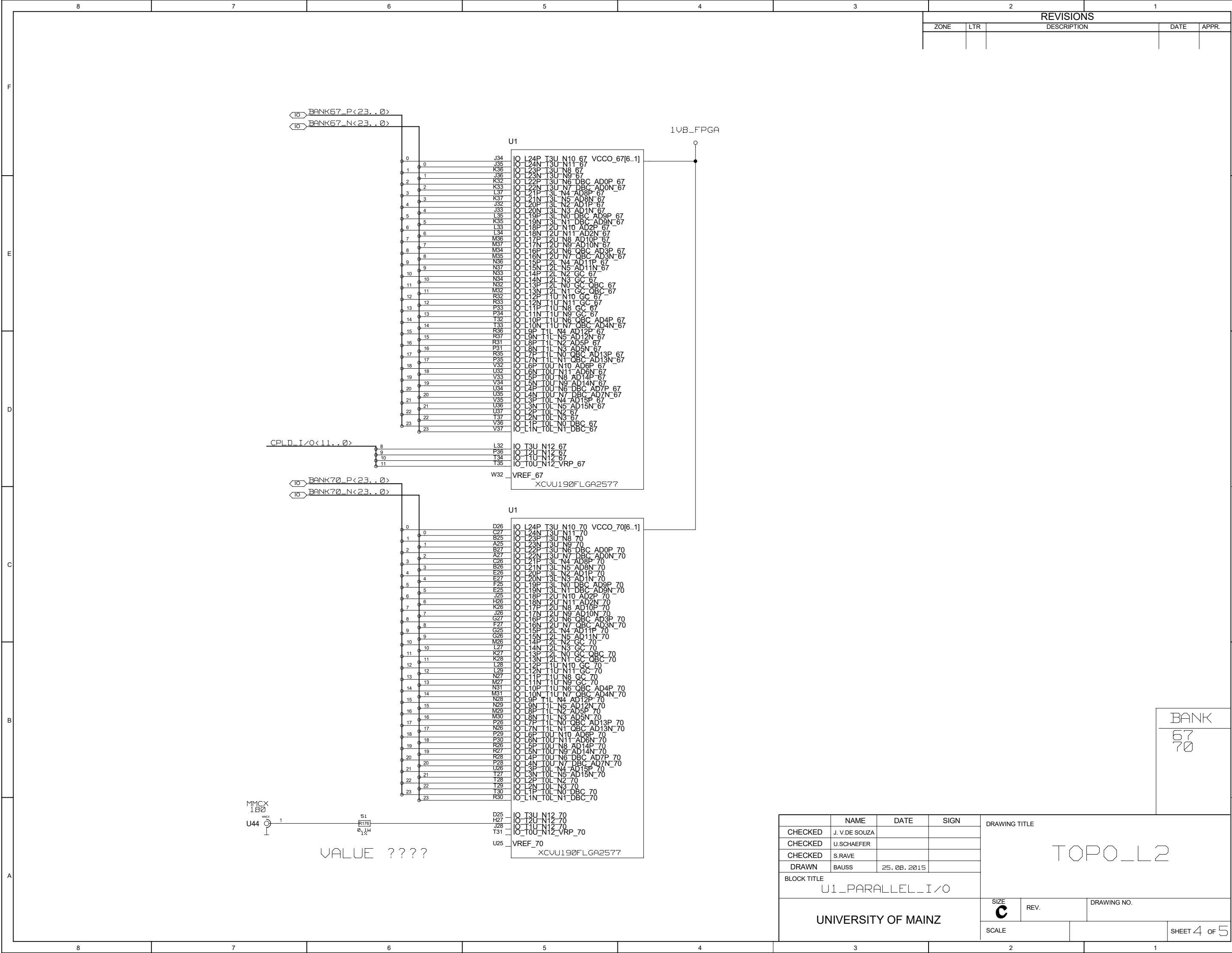




REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

BANK
66
68

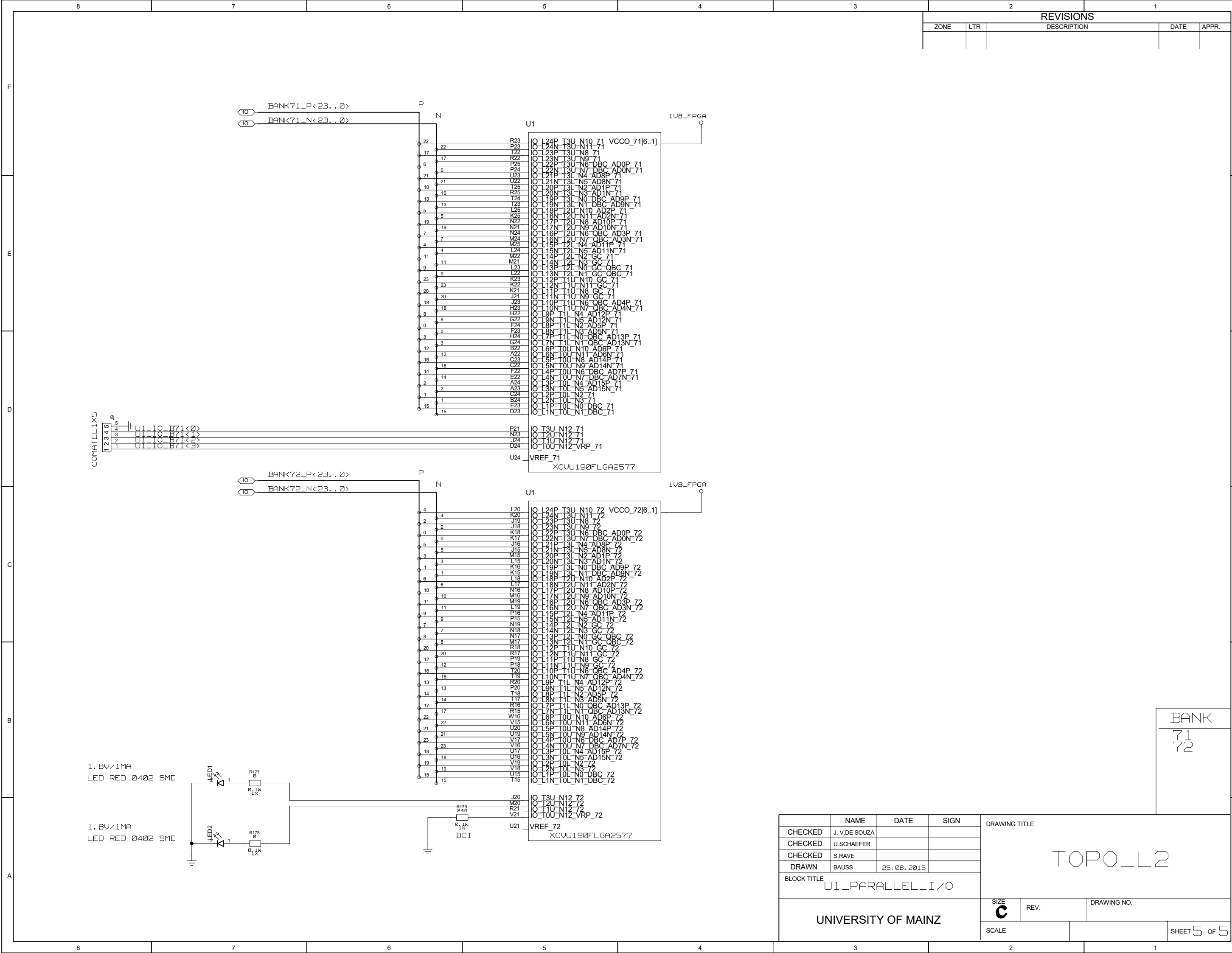
CHECKED	J. V.DE SOUZA	DATE	SIGN	DRAWING TITLE TOPO_L2	
CHECKED	U.SCHAEFER				
CHECKED	S.RAVE				
DRAWN	BAUSS	25. 08. 2015			
BLOCK TITLE U1_PARALLEL_I/O				SIZE C	REV.
UNIVERSITY OF MAINZ				DRAWING NO.	
				SCALE	SHEET 3 OF 5

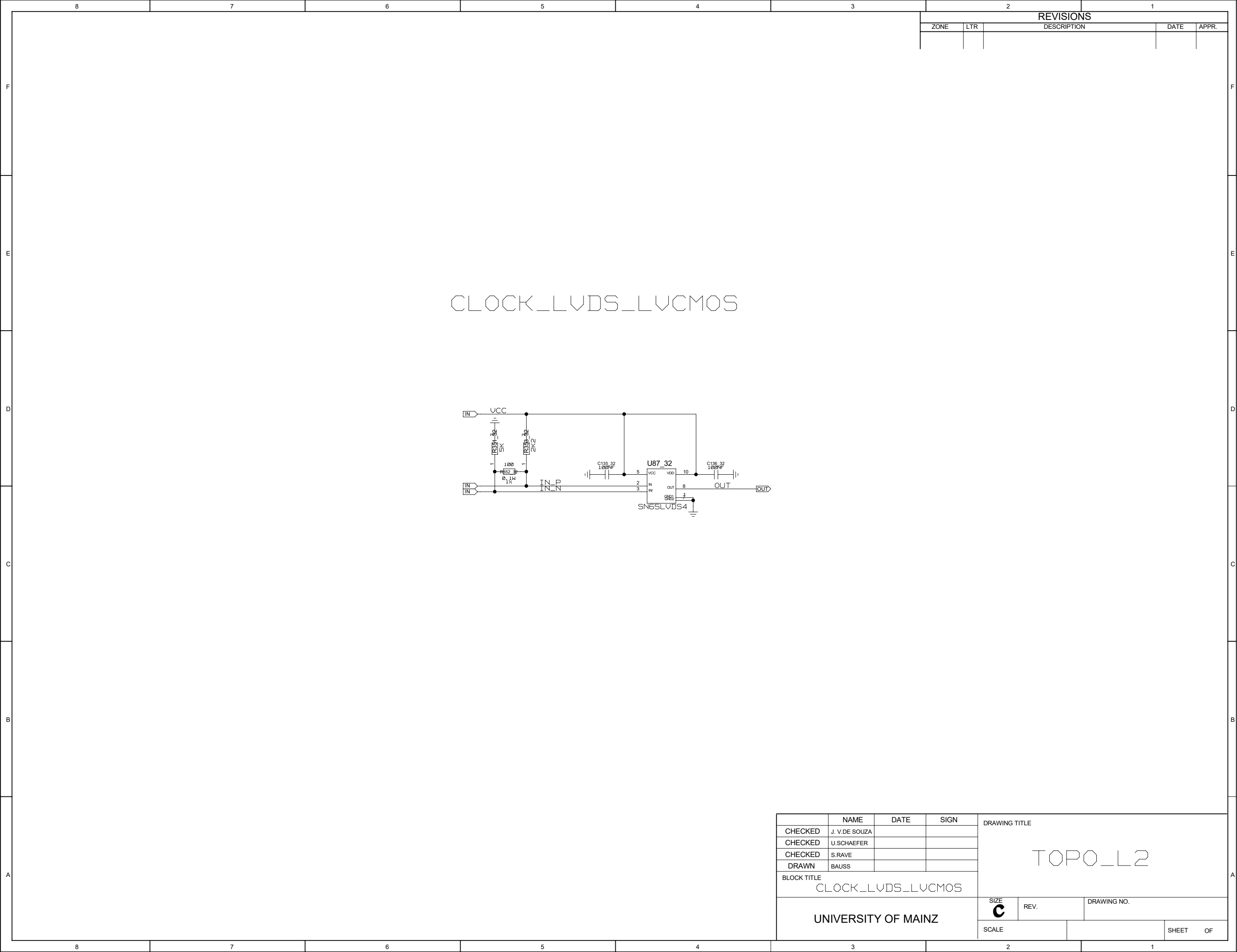


REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

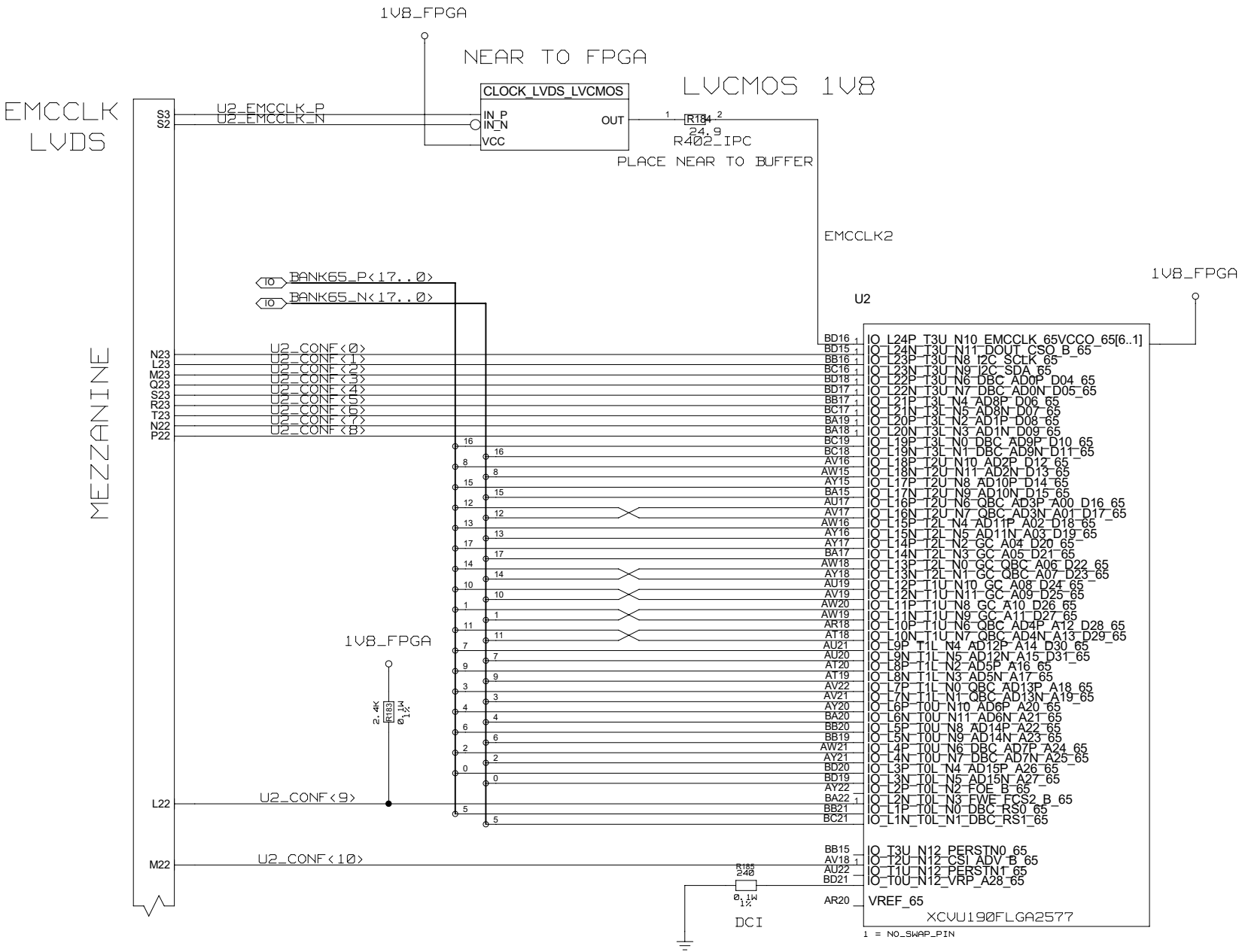
BANK
67
70

NAME	DATE	SIGN	DRAWING TITLE	
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CHECKED S.RAVE				
DRAWN BAUSS	25.08.2015			
BLOCK TITLE			U1_PARALLEL_I/O	
UNIVERSITY OF MAINZ			SIZE C	DRAWING NO.
			SCALE	SHEET 4 OF 5



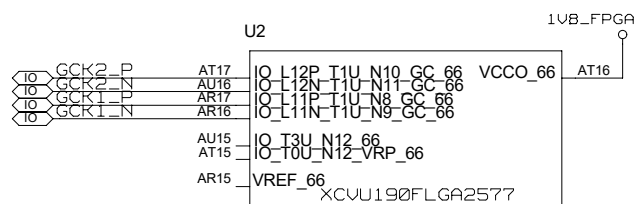
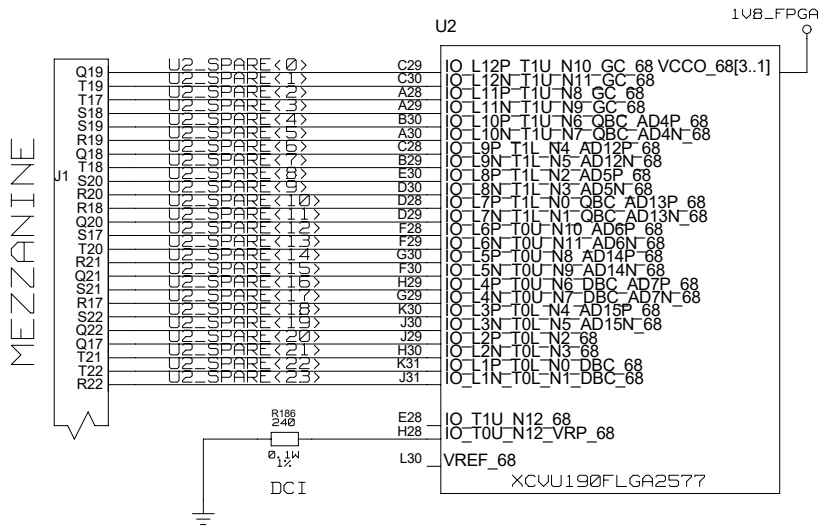


REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



BANK
65

CHECKED	NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V.DE SOUZA			TOPO_LL2	
CHECKED	U.SCHAEFER				
CHECKED	S.RAVE				
DRAWN	BAUSS	25.08.2015			
BLOCK TITLE				U2_PARALLEL_I/O	
UNIVERSITY OF MAINZ				SIZE C	DRAWING NO.
				SCALE	SHEET 2 OF 5

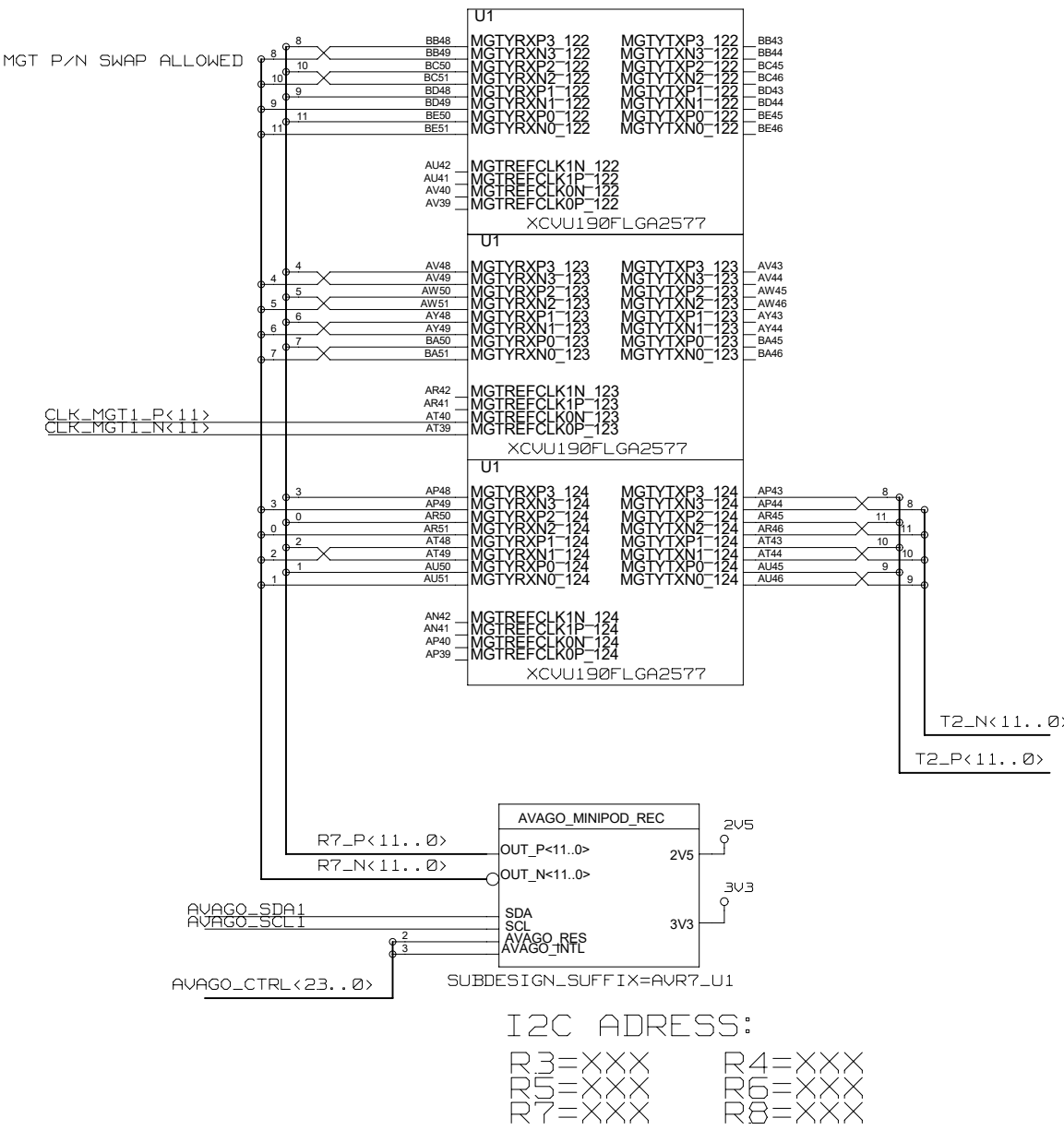
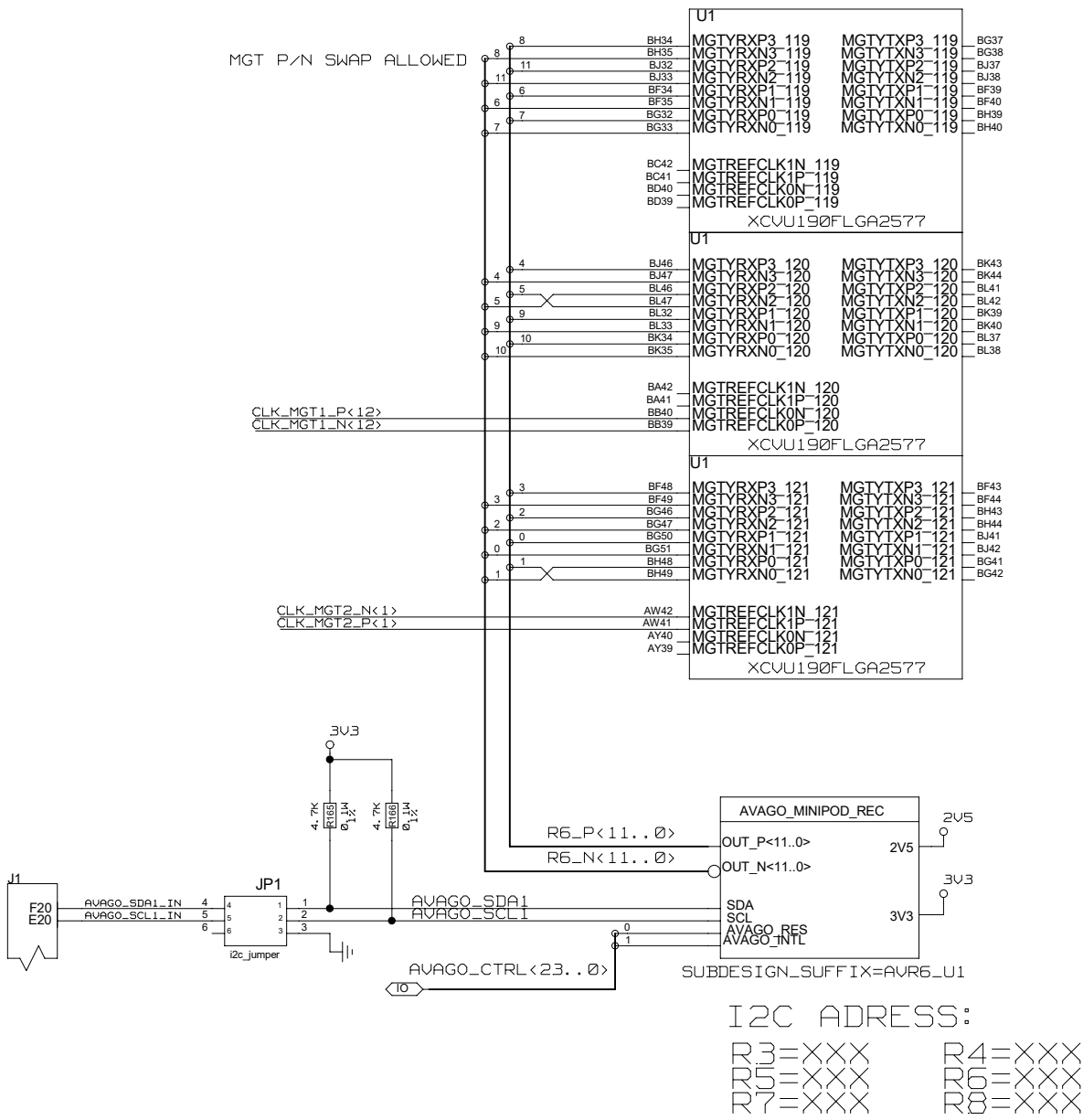


REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

BANK
66
68

CHECKED	J. V.DE SOUZA	DATE	SIGN	DRAWING TITLE TOPO_LL2	
CHECKED	U.SCHAEFER				
CHECKED	S.RAVE				
DRAWN	BAUSS	25. 08. 2015			
BLOCK TITLE U2_PARALLEL_I/O				SIZE C	REV.
UNIVERSITY OF MAINZ				DRAWING NO.	
				SCALE	SHEET 3 OF 5

HIGH SPPED OPTICAL LINKS



CLK_MGT1_P<12..1>
CLK_MGT1_N<12..1>
CLK_MGT2_P<6..1>
CLK_MGT2_N<6..1>

NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA		UNIVERSITY OF MAINZ	
CHECKED	U. SCHAEFER			
CHECKED	S. RAVE			
DRAWN	BAUSS	07.08.2015		
BLOCK TITLE			U1_MGT_REAL_TIME	
UNIVERSITY OF MAINZ			SIZE	DRAWING NO.
			SCALE	

BANK

119
120
121
122
123
124

TOPO_L2

REV.

SHEET 1 OF 7

HIGH SPPEED OPTICAL LINKS
HIGH SPEED IPBUS

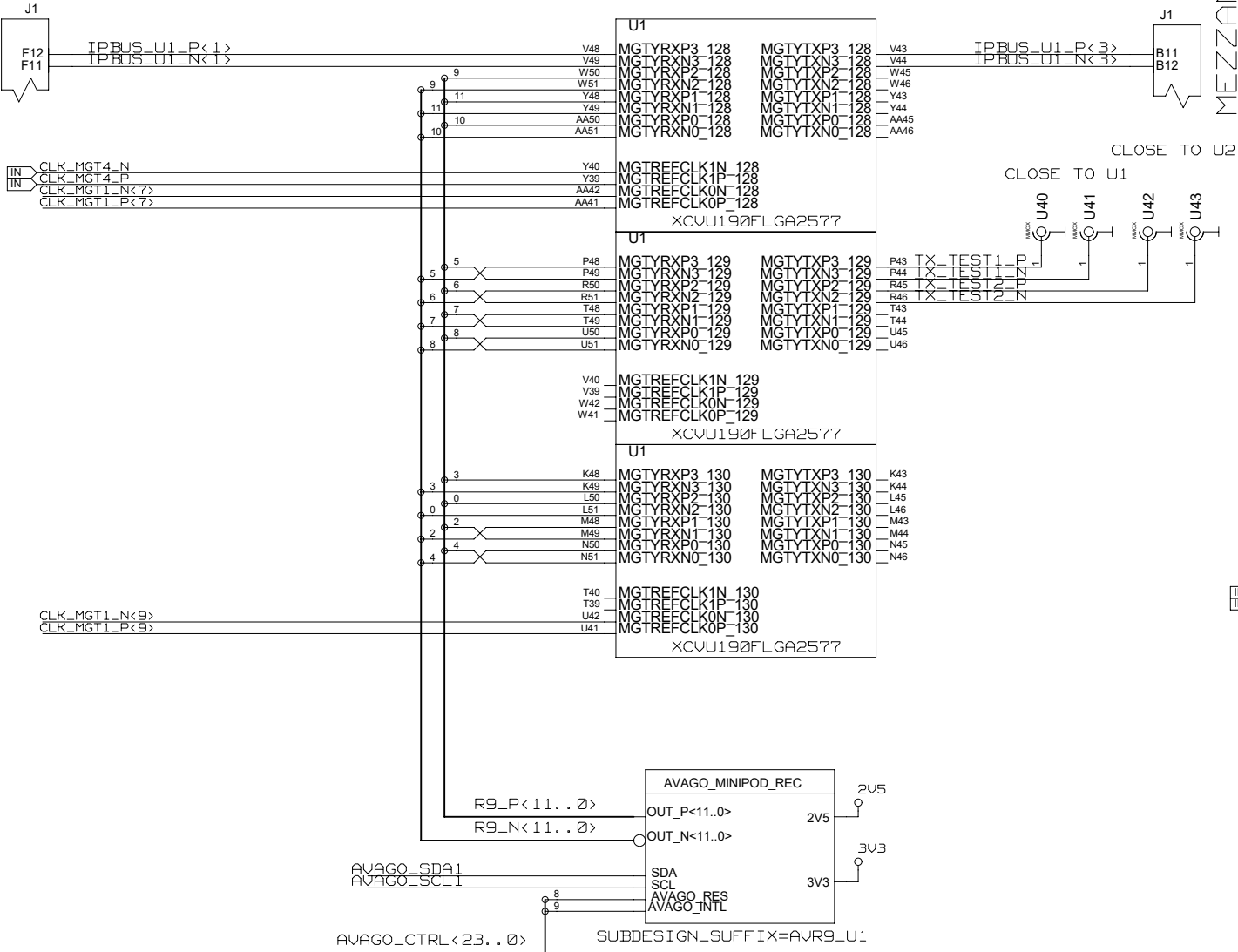
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

MEZZANINE

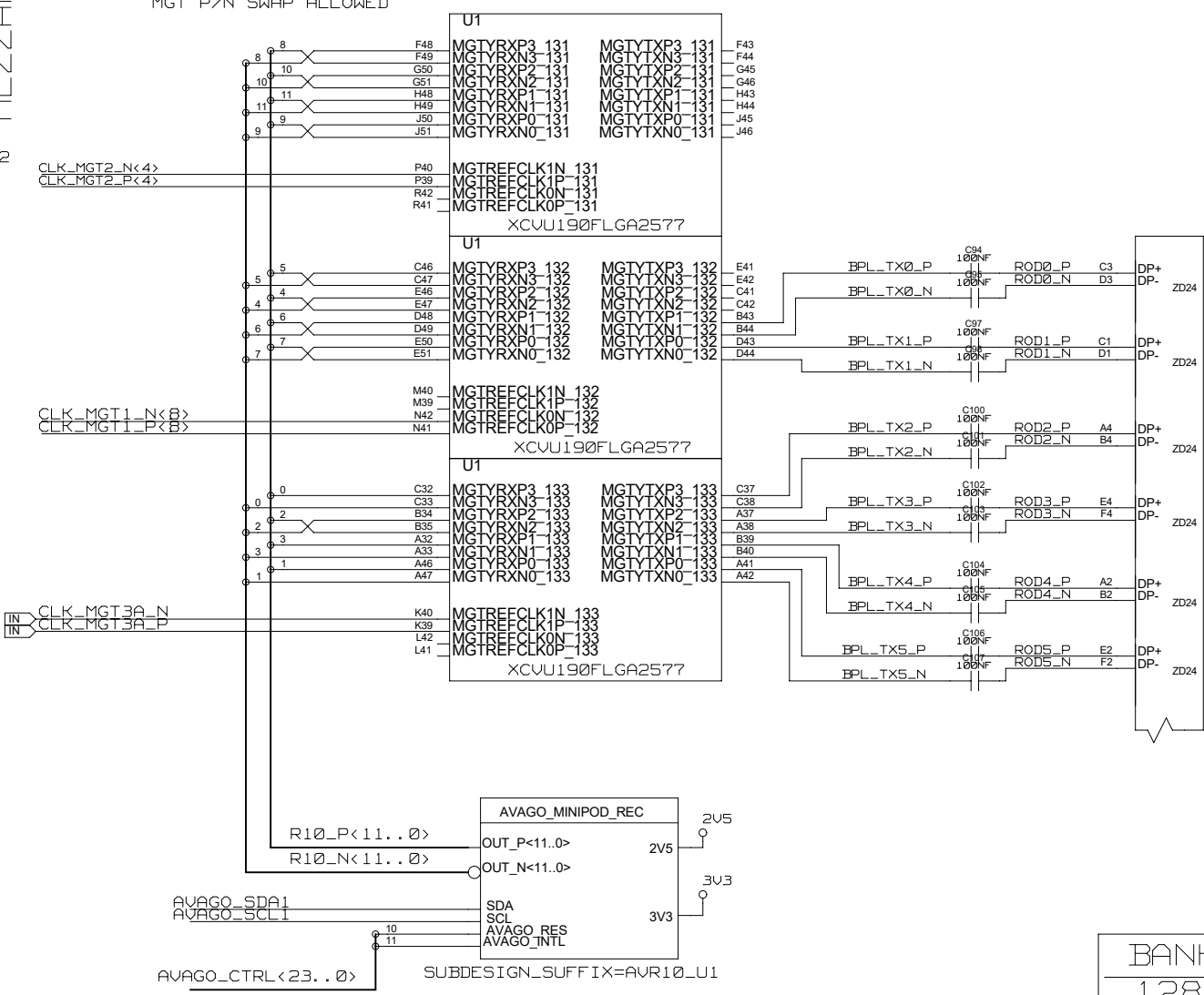
MEZZANINE

MGT P/N SWAP ALLOWED

MGT P/N SWAP ALLOWED



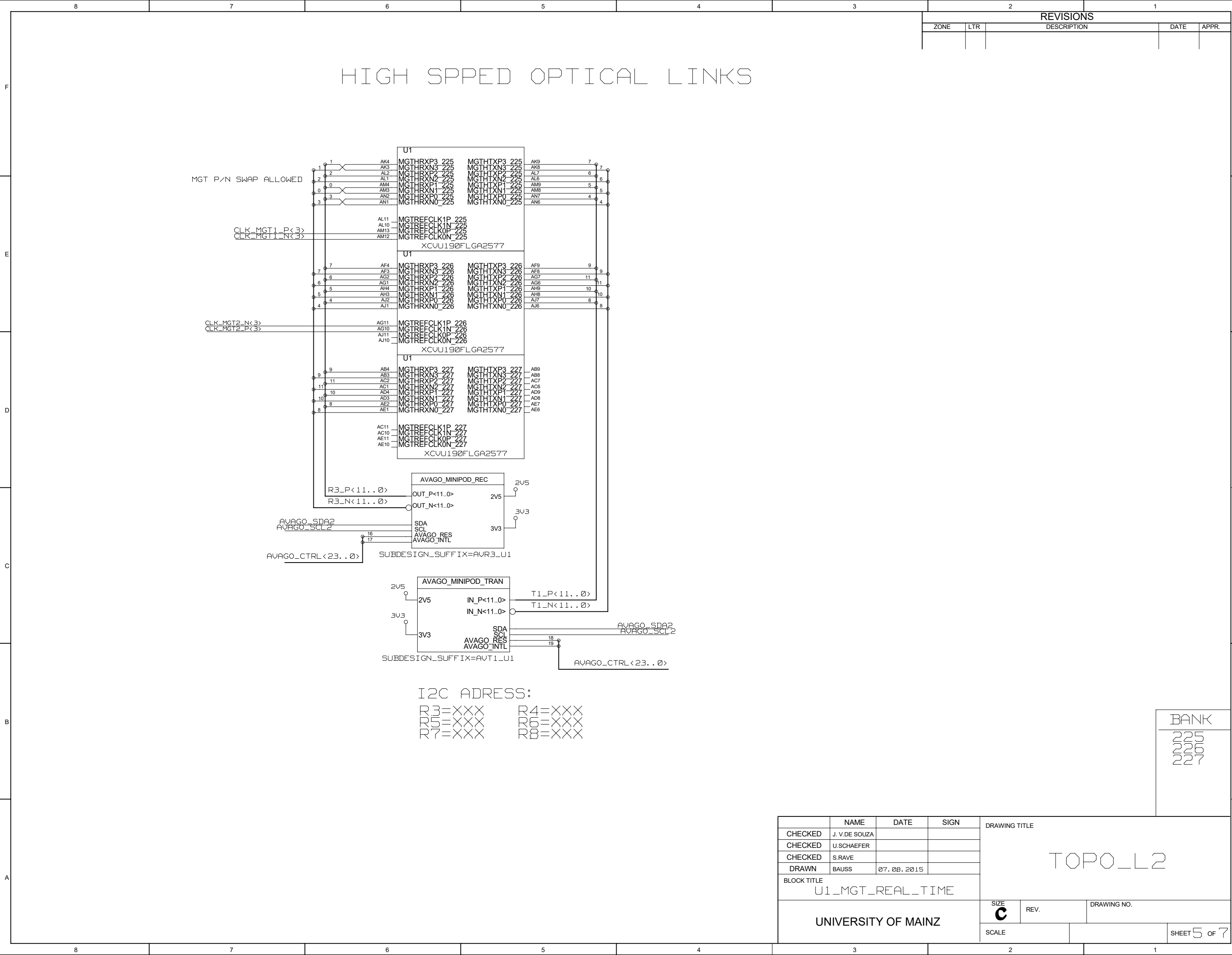
I2C ADDRESS:
R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX



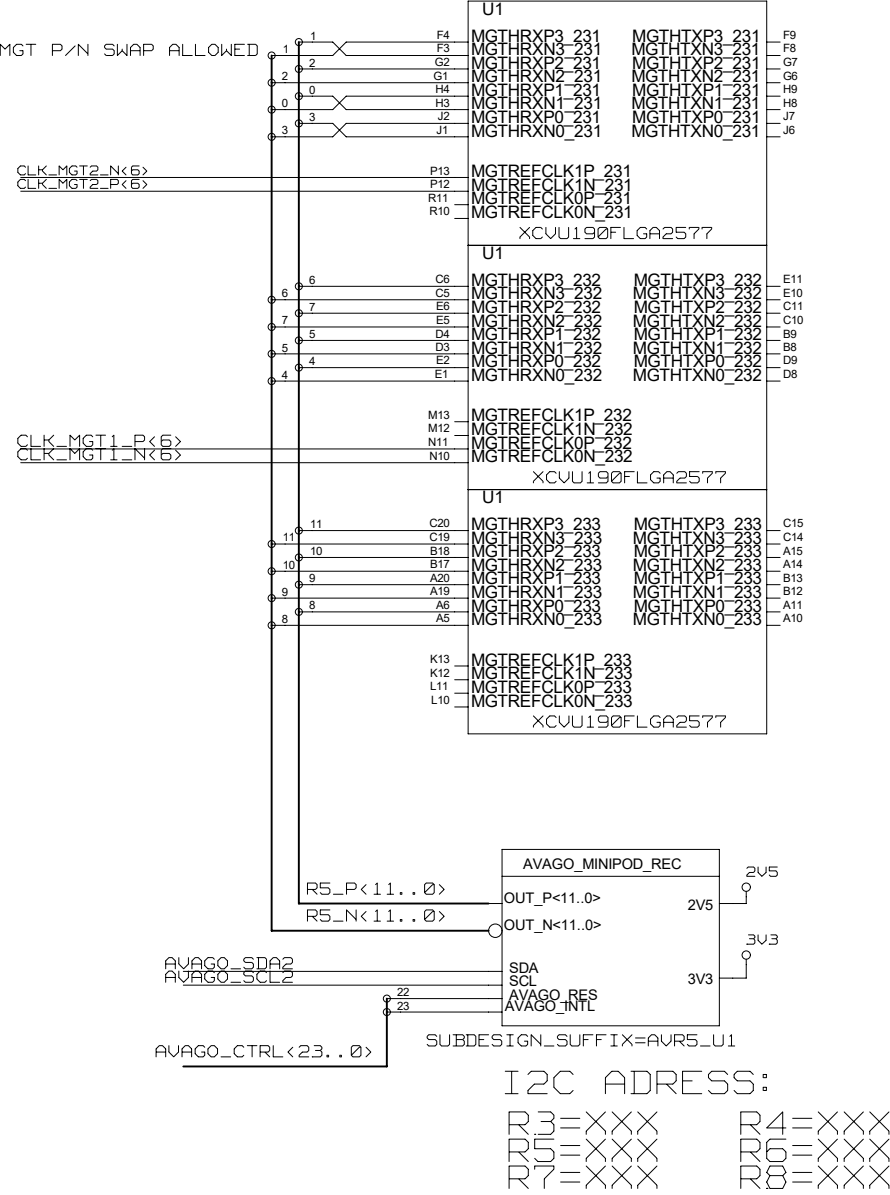
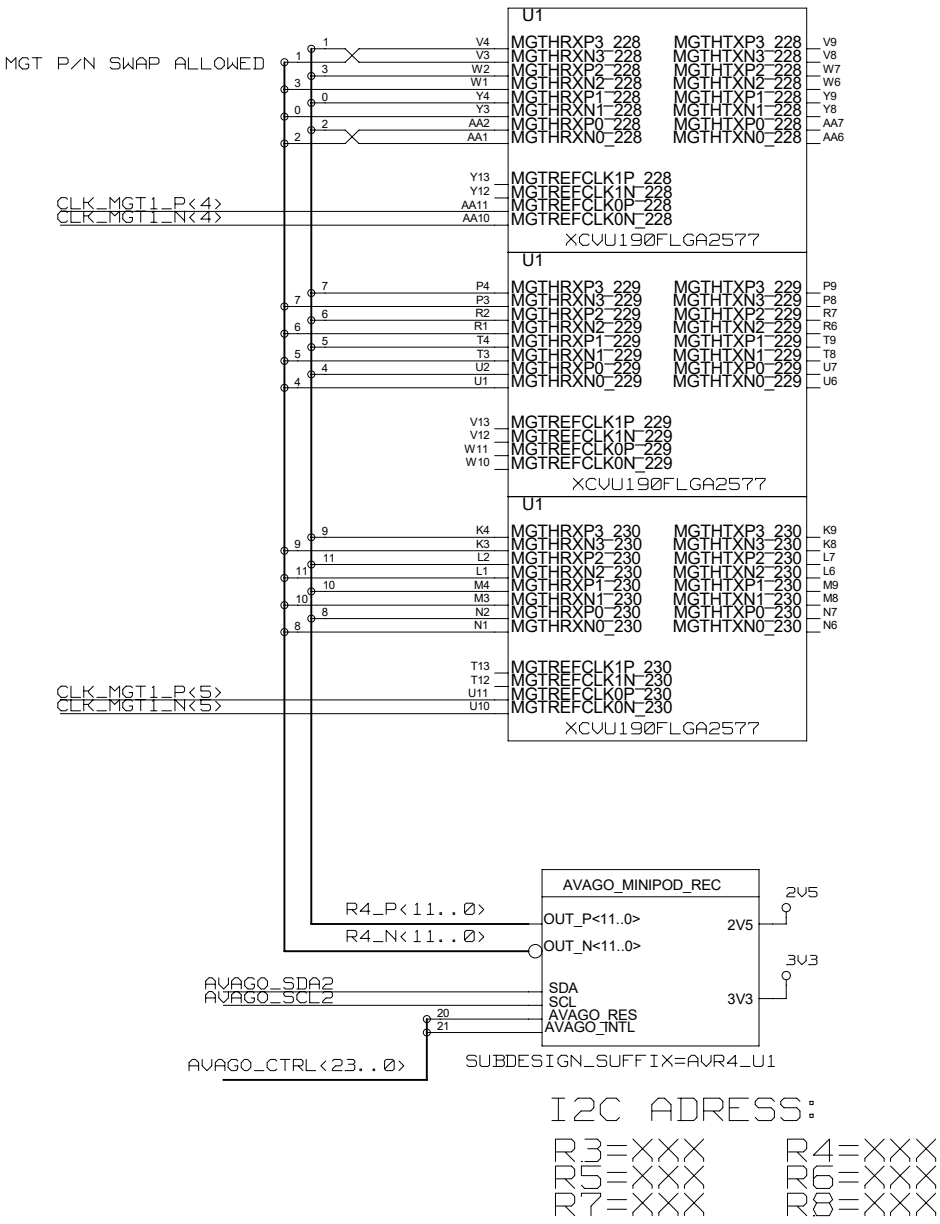
I2C ADDRESS:
R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

BANK
128
128
128
128
128
128
128
128

NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA		TOPO_L2	
CHECKED	U. SCHAEFER			
CHECKED	S. RAVE			
DRAWN	BAUSS	07.08.2015		
BLOCK TITLE			U1_MGT_REAL_TIME	
UNIVERSITY OF MAINZ			SIZE C	DRAWING NO.
SCALE			REV.	SHEET 3 OF 7



HIGH SPPED OPTICAL LINKS

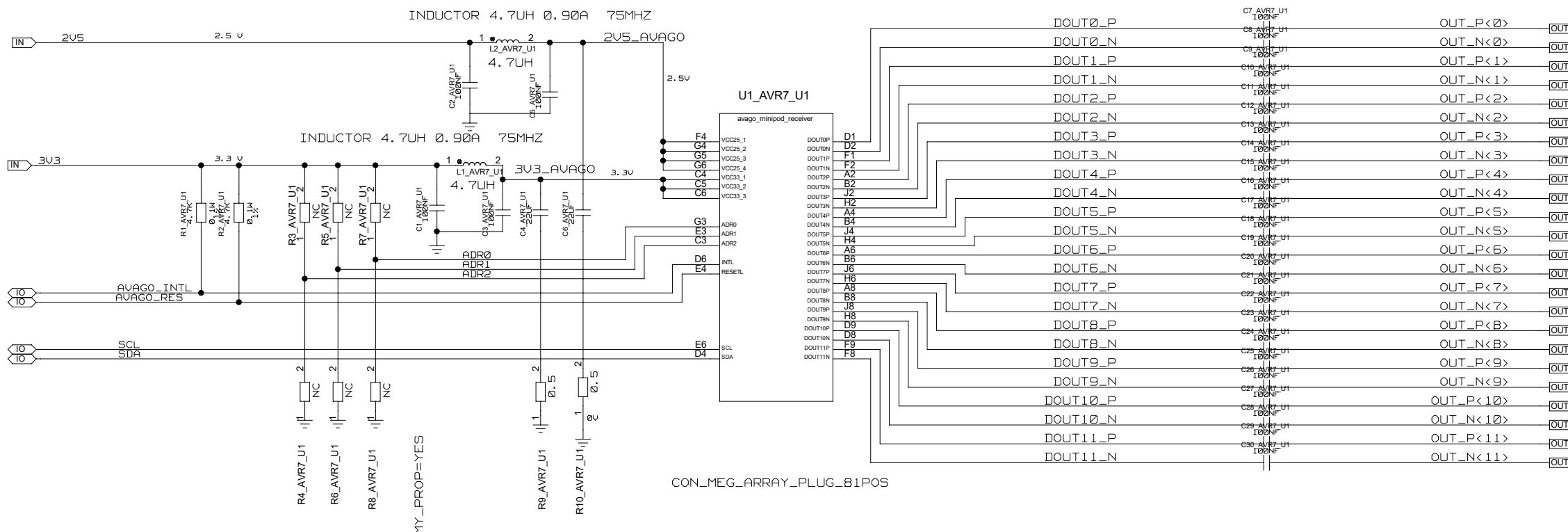


BANK

228
228
228
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228
228
228
228

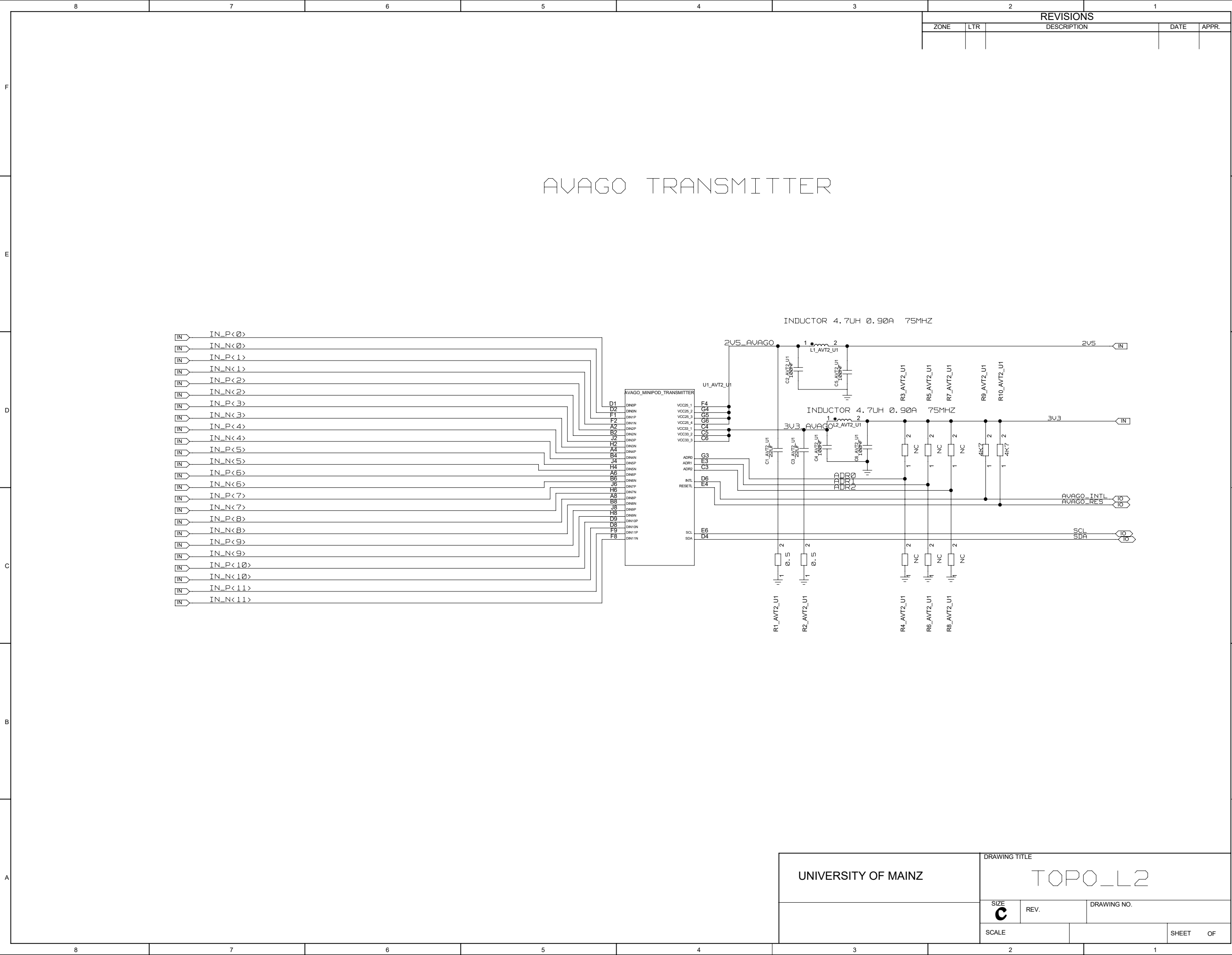
NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V.DE SOUZA		TOPO_L2	
CHECKED	U.SCHAEFER			
CHECKED	S.RAVE			
DRAWN	BAUSS	07.08.2015		
BLOCK TITLE			DRAWING NO.	
U1_MGT_REAL_TIME				
UNIVERSITY OF MAINZ			SIZE	REV.
			C	
SCALE			SHEET 6 OF 7	

AVAGO RECEIVER



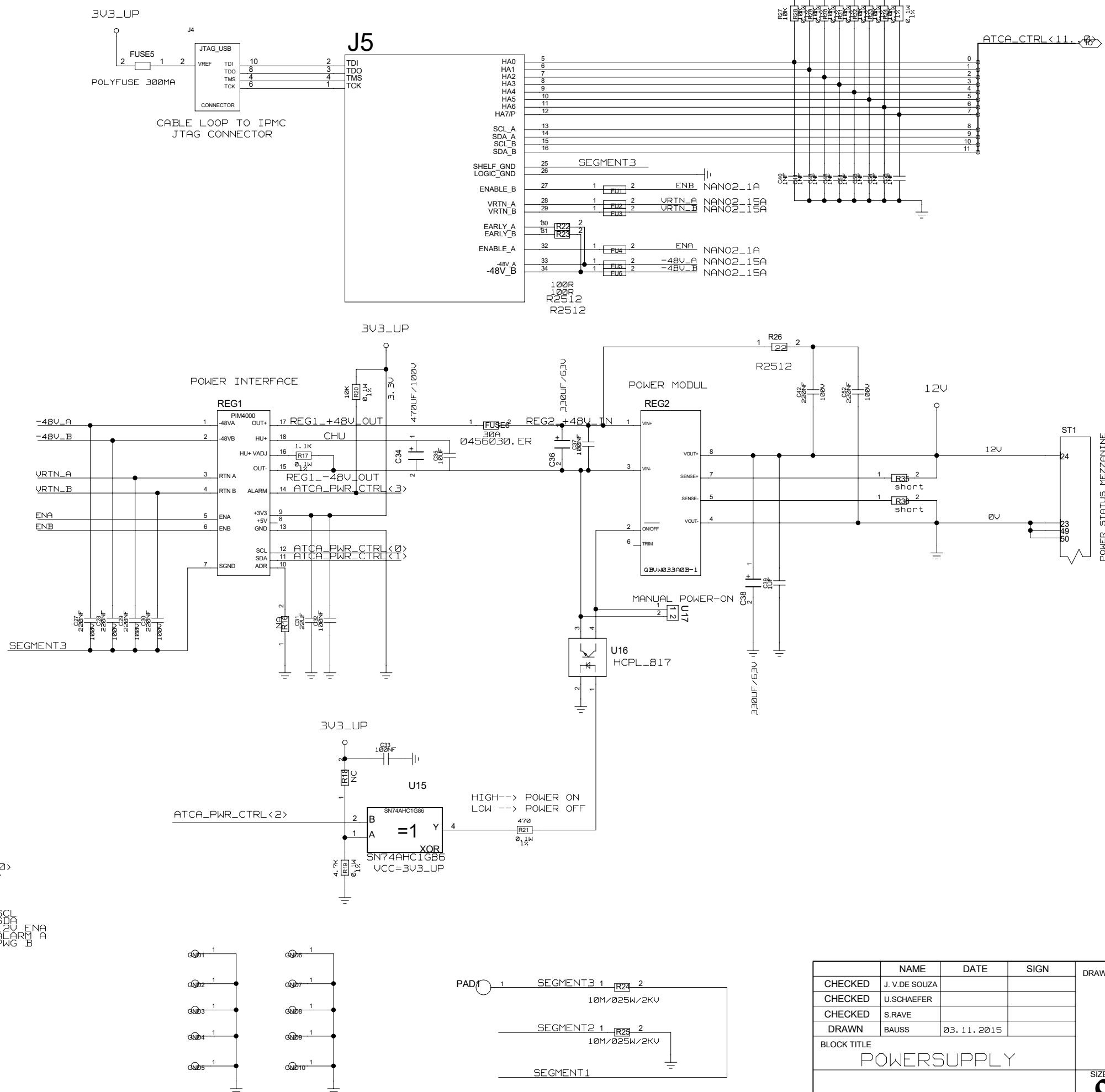
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

UNIVERSITY OF MAINZ		DRAWING TITLE		
		TOPO_L2		
		SIZE C	REV.	DRAWING NO.
SCALE		SHEET		OF



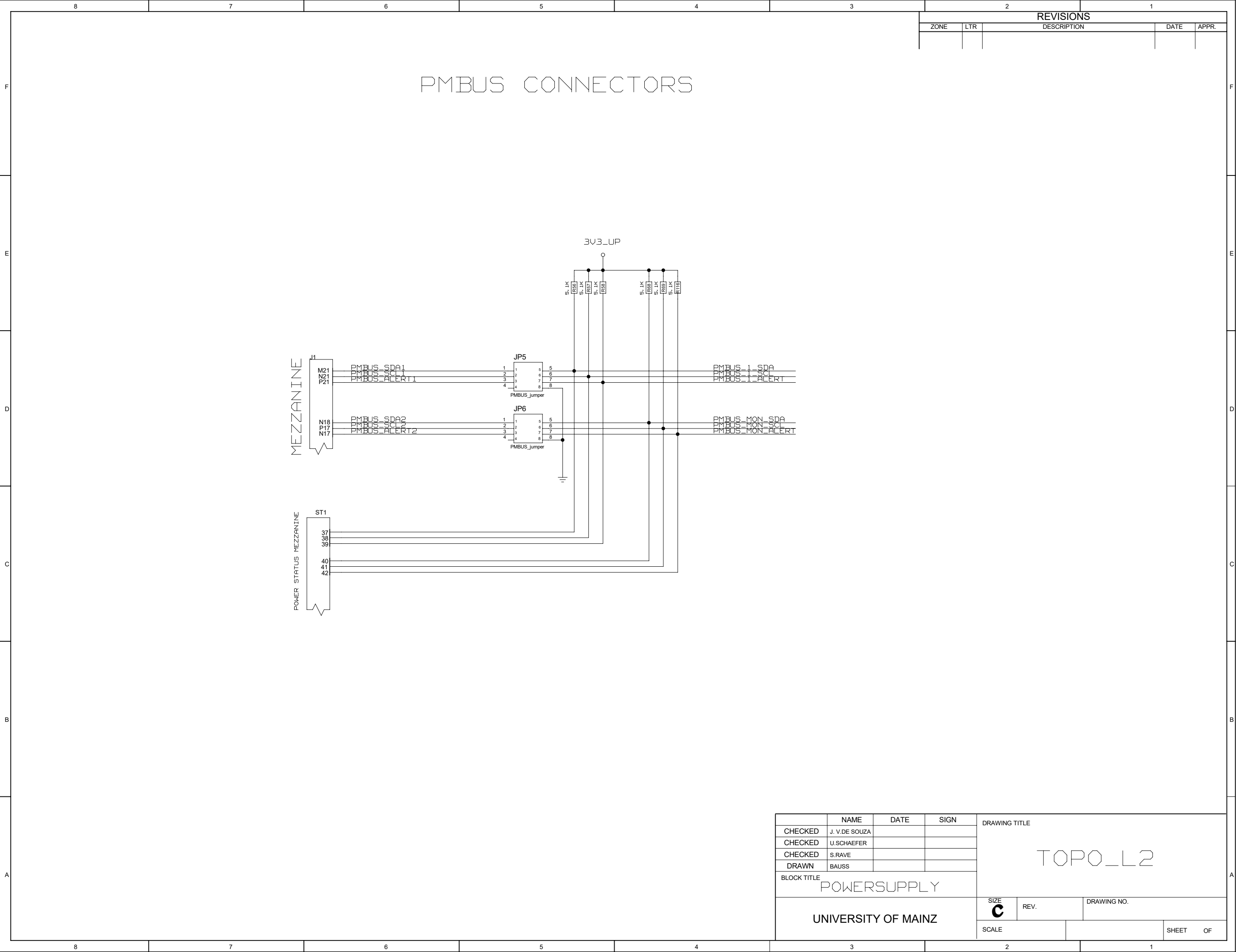
ATCA POWER IN & CTRL

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE



ATCA_PWR_CTRL<0> = SCL
ATCA_PWR_CTRL<1> = SDA
ATCA_PWR_CTRL<2> = TMS
ATCA_PWR_CTRL<3> = TCK
ATCA_PWR_CTRL<4> = ENB

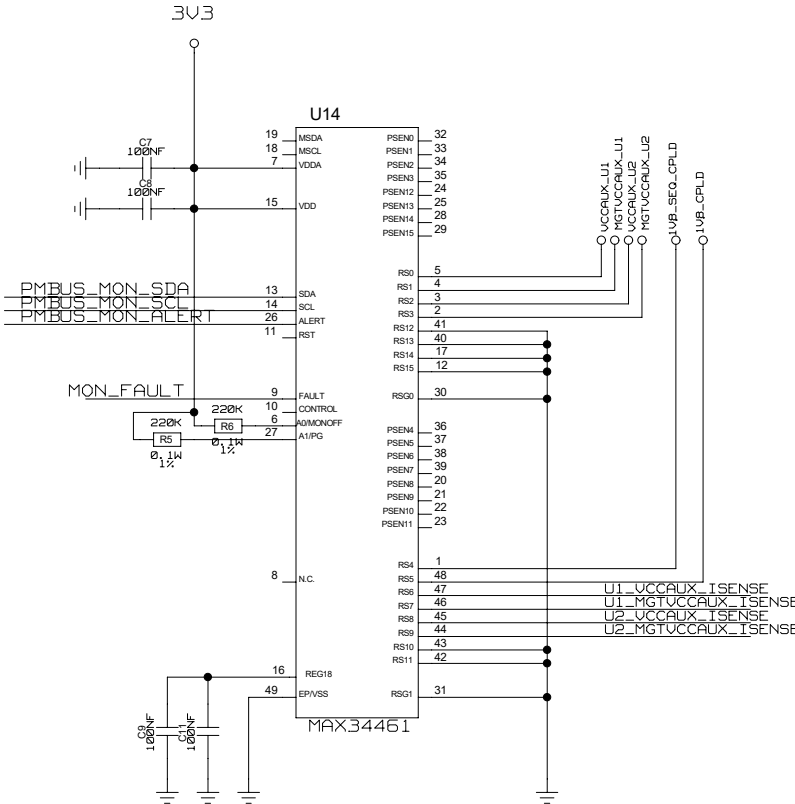
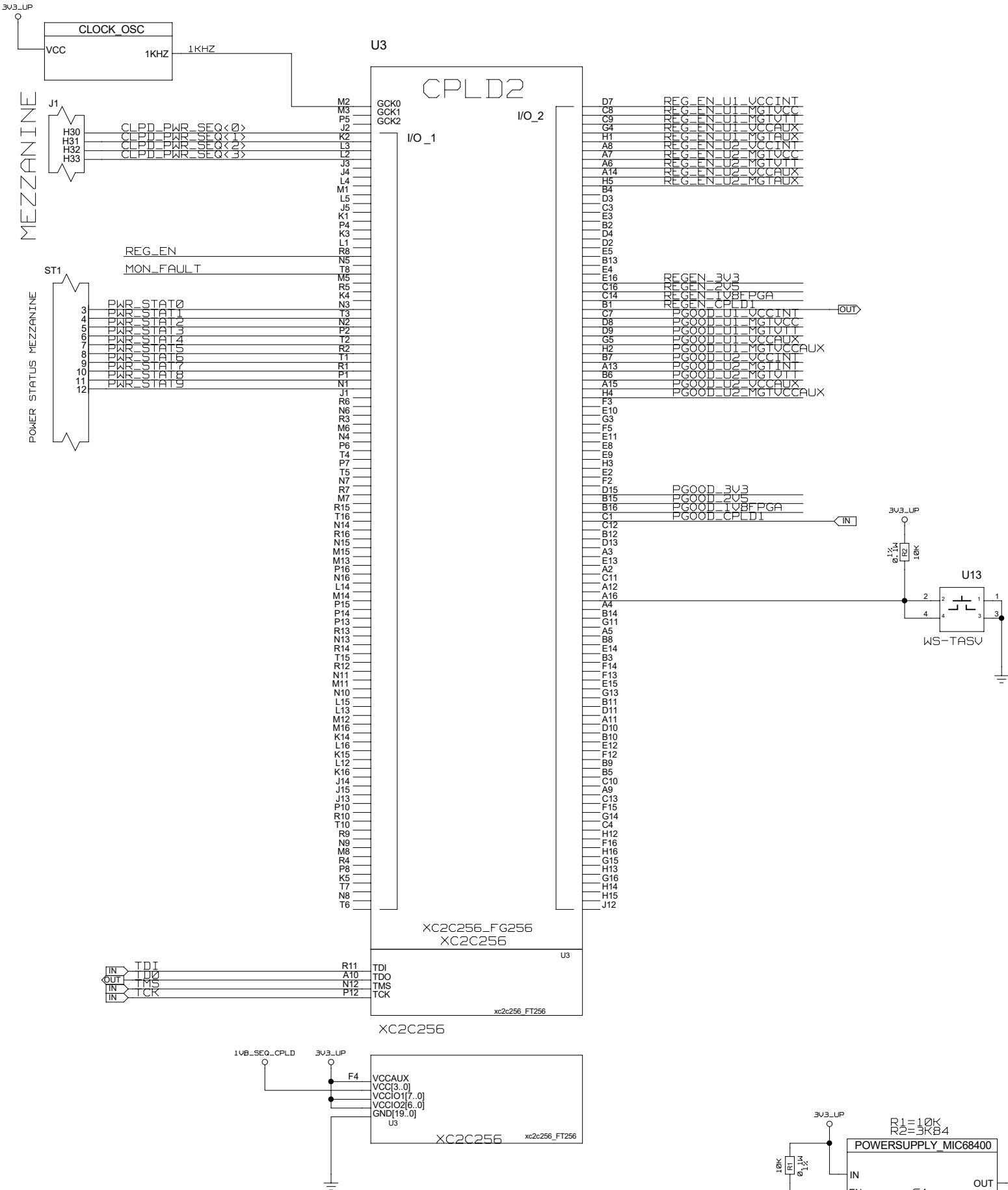
NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA		TOPO_L2	
CHECKED	U. SCHAEFER			
CHECKED	S. RAVE			
DRAWN	BAUSS	03.11.2015		
BLOCK TITLE			POWERSUPPLY	
UNIVERSITY OF MAINZ			SIZE C	DRAWING NO.
			SCALE	SHEET OF



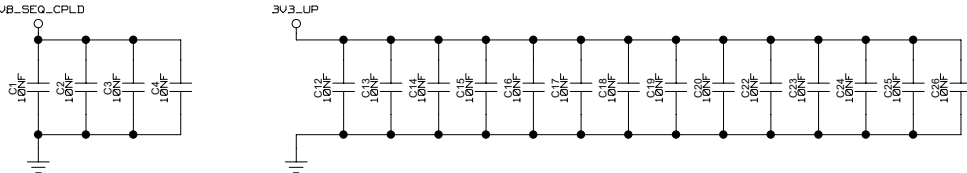
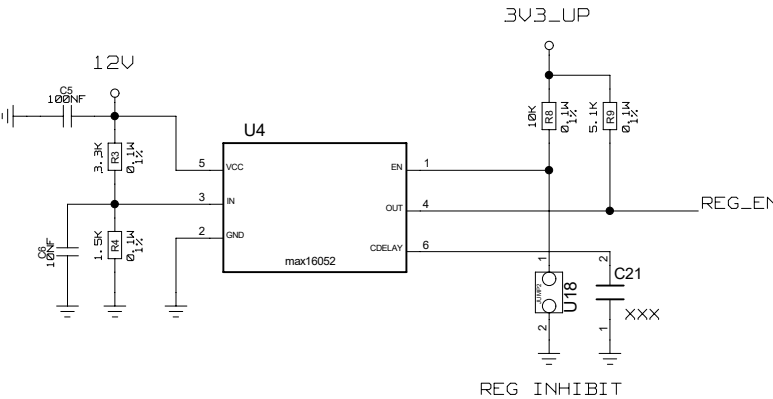
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE

POWERSEQUENCING

VOLTAGE MONITORING

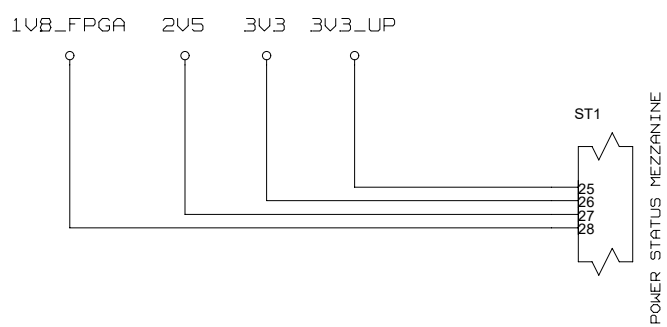
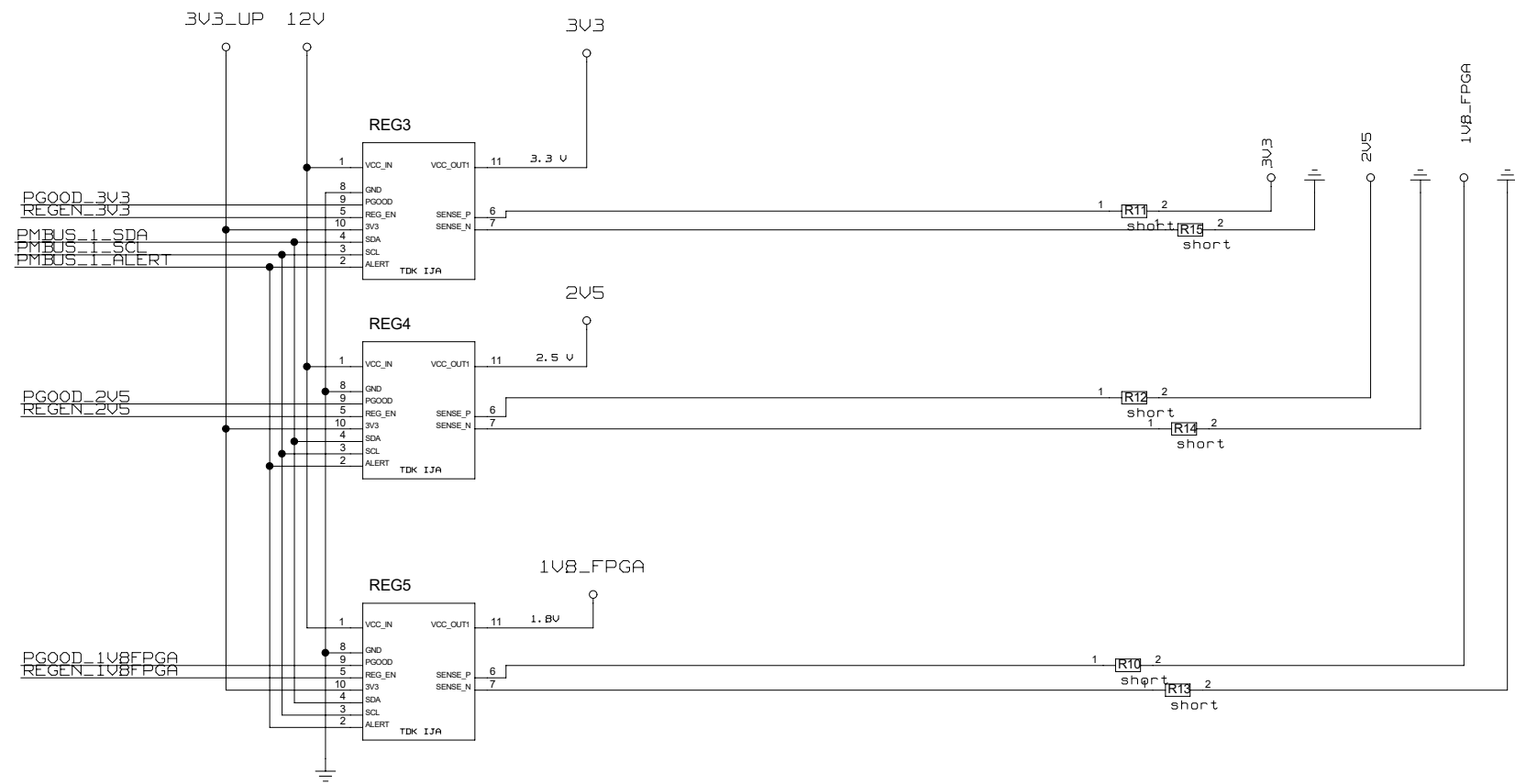


12V SUPERVISORY



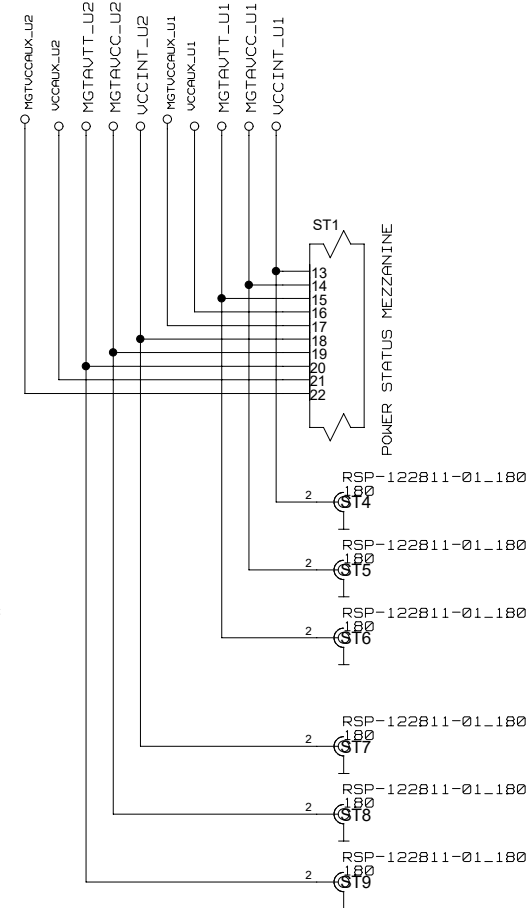
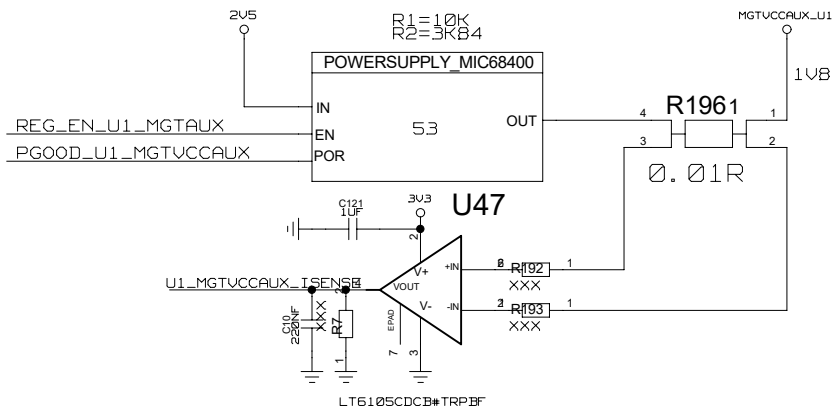
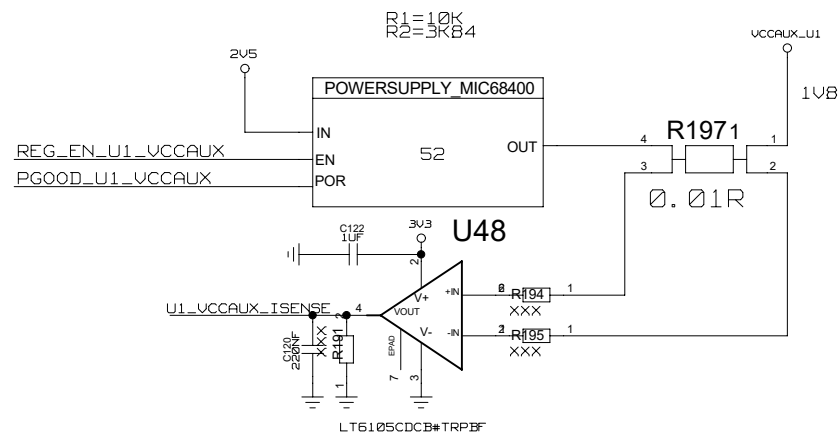
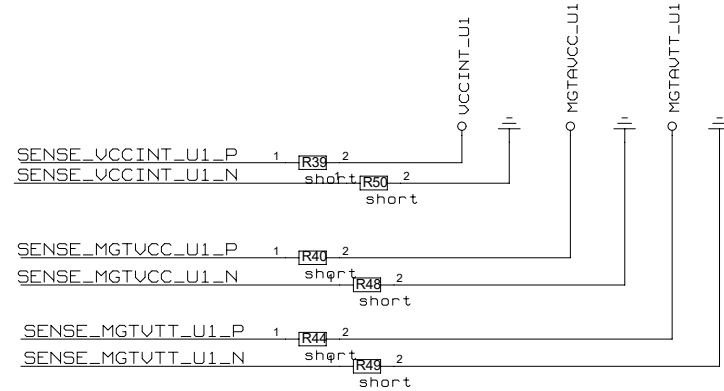
NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA		TOPO_L2 POWERSUPPLY UNIVERSITY OF MAINZ	
CHECKED	U. SCHAEFER			
CHECKED	S. RAVE			
DRAWN	BAUSS			
BLOCK TITLE			SIZE	DRAWING NO.
			REV.	
			SCALE	SHEET OF

BOARDLEVEL 1V8, 2V5, 3V3



REVISIONS				1	
ZONE	LTR	DESCRIPTION	DATE	APPR.	

CHECKED	J. V. DE SOUZA	DATE	SIGN	DRAWING TITLE TOPOLL2	
CHECKED	U. SCHAEFER				
CHECKED	S. RAVE				
DRAWN	BAUSS				
BLOCK TITLE POWERSUPPLY				SIZE C	REV.
UNIVERSITY OF MAINZ				DRAWING NO.	
				SCALE	SHEET OF



The schematic diagram illustrates the internal structure of the TDK_FPGA_PWR module. It features a central component labeled 'TDK_FPGA_PWR' with various pins connected to external signals and power sources.

Power Connections:

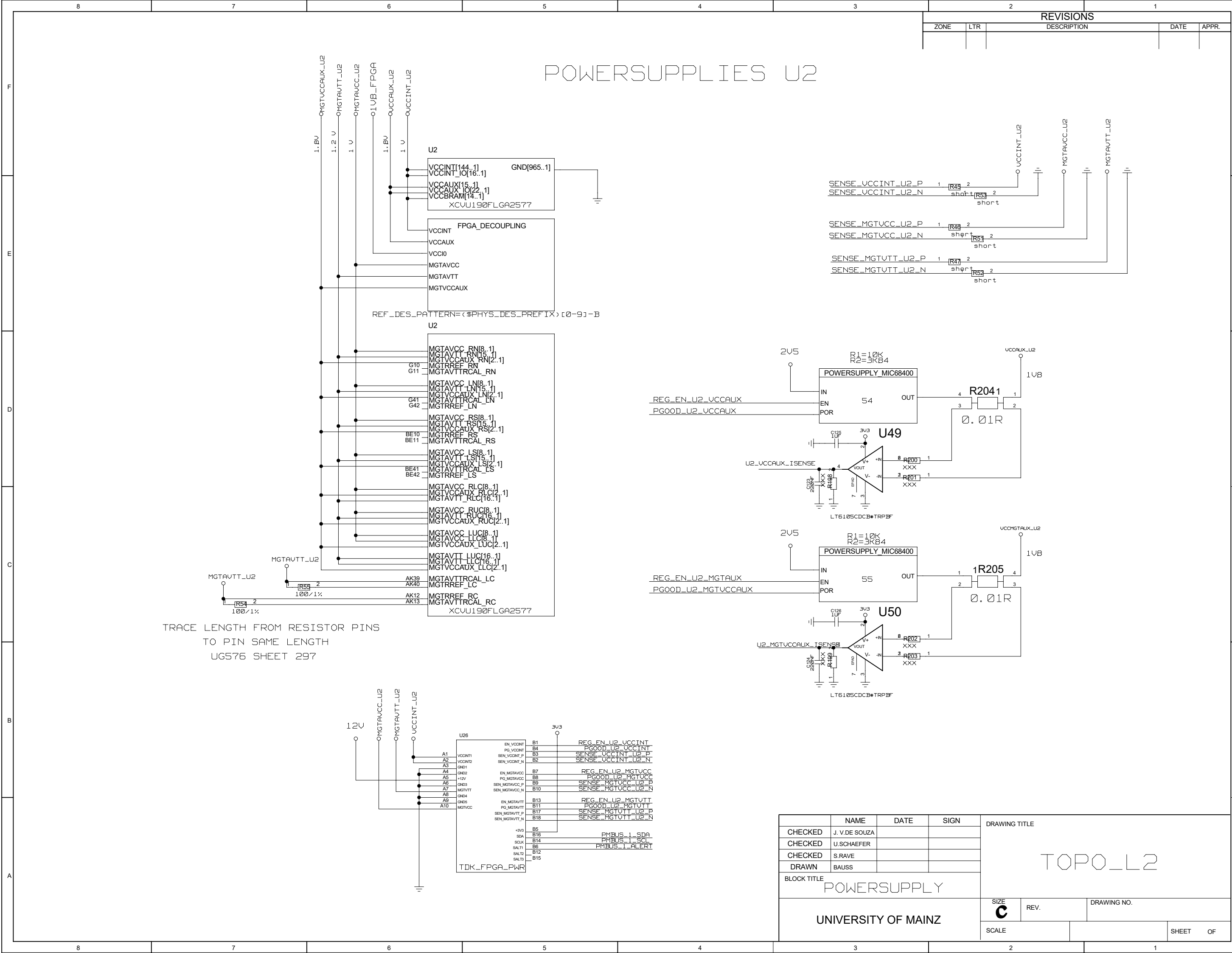
- 12V:** Connected to the **OMGTAVCC_U1** and **OMGTAU1T_U1** pins.
- 3V3:** Connected to the **UCCINT_U1** pin.

Internal Components and Connections:

- U19:** A multi-pin component with connections to:
 - VCCINT1, VCCINT2, GND1, GND2, GND3, GND4, GND5, GND6:** These pins are connected to the **OMGTAVCC_U1** and **OMGTAU1T_U1** lines.
 - EN_VCCINT, PG_VCCINT, SEN_VCCINT_P, SEN_VCCINT_N:** These pins are connected to the **UCCINT_U1** line.
 - EN_MGTAVCC, PG_MGTAVCC, SEN_MGTAVCC_P, SEN_MGTAVCC_N:** These pins are connected to the **OMGTAVCC_U1** line.
 - EN_MGTAU1T, PG_MGTAU1T, SEN_MGTAU1T_P, SEN_MGTAU1T_N:** These pins are connected to the **OMGTAU1T_U1** line.
- B1-B18:** A series of pins connected to the **TDK_FPGA_PWR** module, which then connects to external signals:
 - B1:** REG_EN_U1_VCCINT
 - B4:** PGOOD_U1_VCCINT
 - B3:** SENSE_VCCINT_U1_P
 - B2:** SENSE_VCCINT_U1_N
 - B7:** REG_EN_U1_MGTUCC
 - B8:** PGOOD_U1_MGTUCC
 - B9:** SENSE_MGTUCC_U1_P
 - B10:** SENSE_MGTUCC_U1_N
 - B13:** REG_EN_U1_MGTVTT
 - B11:** PGOOD_U1_MGTVTT
 - B17:** SENSE_MGTVTT_U1_P
 - B18:** SENSE_MGTVTT_U1_N
- B5-B15:** A series of pins connected to the **TDK_FPGA_PWR** module, which then connects to external signals:
 - B5:** PMBUS_1_SDA
 - B14:** PMBUS_1_SCL
 - B6:** PMBUS_1_ALERT
 - B12:** SALT2
 - B15:** SALT3

The diagram shows a complex interconnection of power, control, and data lines, with the TDK_FPGA_PWR module acting as the central hub for these signals.

	NAME	DATE	SIGN	DRAWING TITLE TOPO_L2		
CHECKED	J. V.DE SOUZA					
CHECKED	U.SCHAEFER					
CHECKED	S.RAVE					
DRAWN	BAUSS					
BLOCK TITLE POWERSUPPLY						
UNIVERSITY OF MAINZ				SIZE C	REV.	DRAWING NO.
				SCALE		



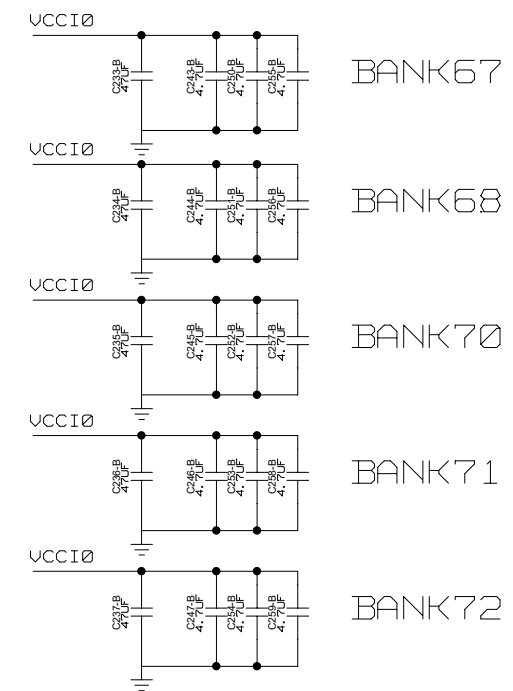
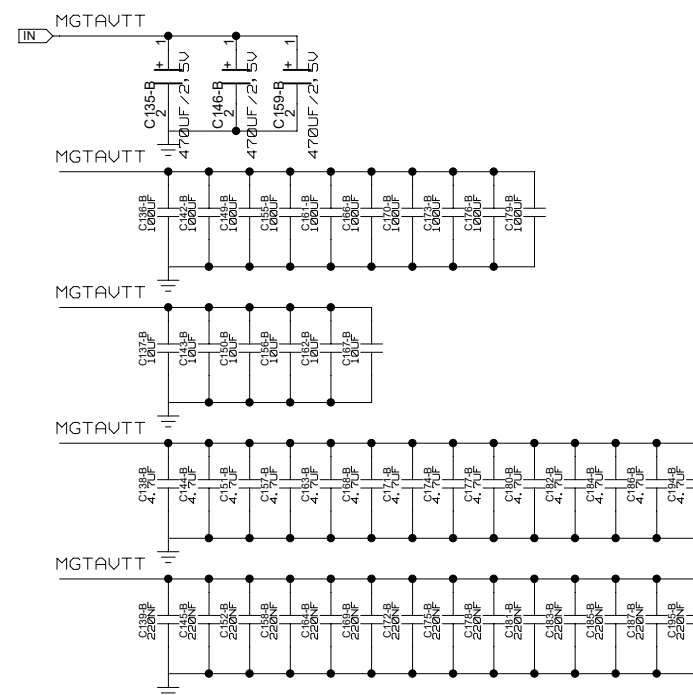


Figure 10 illustrates the recommended capacitor values for the MGTUCCAUX input under four different conditions:

- Configuration 1 (Top):** MGTUCCAUX input with an IN signal. Capacitor values are: 22.1 pF, 4.7 pF, 2.2 pF, 4.7 pF, 2.2 pF, 4.7 pF.
- Configuration 2:** MGTUCCAUX input. Capacitor values are: 100 pF, 100 pF, 100 pF, 100 pF, 100 pF, 100 pF.
- Configuration 3:** MGTUCCAUX input. Capacitor values are: 22.1 pF, 100 pF, 2.2 pF, 22.1 pF, 100 pF, 2.2 pF.
- Configuration 4 (Bottom):** MGTUCCAUX input. Capacitor values are: 22.1 pF, 4.7 pF, 2.2 pF, 4.7 pF, 2.2 pF, 4.7 pF, 2.2 pF, 4.7 pF, 2.2 pF, 4.7 pF.

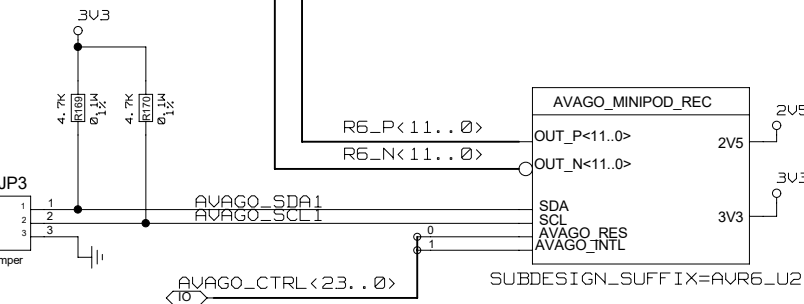
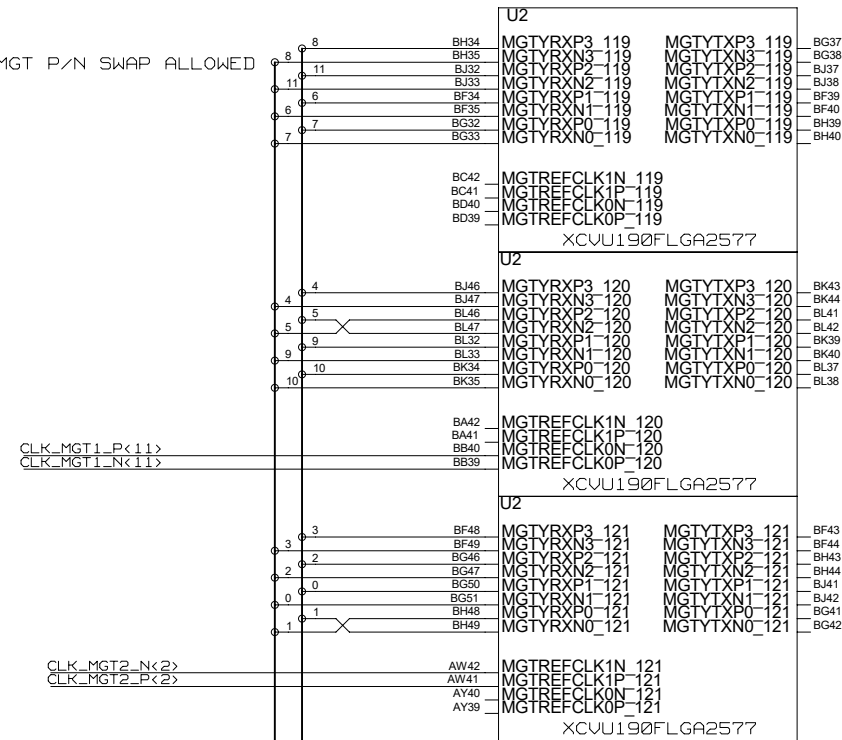


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CHECKED	U.SCHAEFER								
CHECKED	S.RAVE								
DRAWN	BAUSS								
BLOCK TITLE FPGA_DECOUPLING									
UNIVERSITY OF MAINZ				SIZE C	REV.	DRAWING NO.			
				SCALE				SHEET	OF

HIGH SPPED OPTICAL LINKS

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

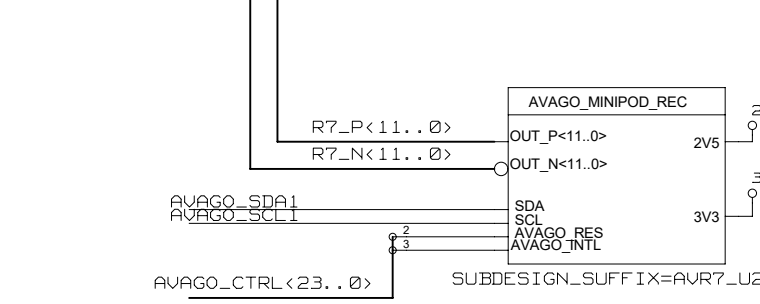
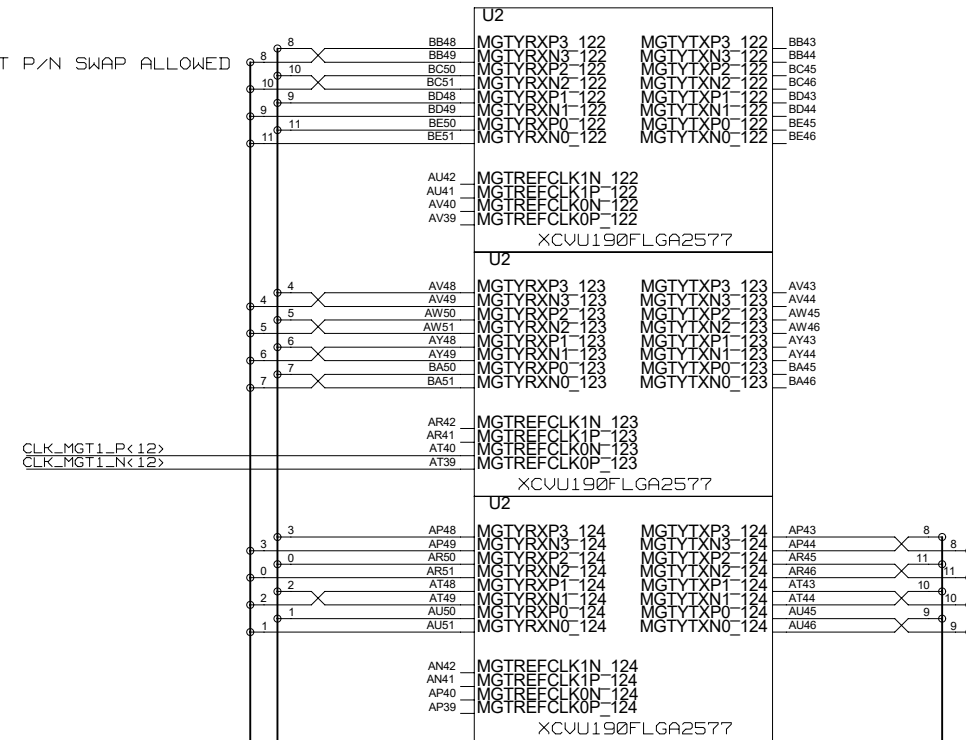
MGT P/N SWAP ALLOWED



I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

MGT P/N SWAP ALLOWED



I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

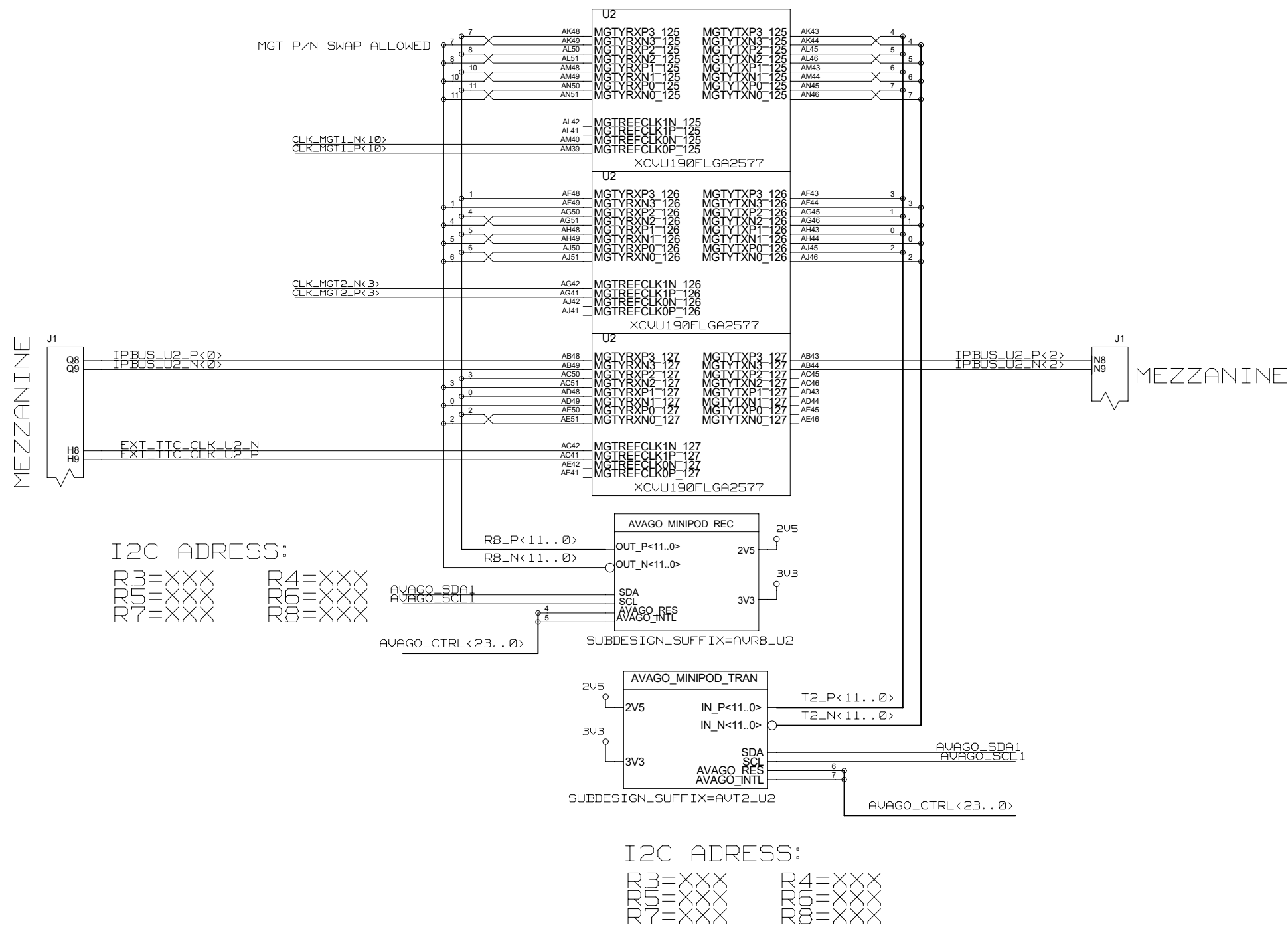
BANK
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NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA		TOPO_L2	
CHECKED	U. SCHAEFER			
CHECKED	S. RAVE			
DRAWN	BAUSS	07.08.2015		
BLOCK TITLE			SIZE	DRAWING NO.
U2_MGT_REAL_TIME			C	
UNIVERSITY OF MAINZ			SCALE	SHEET 5 OF 7

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HIGH SPED OPTICAL LINKS

HIGH SPEED IPBUS

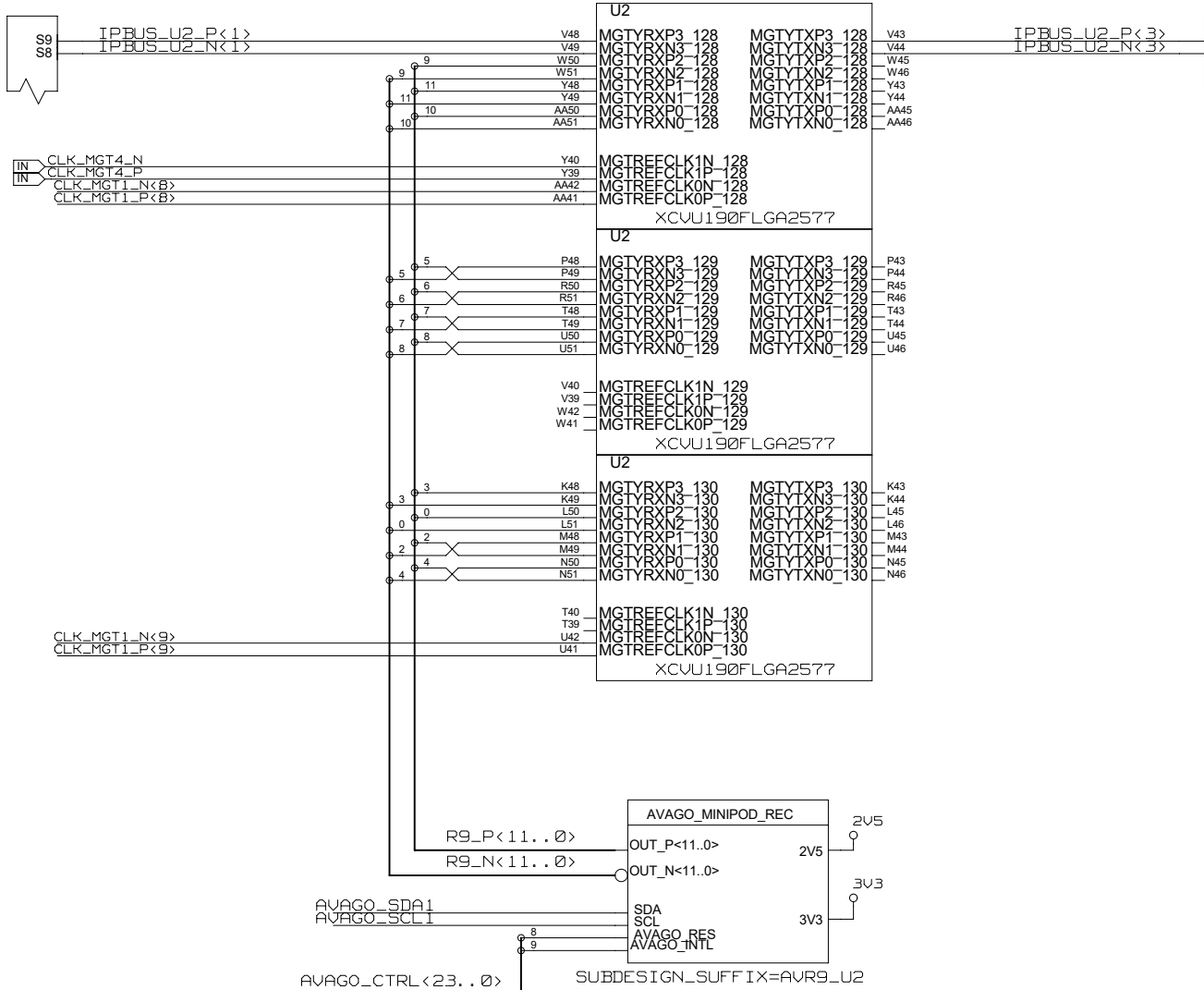


CHECKED	NAME	DATE	SIGN	DRAWING TITLE	
CHECKED	J. V. DE SOUZA			TOPO_L2	
CHECKED	U. SCHAEFER				
CHECKED	S. RAVE				
DRAWN	BAUSS	07.08.2015			
BLOCK TITLE				U2_MGT_REAL_TIME	
UNIVERSITY OF MAINZ				SIZE C	REV.
				SCALE	DRAWING NO.
				SHEET 6 OF 7	

HIGH SPEED OPTICAL LINKS

MEZZANINE

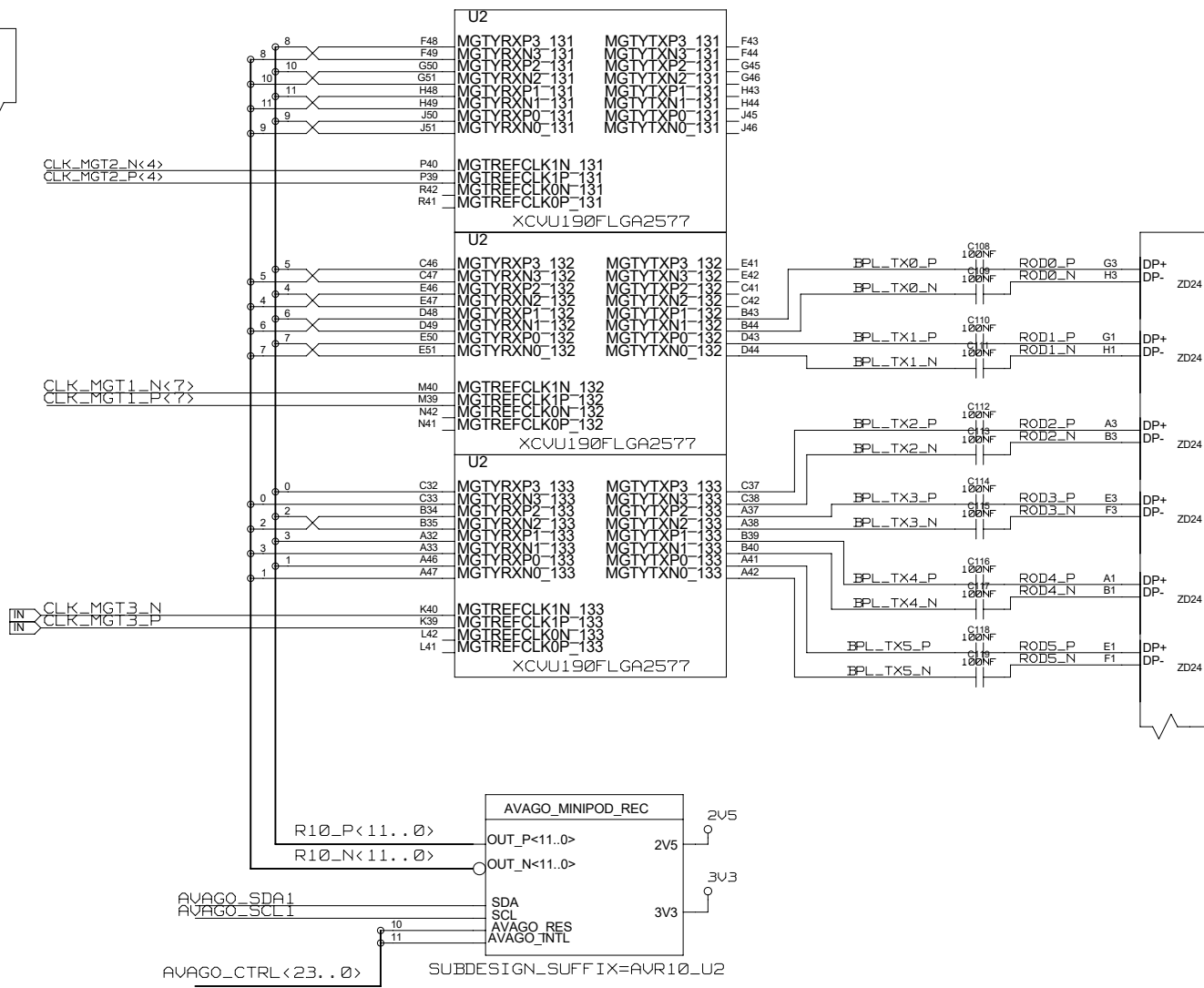
MGT P/N SWAP ALLOWED



I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

MGT P/N SWAP ALLOWED



I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

BANK
128
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134
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CHECKED	NAME	DATE	SIGN	DRAWING TITLE		
CHECKED	J. V. DE SOUZA			TOPO_L2		
CHECKED	U. SCHAEFER					
CHECKED	S. RAVE					
DRAWN	BAUSS	07.08.2015				
BLOCK TITLE				U2_MGT_REAL_TIME		
UNIVERSITY OF MAINZ				SIZE	REV.	DRAWING NO.
				C		
				SCALE		SHEET 7 OF 7

HIGH SPPEED OPTICAL LINKS

MGT P/N SWAP ALLOWED

MGT P/N SWAP ALLOWED

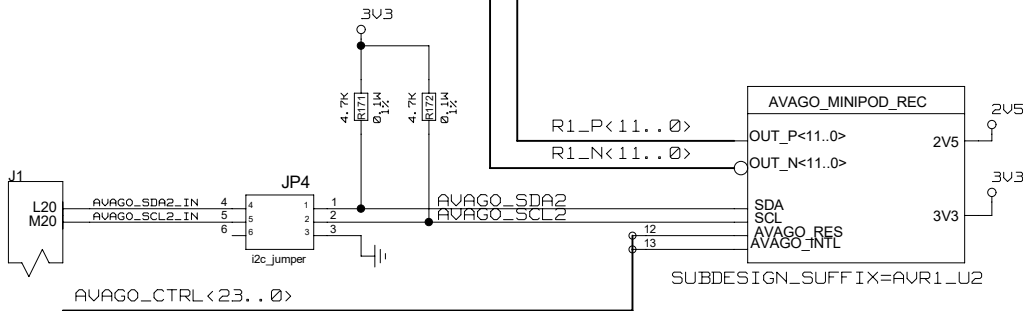
CLK_MGT1_P<1>
CLK_MGT1_N<1>

CLK_MGT1_P<4>
CLK_MGT1_N<4>

CLK_MGT2_N<1>
CLK_MGT2_P<1>

T1_N<11..0>

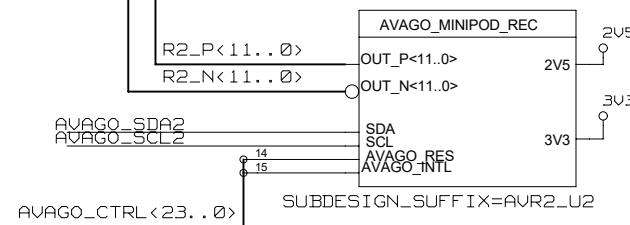
T1_P<11..0>



AVAGO_CTRL<11..0>
AVAGO_CTRL 0, 2, 4, 6, 8, 10 = AVAGO_RES_XX
AVAGO_CTRL 1, 3, 5, 7, 9, 11 = AVAGO_INTL_XX

I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX



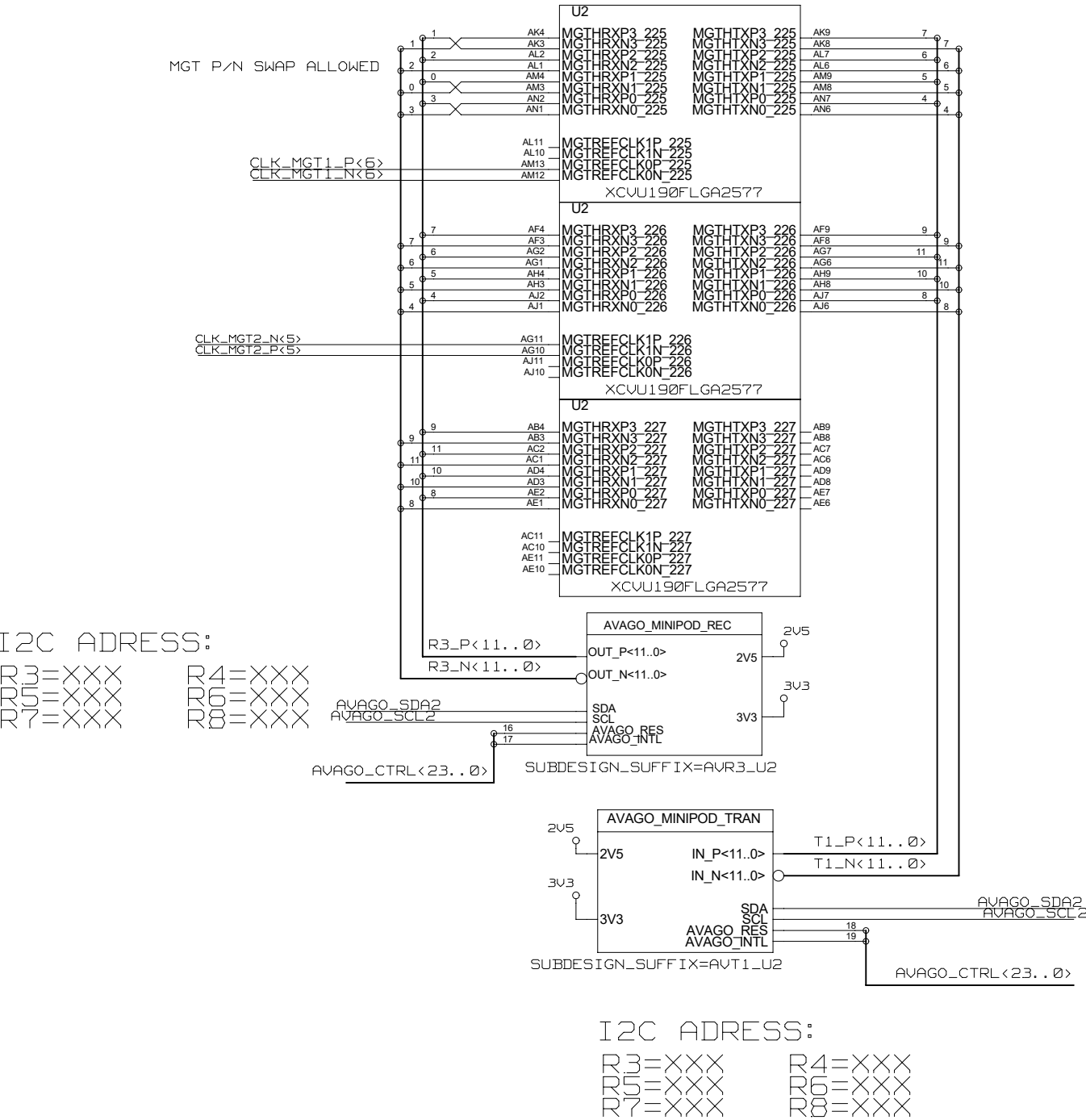
I2C ADDRESS:

R3=XXX R4=XXX
R5=XXX R6=XXX
R7=XXX R8=XXX

BANK
219
220
221
222
223
224

	NAME	DATE	SIGN	DRAWING TITLE TOPO_L2			
CHECKED	J. V.DE SOUZA						
CHECKED	U.SCHAEFER						
CHECKED	S.RAVE						
DRAWN	BAUSS	07. 08. 2015					
BLOCK TITLE U2_MGT_REAL_TIME				UNIVERSITY OF MAINZ			
		SIZE C	REV.		DRAWING NO.		
		SCALE				SHEET 2 OF 7	

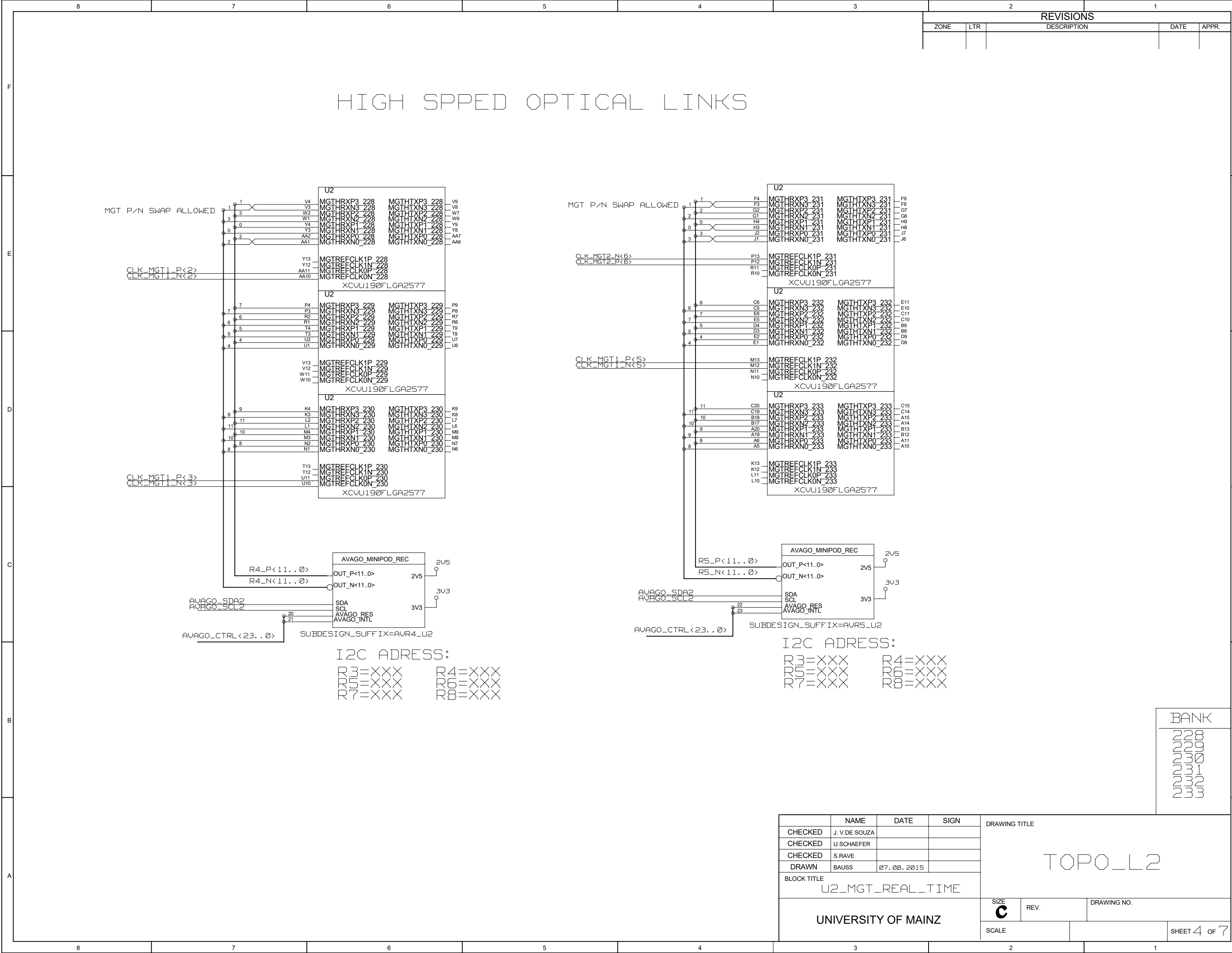
HIGH SPPED OPTICAL LINKS

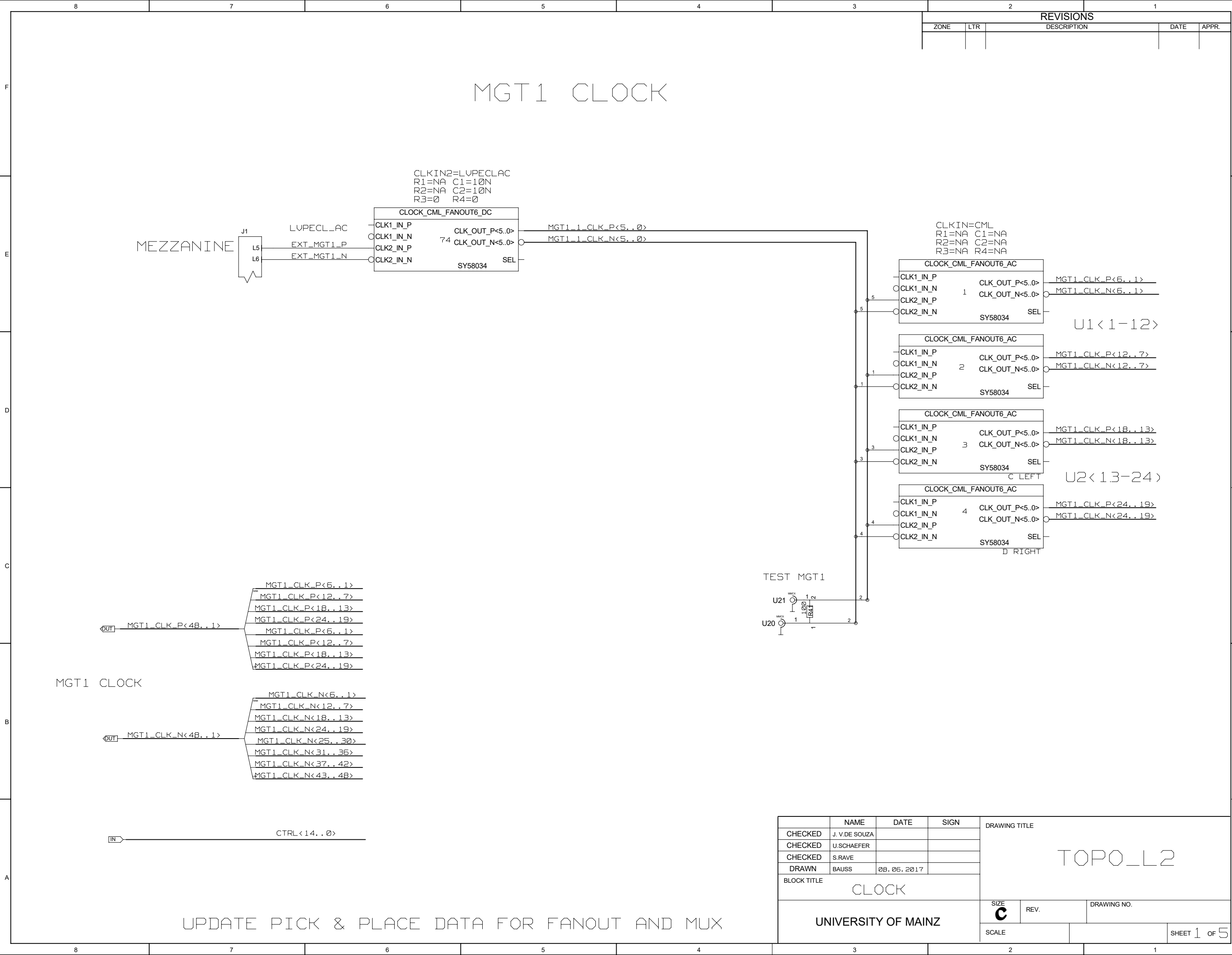


REVISIONS					DATE		APPR.	
ZONE	LTR	DESCRIPTION						

DRAWING TITLE				DRAWING NO.	
TOPOLL2					
BLOCK TITLE					
U3_MGT_REAL_TIME					
UNIVERSITY OF MAINZ					
SIZE		REV.			
C					
SCALE					
				SHEET 3 OF 7	

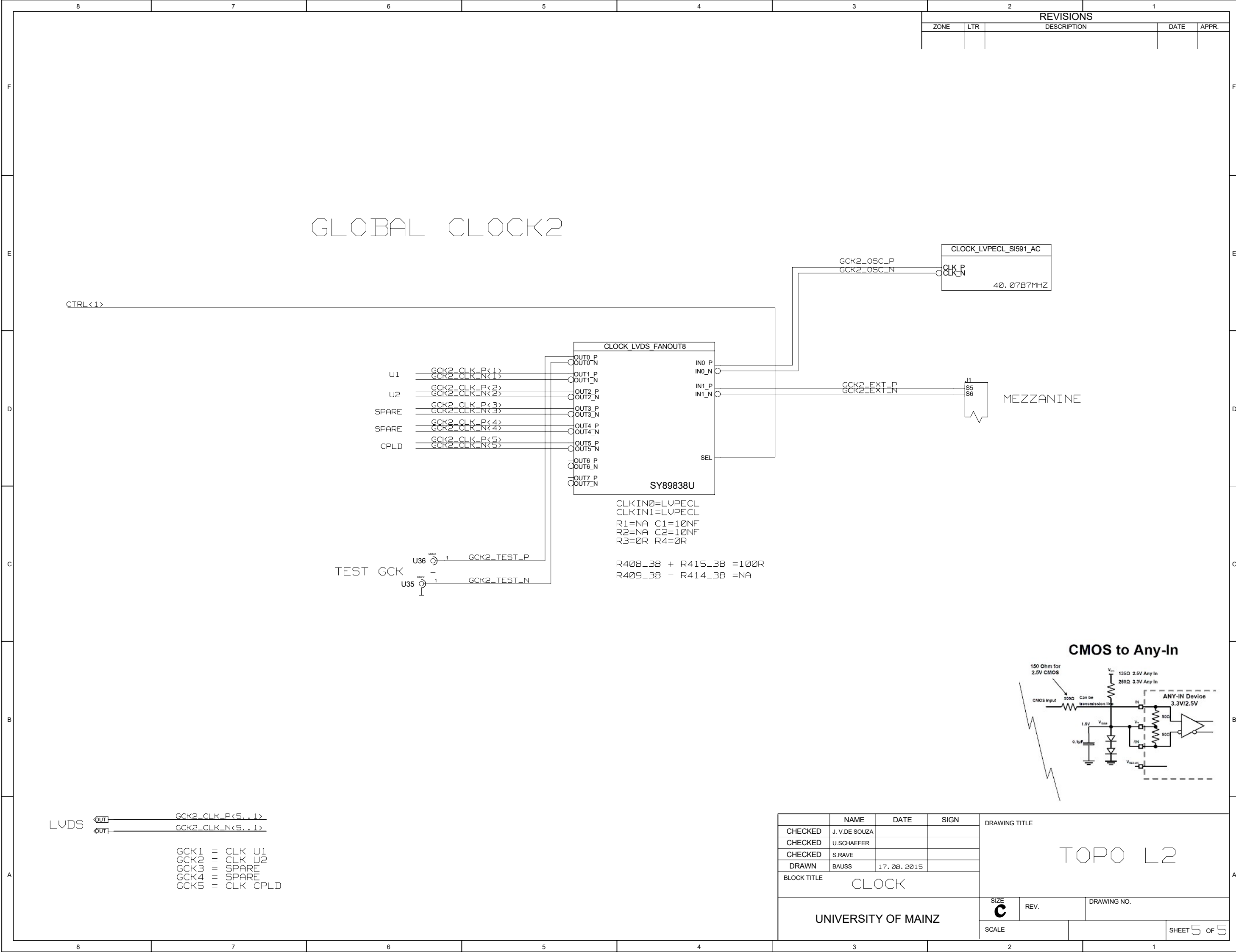
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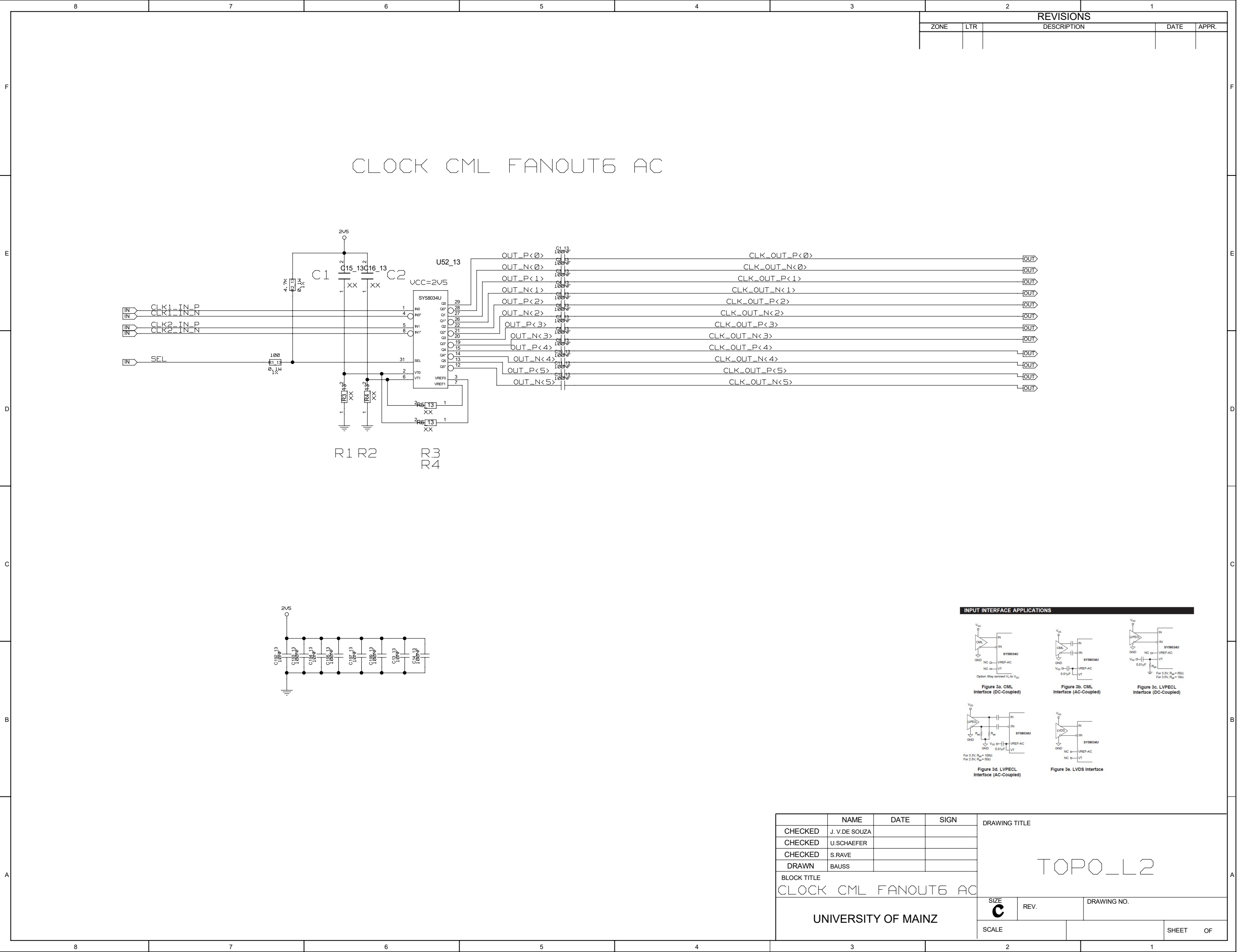




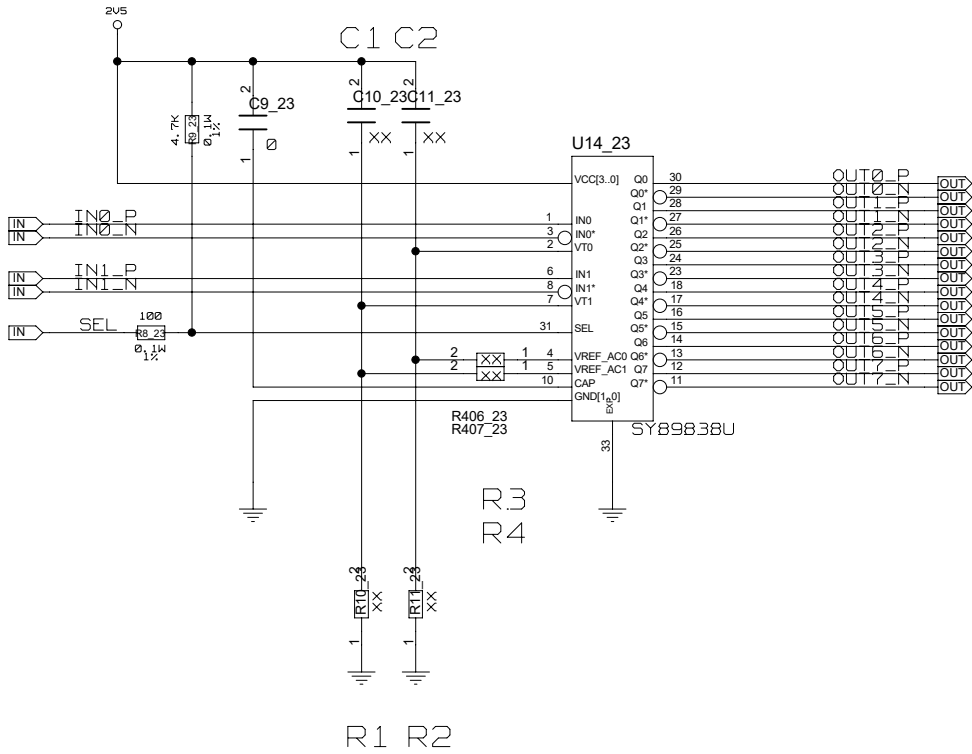
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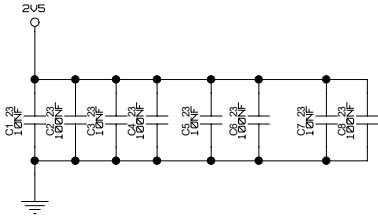




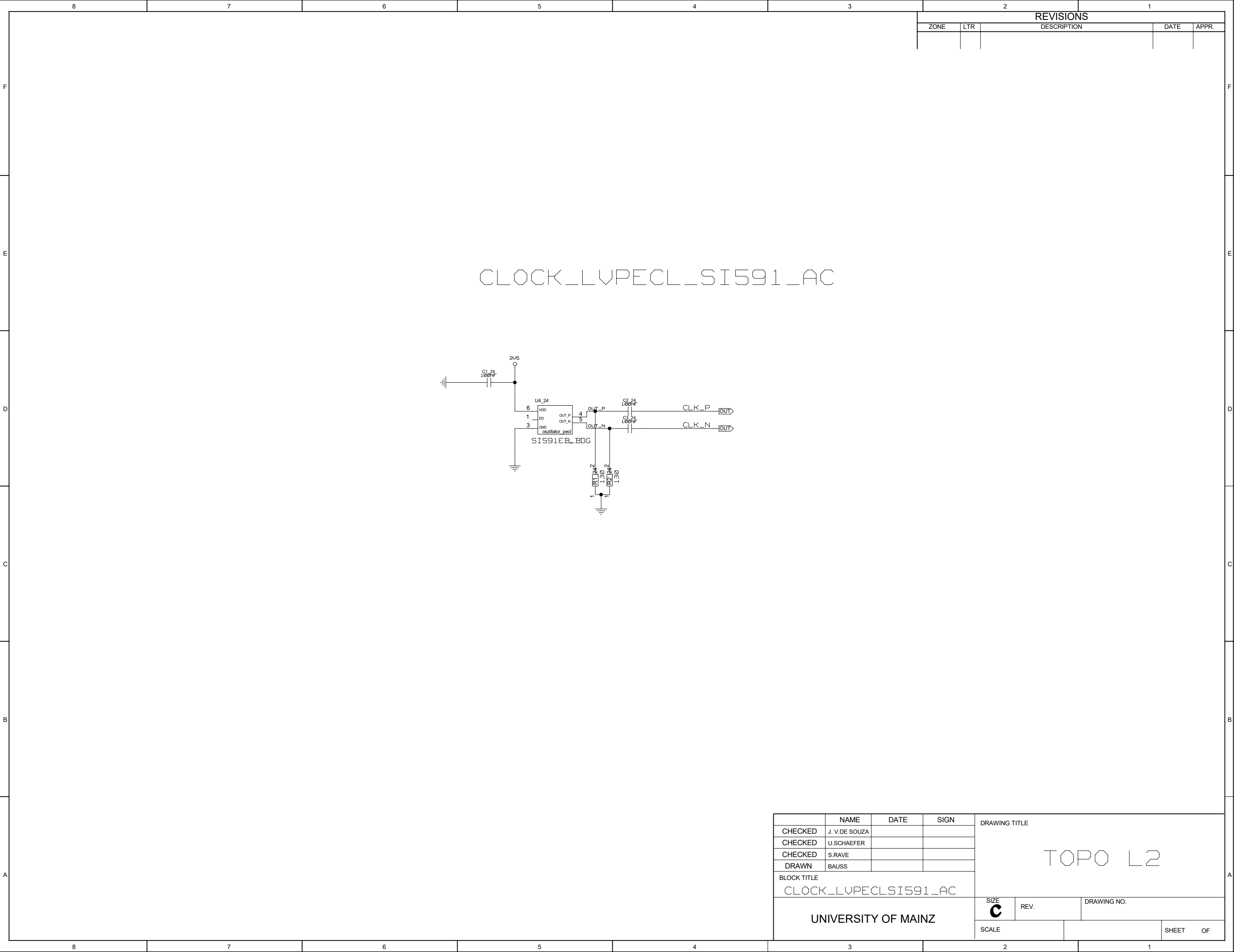
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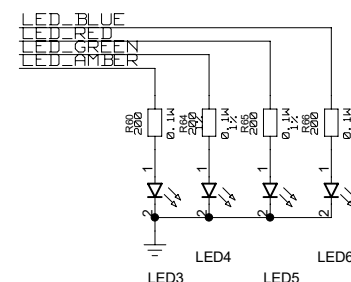
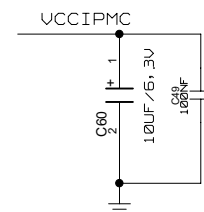
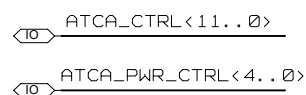
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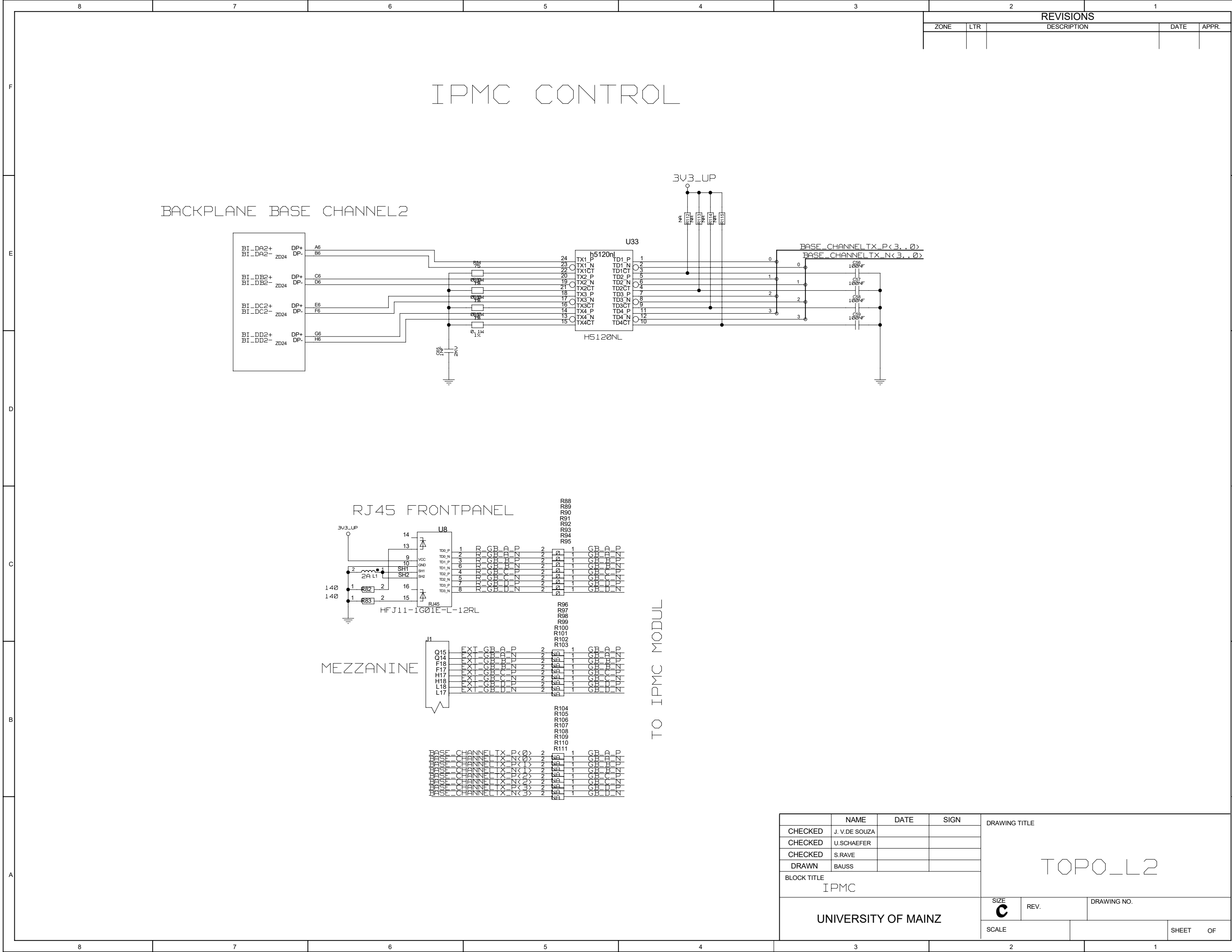
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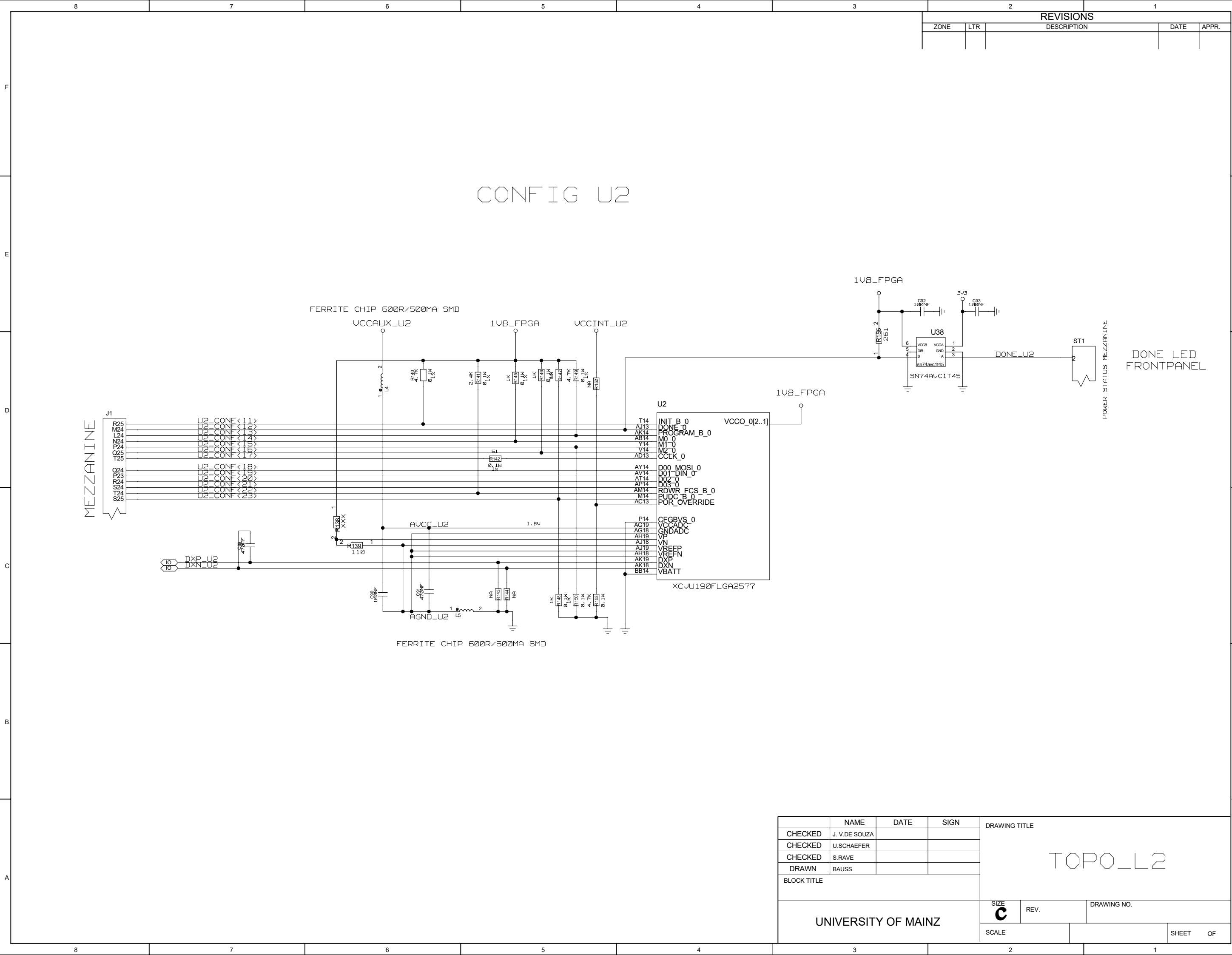


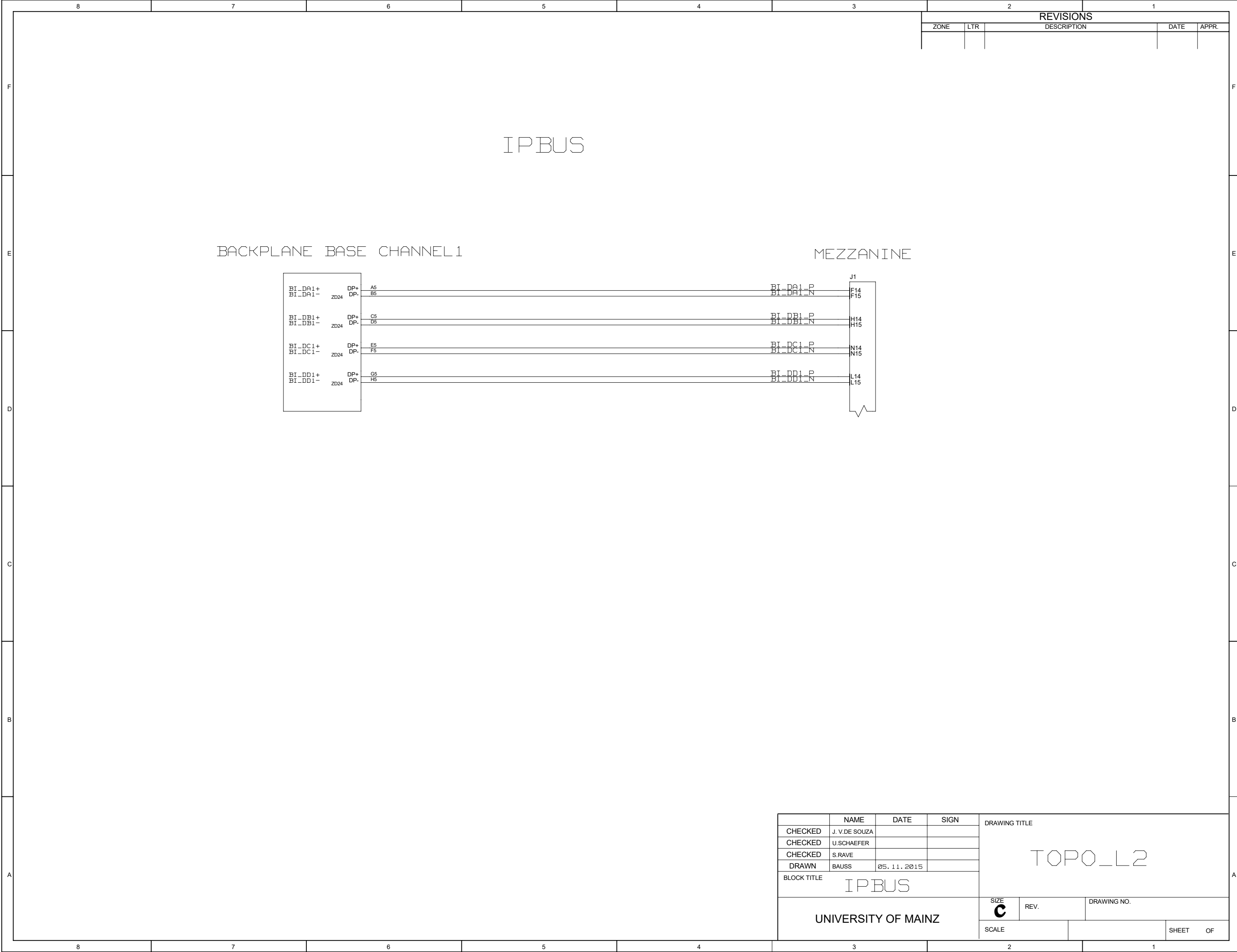
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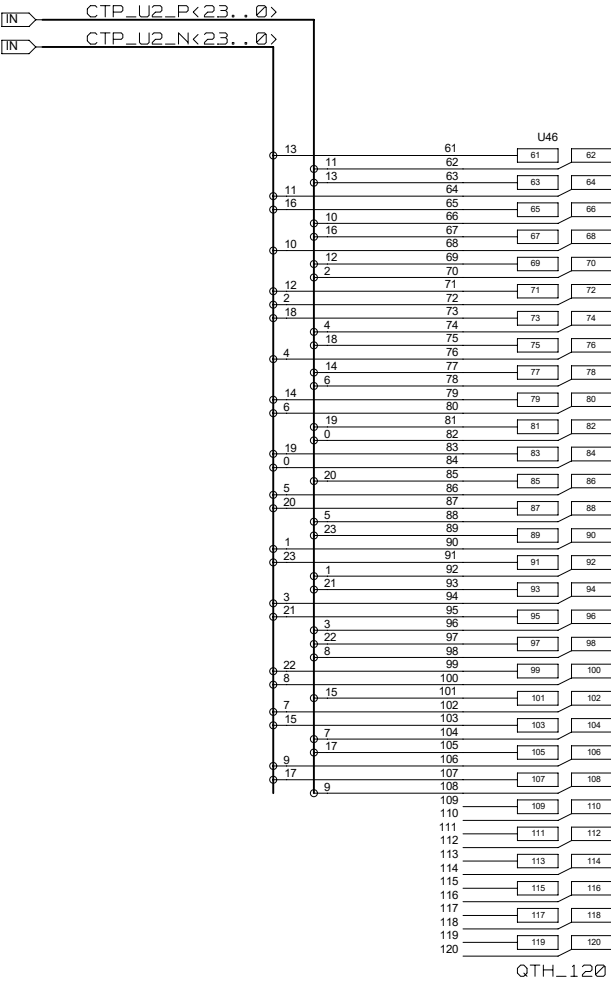
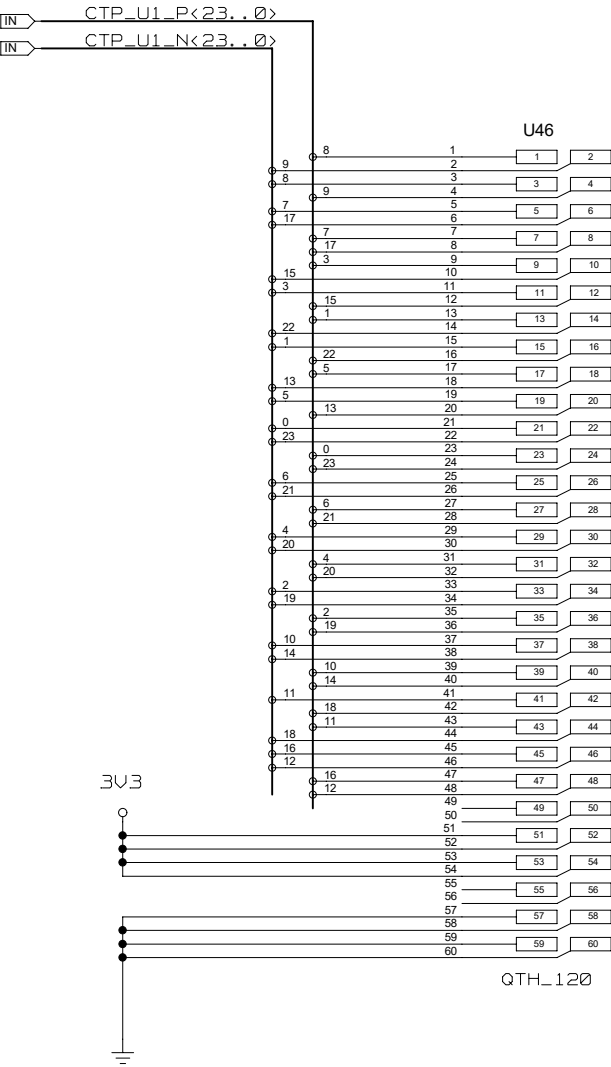
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				SCALE		







CONNECTOR CTP MEZZ



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CHECKED		U.SCHAEFER						
CHECKED		S.RAVE						
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