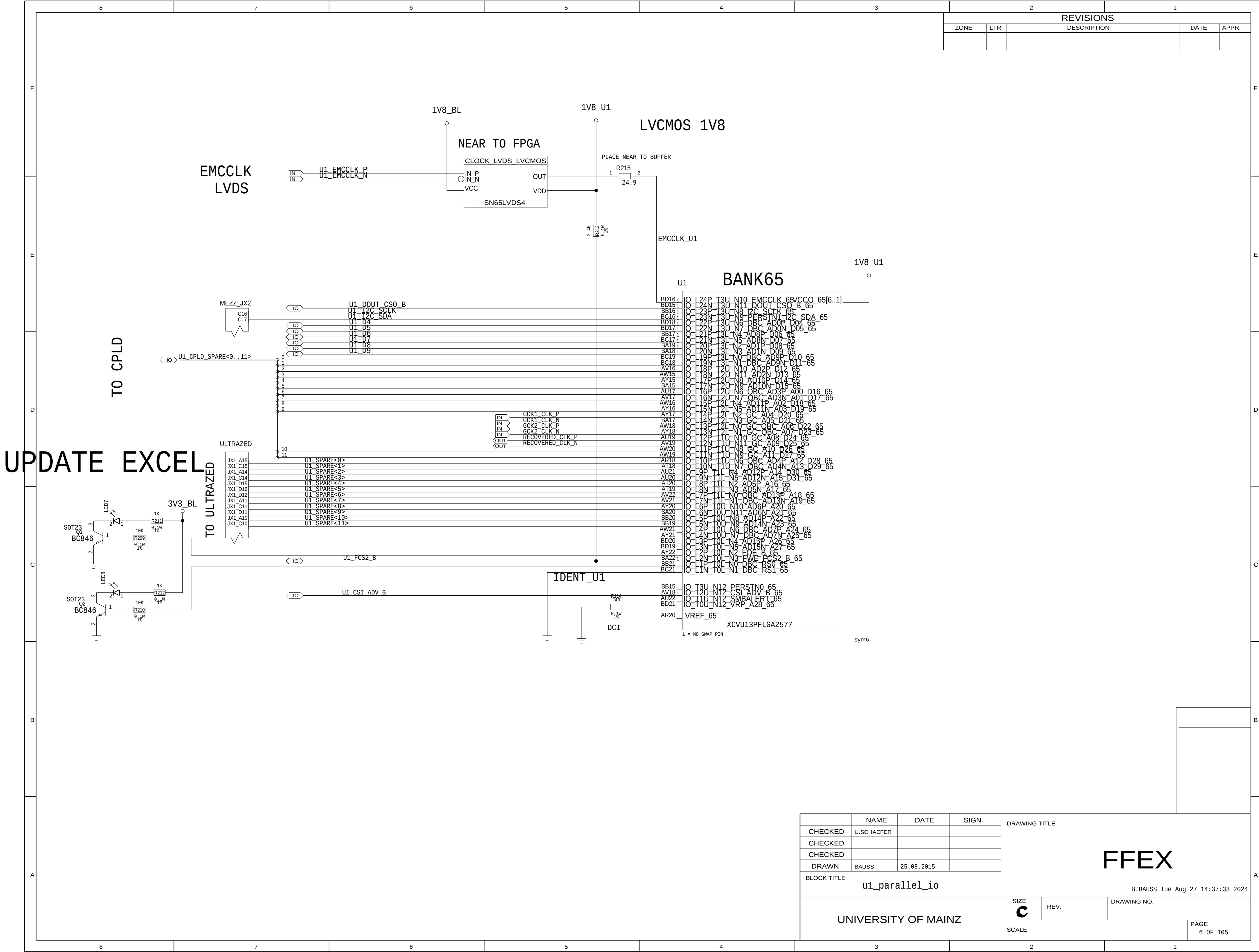
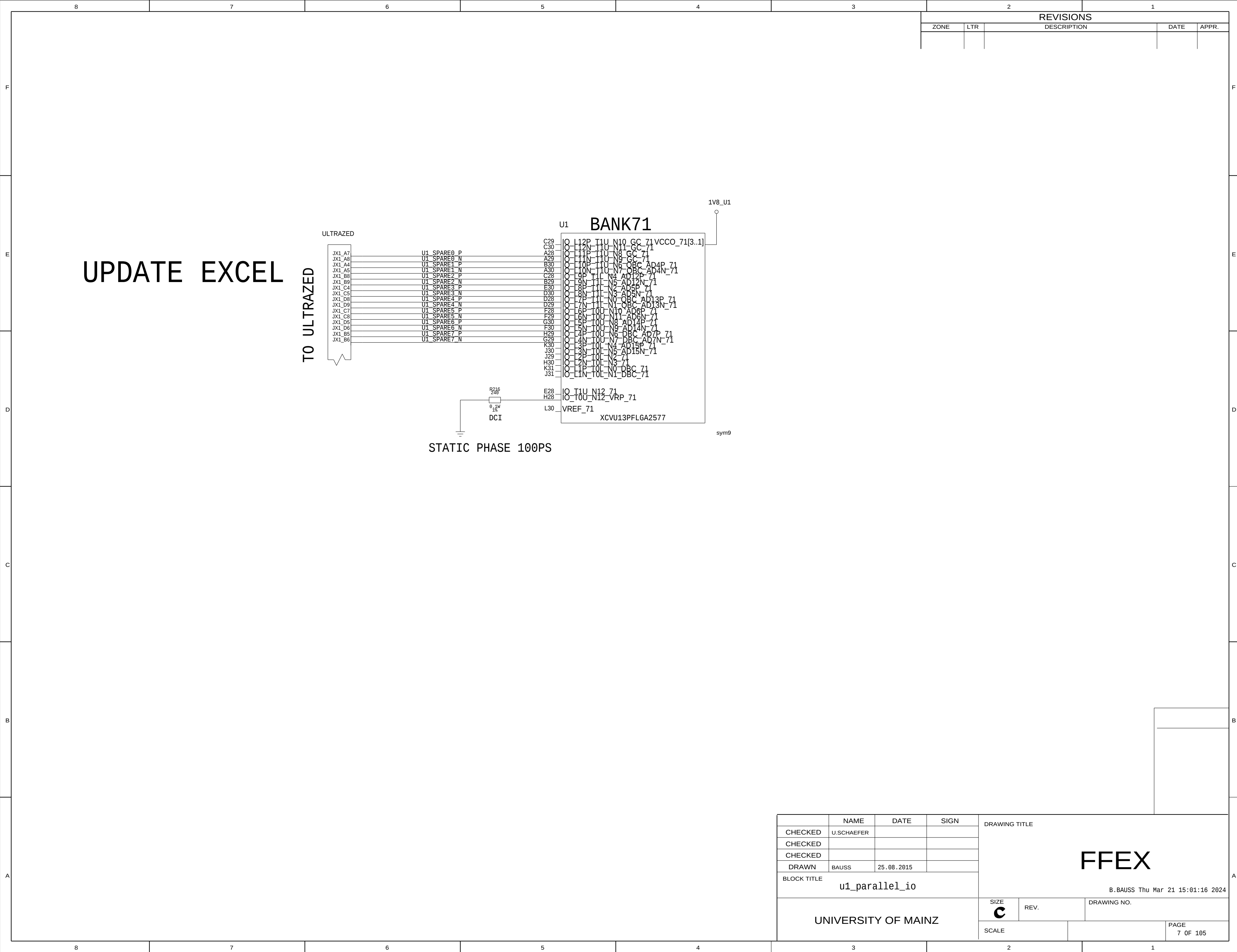




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u1_parallel_io

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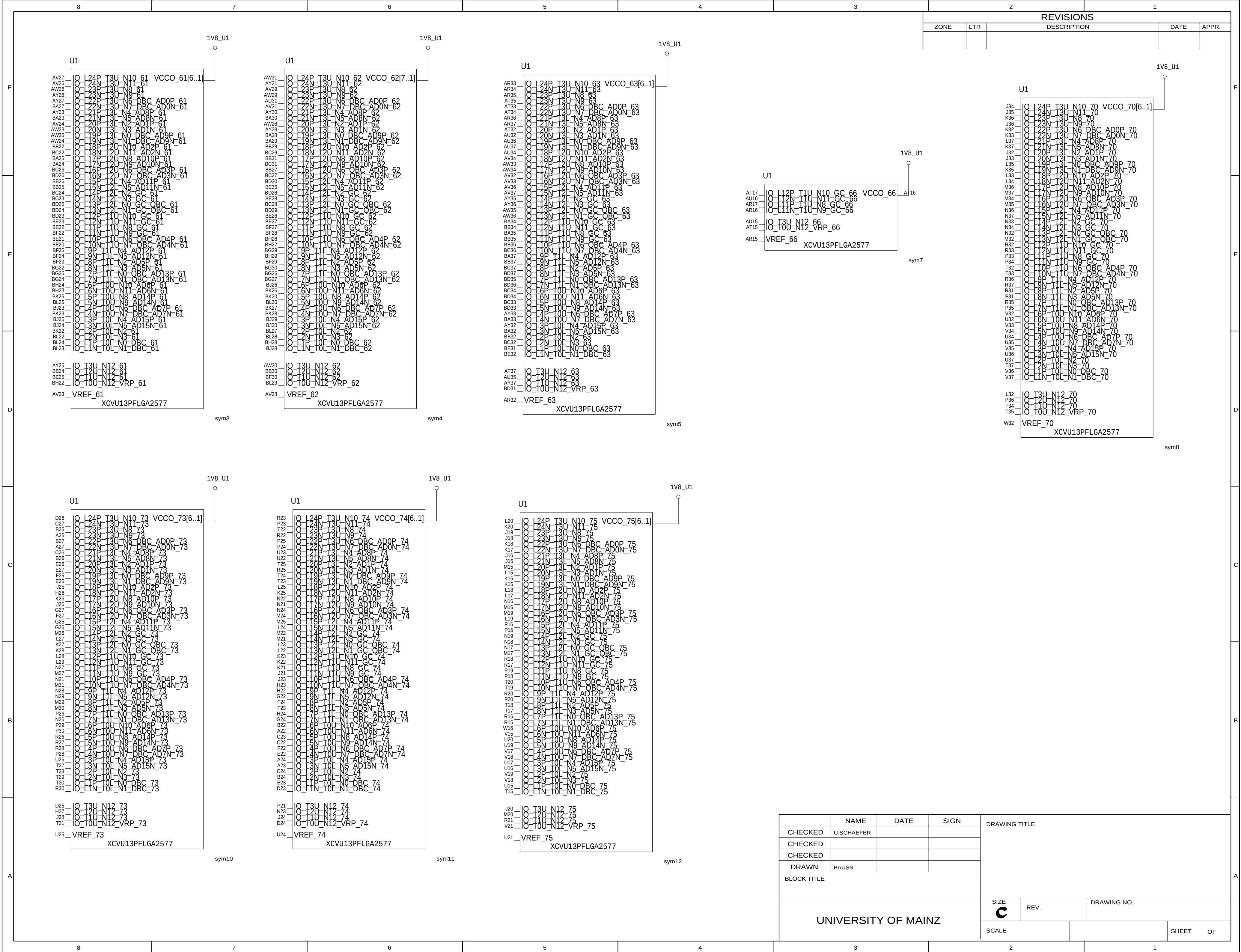
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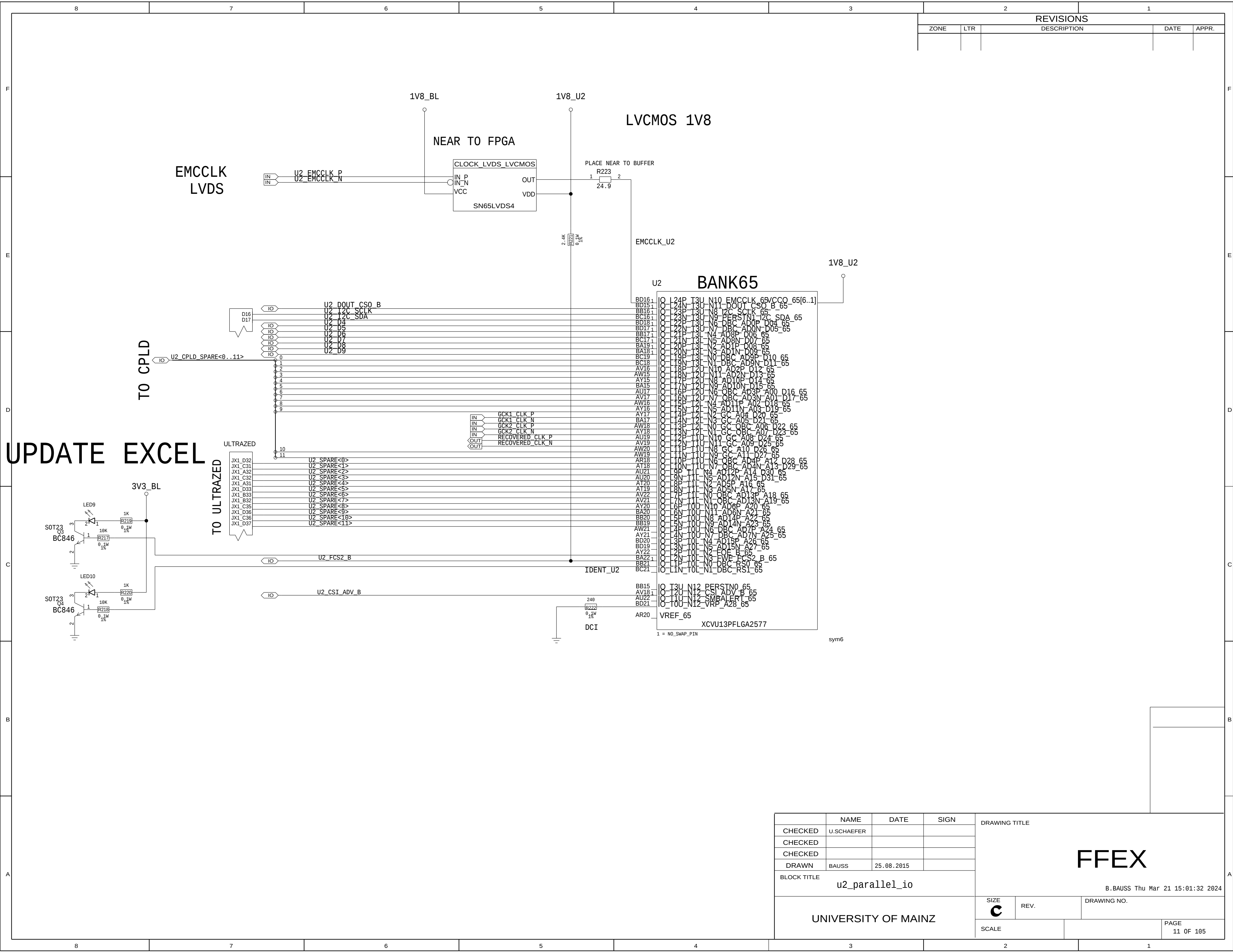
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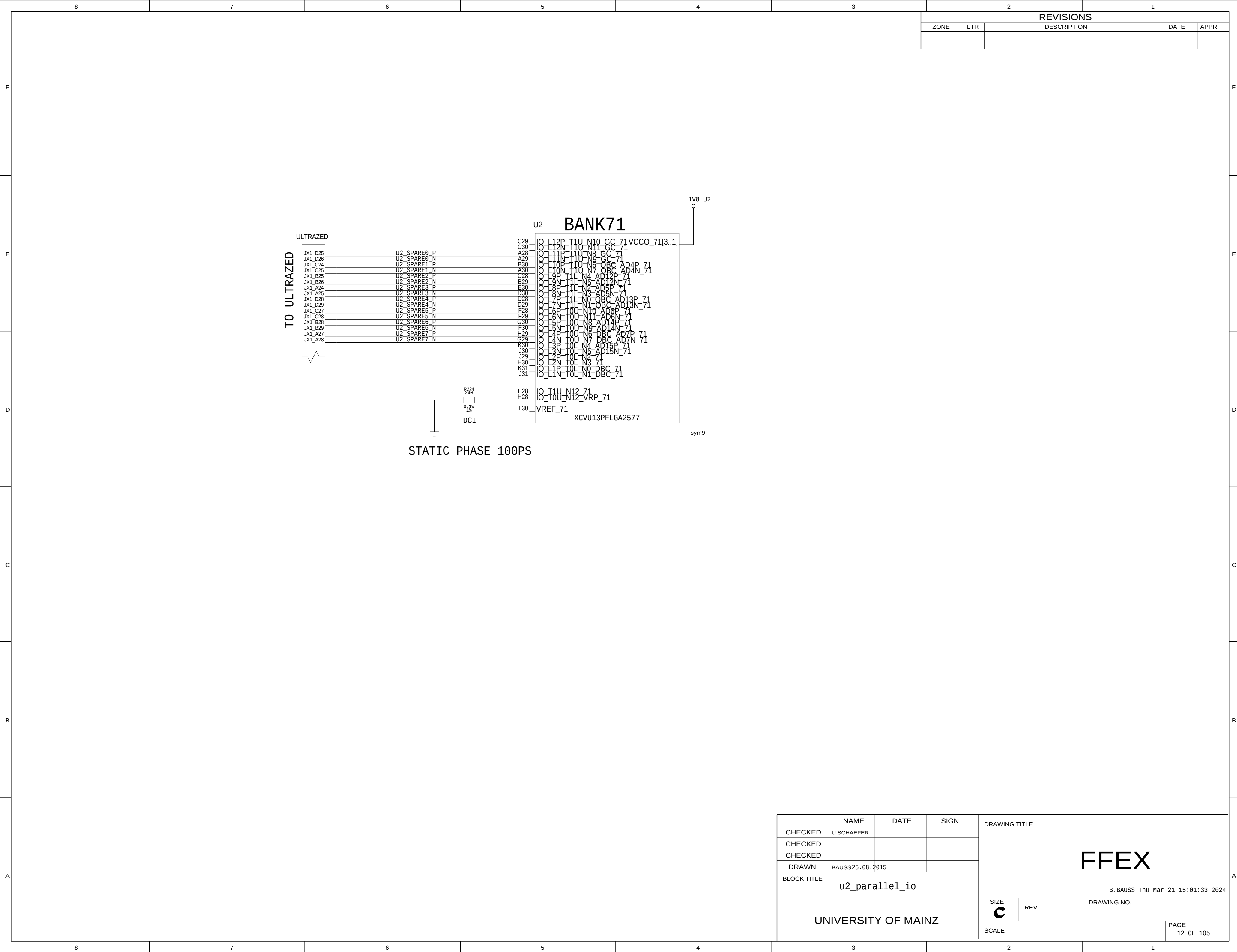
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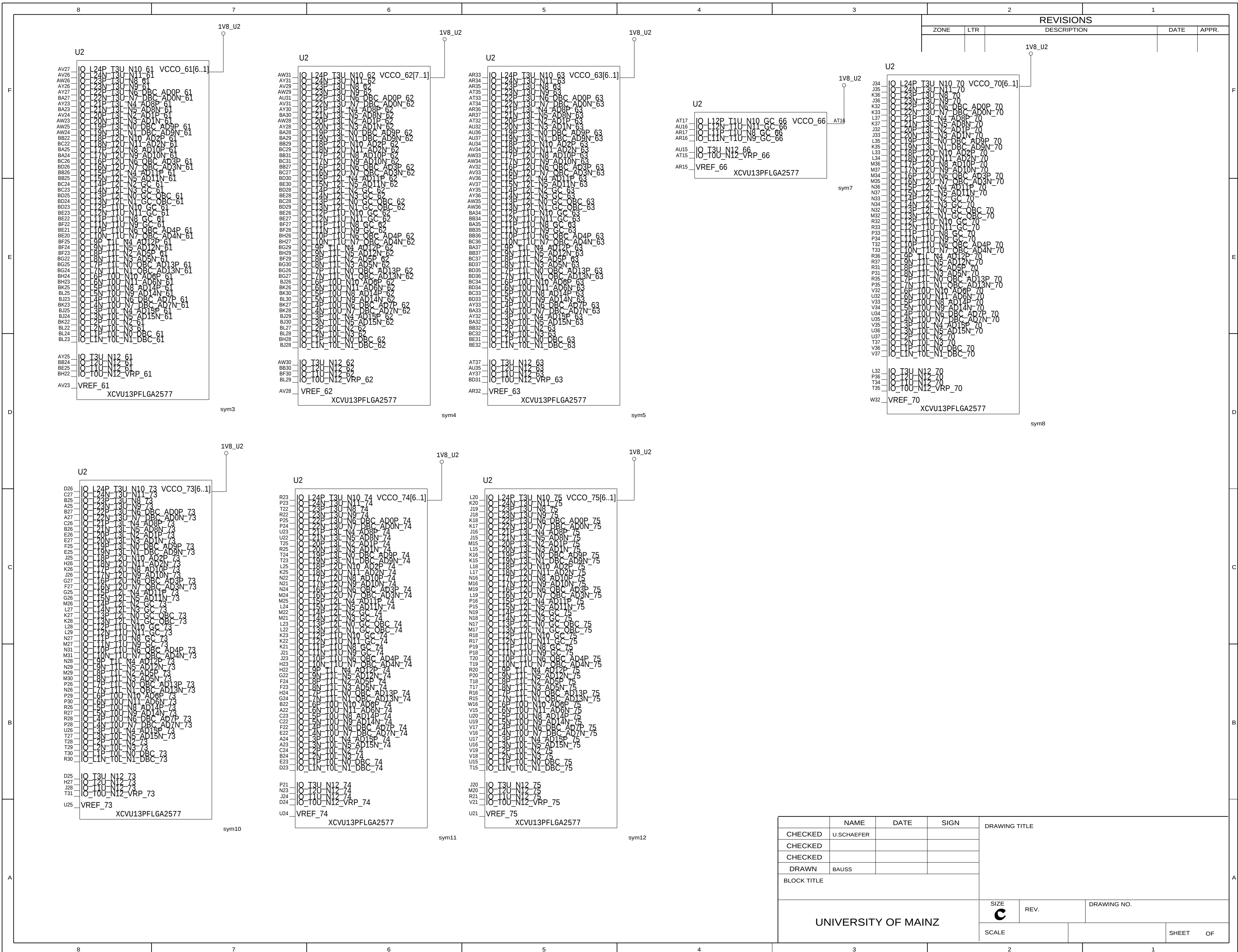
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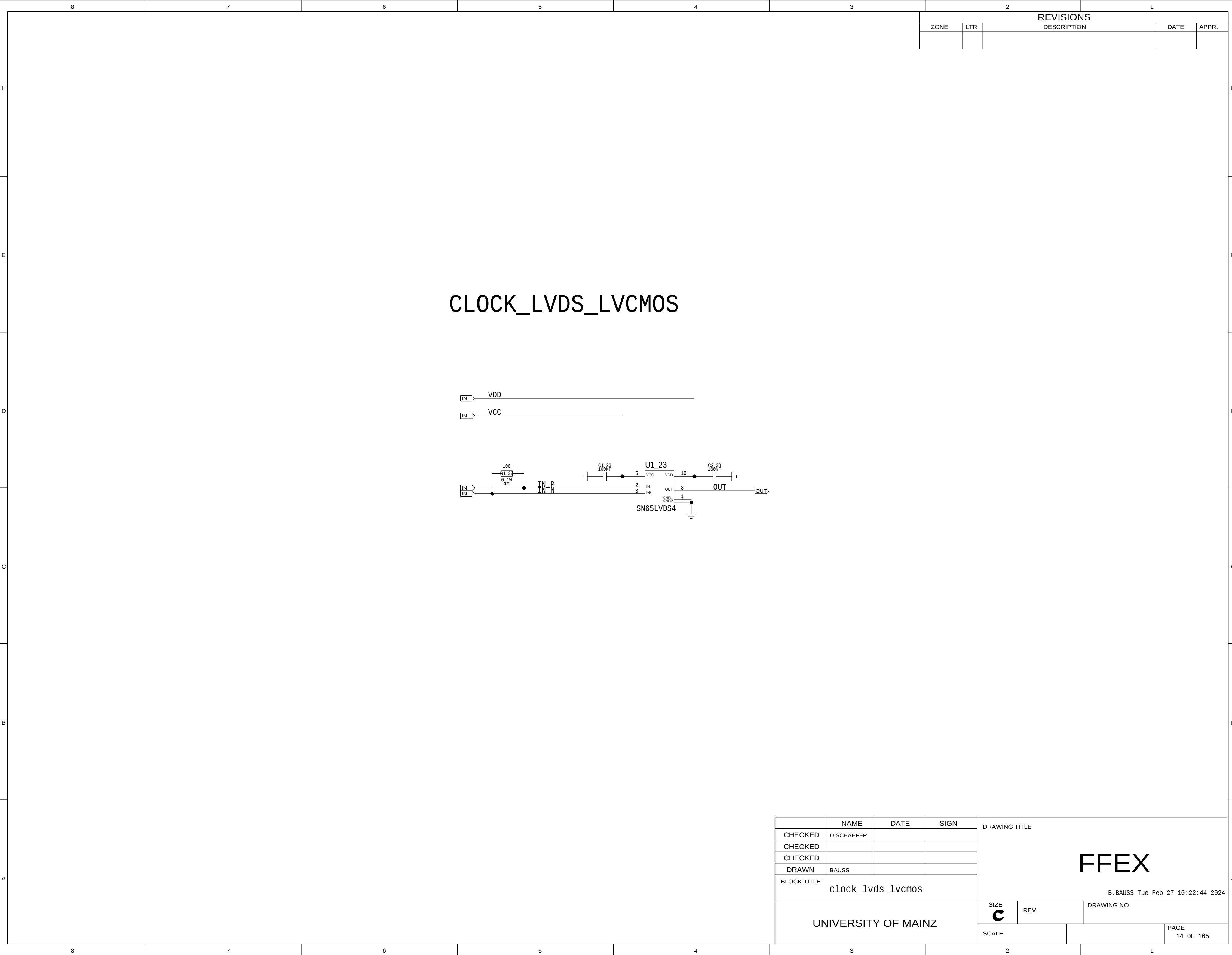




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Diagram illustrating the connection of three XCVU13PFLGA2577 FPGAs (U1, RX1_U1, RX2_U1) to a high-speed optical link system, specifically for 120, 121, 122 and 124, 125, 126 channels.

The diagram shows the internal routing and pin connections for each device, including management signals (MGT1, MGT2, MGT3, MGT4, MGT5) and data signals (RX1_U1_P, RX1_U1_N, RX2_U1_P, RX2_U1_N).

Key components and connections include:

- U1 (Top):** Connected to MGT1, MGT2, MGT3, MGT4, MGT5. Pins 7, 11, 6, 10, 4, 5, 9, 8 are shown. Management signals are connected to pins 4, 5, 9, 8. Data signals are connected to pins 7, 11, 6, 10.
- RX1_U1 (Bottom Left):** Connected to MGT1, MGT2, MGT3, MGT4, MGT5. Pins 7, 11, 6, 10, 4, 5, 9, 8 are shown. Management signals are connected to pins 4, 5, 9, 8. Data signals are connected to pins 7, 11, 6, 10.
- RX2_U1 (Bottom Right):** Connected to MGT1, MGT2, MGT3, MGT4, MGT5. Pins 7, 11, 6, 10, 4, 5, 9, 8 are shown. Management signals are connected to pins 4, 5, 9, 8. Data signals are connected to pins 7, 11, 6, 10.

The diagram also shows the connection of the FPGAs to a 3V3_BL power supply and a 3V3_GND ground plane. The connection to the 3V3_BL is made via a 4.7k resistor and a 0.1uF capacitor. The connection to the 3V3_GND is made via a 4.7k resistor and a 0.1uF capacitor.

The diagram includes a table of pin connections for each device, showing the pin number, the signal name, and the device pin number.

Pin	Signal	Device Pin
7	MGT1_CLK_P<2>	7
11	MGT1_CLK_N<2>	11
6	MGT5_CLK_P<4>	6
10	MGT5_CLK_N<4>	10
4	MGT1_CLK_P<4>	4
5	MGT1_CLK_N<4>	5
9	MGT5_CLK_P<3>	9
8	MGT5_CLK_N<3>	8

8 7 6 5 4 3 2 1

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A

HIGH SPEED OPTICAL LINKS

120, 121, 122

MGT P/N SWAP ALLOWED

MGT1 CLK P<2>
MGT1 CLK N<2>
MGT5 CLK P<4>
MGT5 CLK N<4>

sym13

sym14

sym15

RX1_U1

FF1

FF_CTRL U1<12>
FF_SDA
FF_SCL
FF_CTRL U1<34>
FF_SELECTL
FF_INTL

FF_CTRL U1<35..0>

3V3_BL

SDA_FIREFLY
SCL_FIREFLY

MGT1 CLK P<24..1>
MGT1 CLK N<24..1>
MGT2 CLK P<6..1>
MGT2 CLK N<6..1>
MGT3 CLK P<6..1>
MGT3 CLK N<6..1>
MGT4 CLK P<6..1>
MGT4 CLK N<6..1>
MGT5 CLK P<24..1>
MGT5 CLK N<24..1>

124, 125, 126

MGT P/N SWAP ALLOWED

MGT1 CLK P<4>
MGT1 CLK N<4>
MGT5 CLK P<3>
MGT5 CLK N<3>

sym17

sym18

sym19

RX2_U1

FF2

FF_CTRL U1<25>
FF_SDA
FF_SCL
FF_CTRL U1<18>
FF_SELECTL
FF_INTL

FF_CTRL U1<28>

3V3_BL

SDA_FIREFLY
SCL_FIREFLY

MGT1 CLK P<24..1>
MGT1 CLK N<24..1>
MGT2 CLK P<6..1>
MGT2 CLK N<6..1>
MGT3 CLK P<6..1>
MGT3 CLK N<6..1>
MGT4 CLK P<6..1>
MGT4 CLK N<6..1>
MGT5 CLK P<24..1>
MGT5 CLK N<24..1>

u1_mgt_real_time

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HIGH SPEED OPTICAL LINKS

120, 121, 122

MGT P/N SWAP ALLOWED

MGT1 CLK P<2>
MGT1 CLK N<2>
MGT5 CLK P<4>
MGT5 CLK N<4>

sym13

sym14

sym15

RX1_U1

FF1

FF_CTRL U1<12>
FF_SDA
FF_SCL
FF_CTRL U1<34>
FF_SELECTL
FF_INTL

FF_CTRL U1<35..0>

3V3_BL

SDA_FIREFLY
SCL_FIREFLY

MGT1 CLK P<24..1>
MGT1 CLK N<24..1>
MGT2 CLK P<6..1>
MGT2 CLK N<6..1>
MGT3 CLK P<6..1>
MGT3 CLK N<6..1>
MGT4 CLK P<6..1>
MGT4 CLK N<6..1>
MGT5 CLK P<24..1>
MGT5 CLK N<24..1>

124, 125, 126

MGT P/N SWAP ALLOWED

MGT1 CLK P<4>
MGT1 CLK N<4>
MGT5 CLK P<3>
MGT5 CLK N<3>

sym17

sym18

sym19

RX2_U1

FF2

FF_CTRL U1<25>
FF_RESET
FF_SDA
FF_SCL
FF_CTRL U1<18>
FF_SELECTL
FF_INTL

FF_CTRL U1<28>

3V3_BL

SDA_FIREFLY
SCL_FIREFLY

MGT1 CLK P<24..1>
MGT1 CLK N<24..1>
MGT2 CLK P<6..1>
MGT2 CLK N<6..1>
MGT3 CLK P<6..1>
MGT3 CLK N<6..1>
MGT4 CLK P<6..1>
MGT4 CLK N<6..1>
MGT5 CLK P<24..1>
MGT5 CLK N<24..1>

FFEX

u1_mgt_real_time

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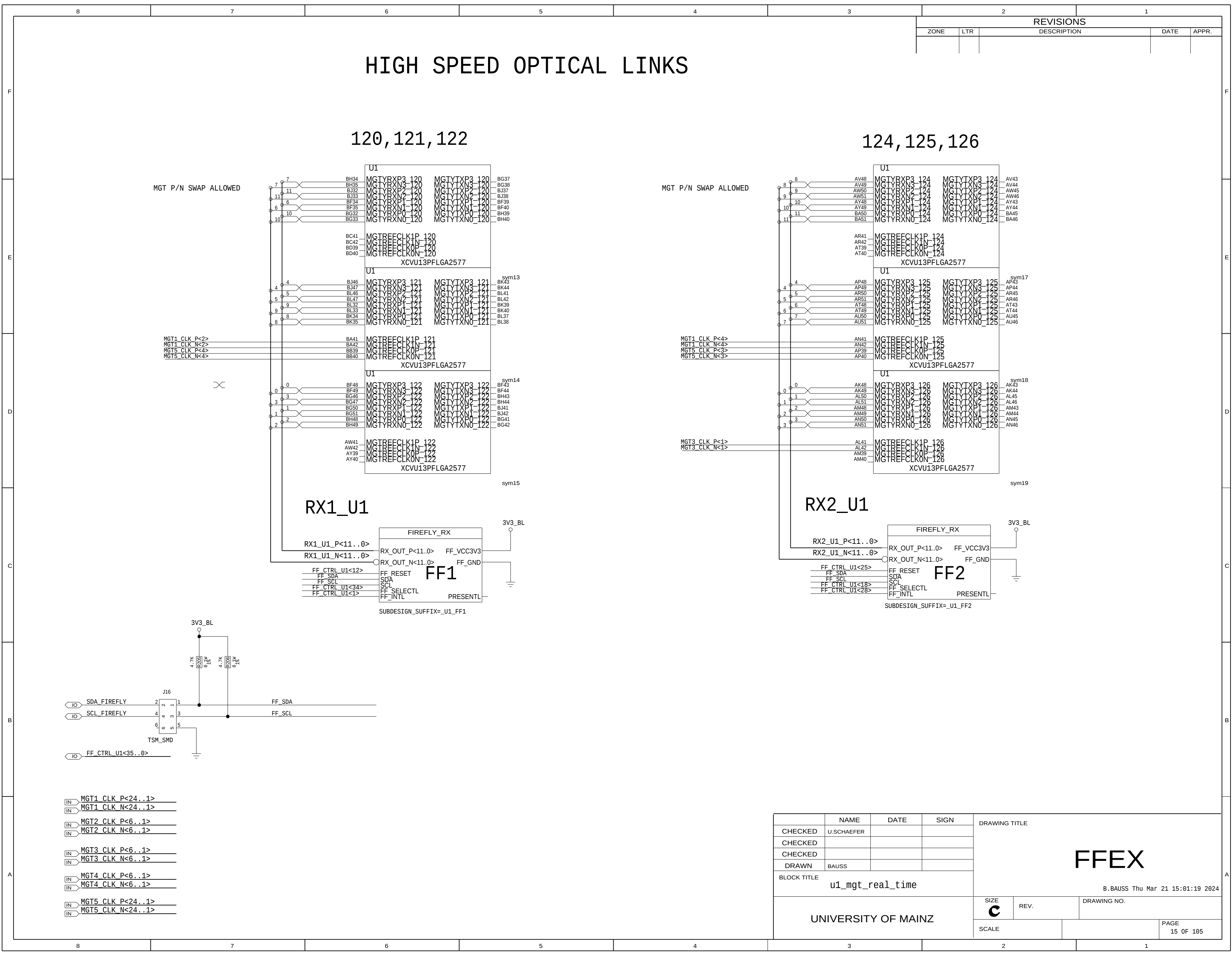
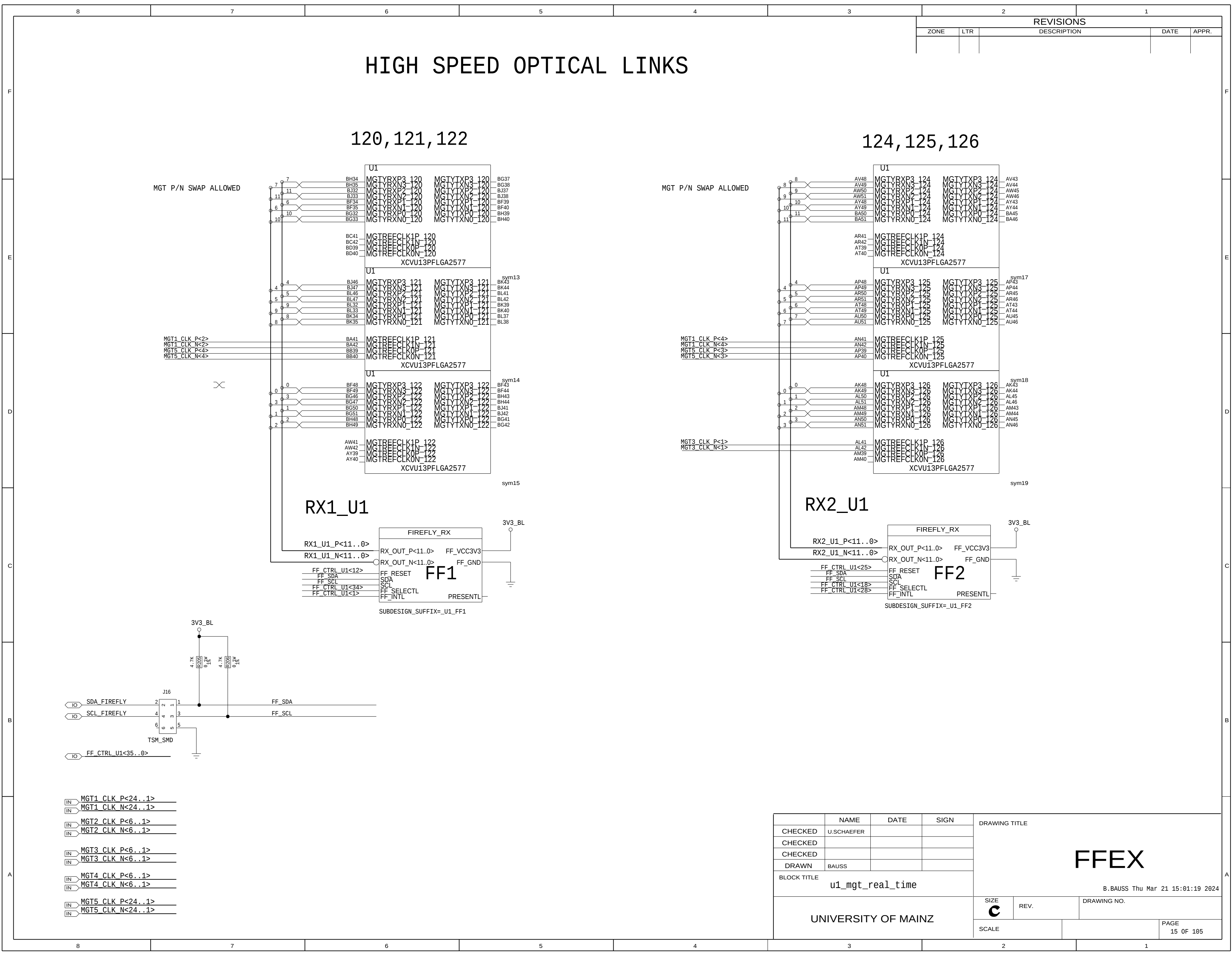
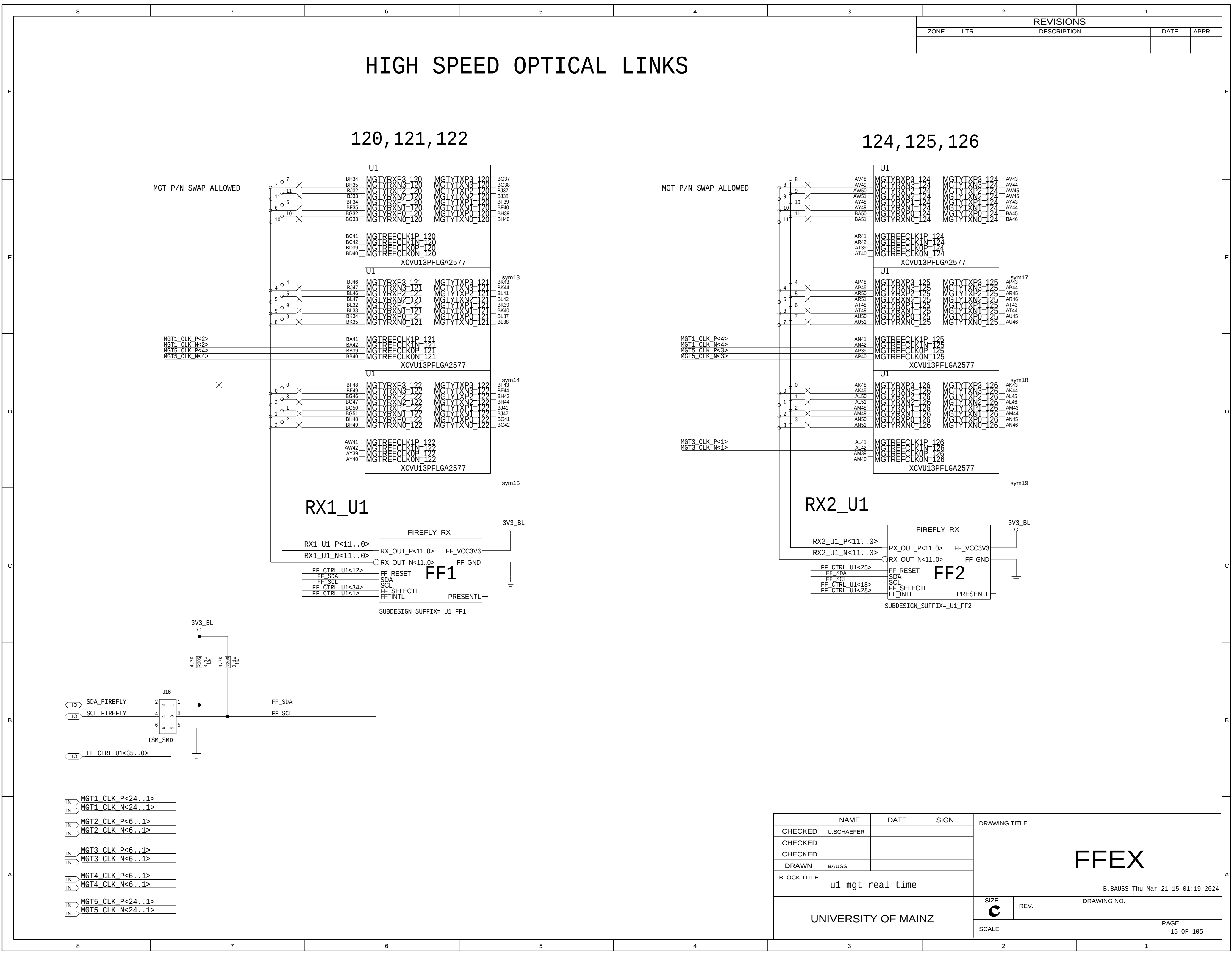
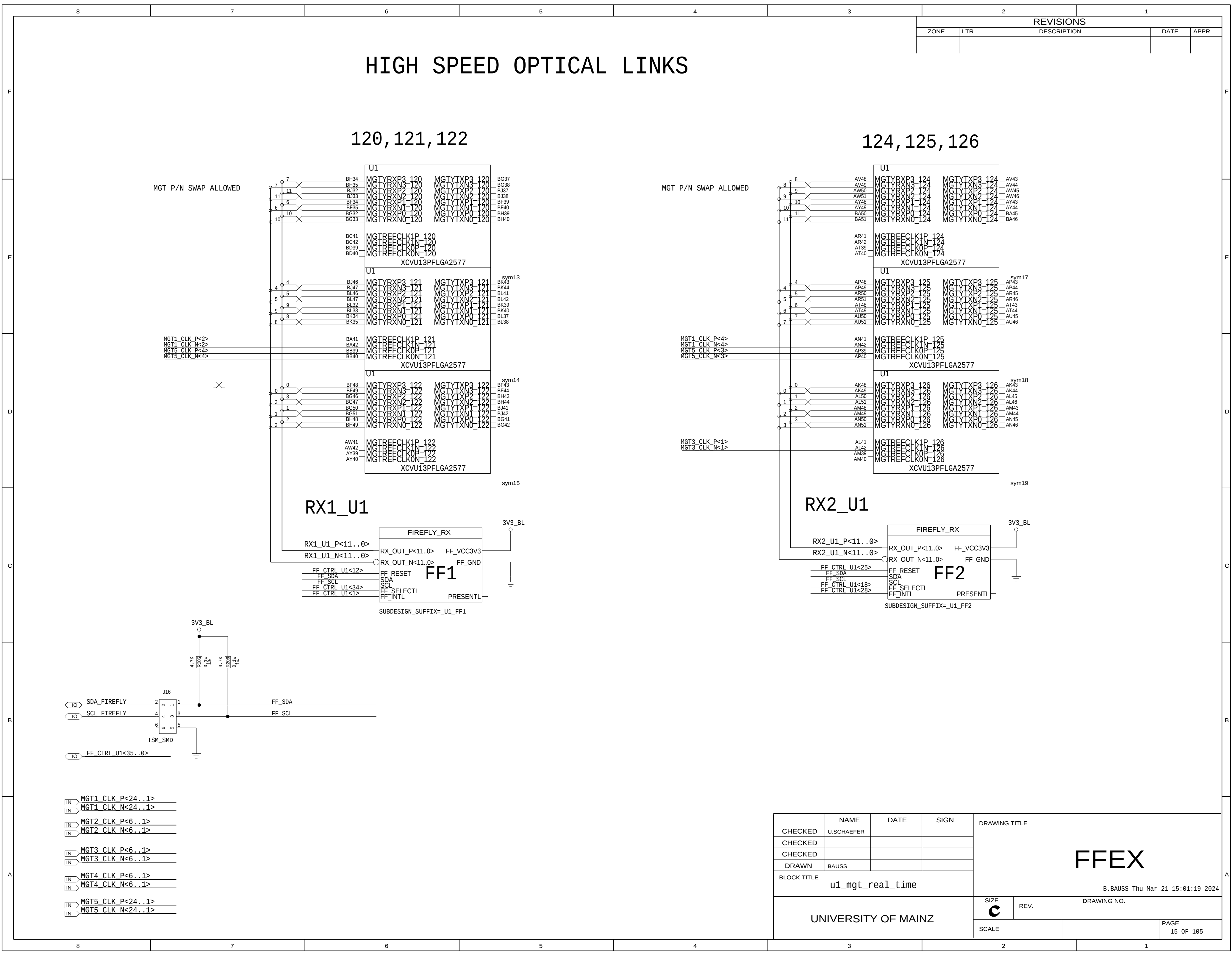
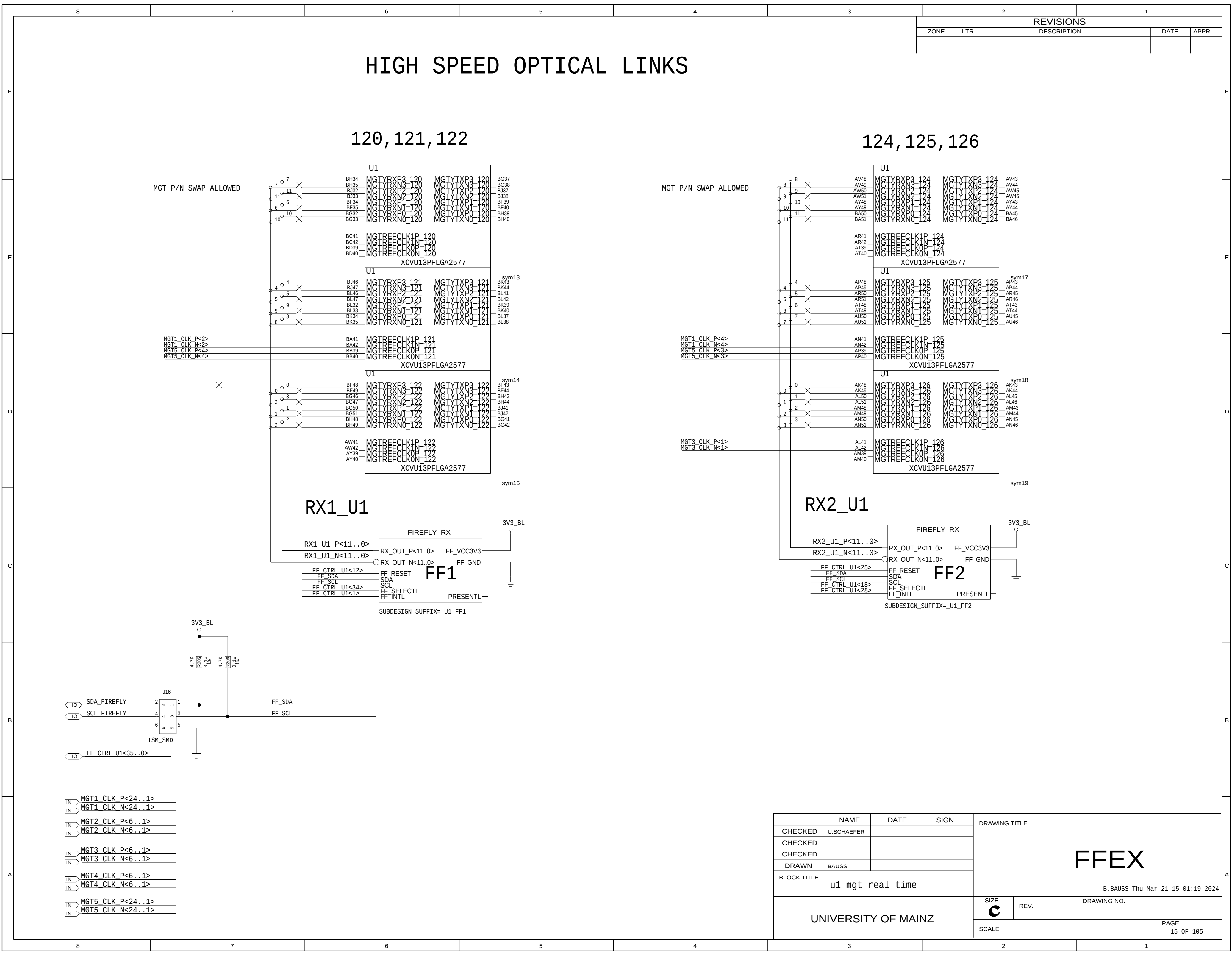
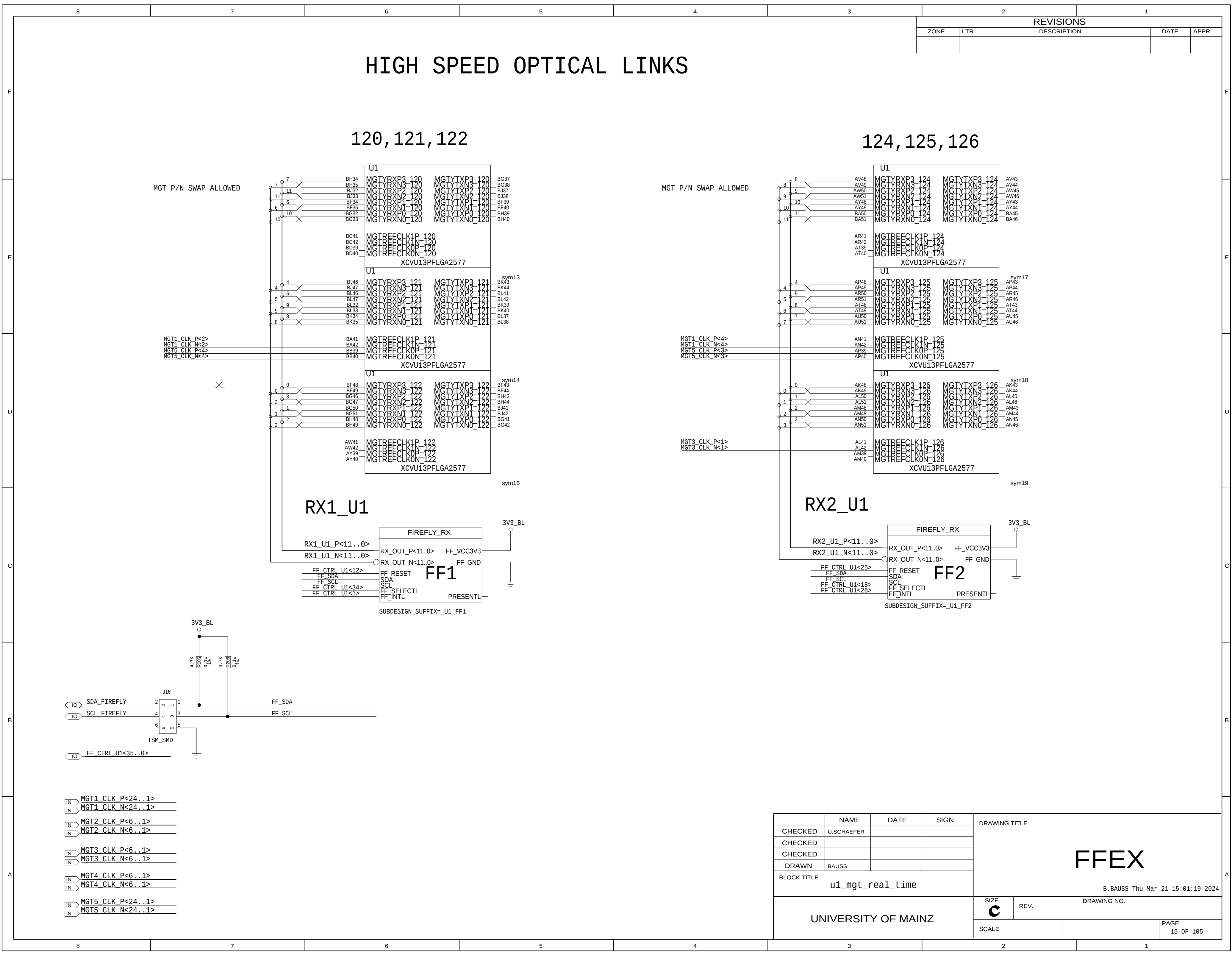
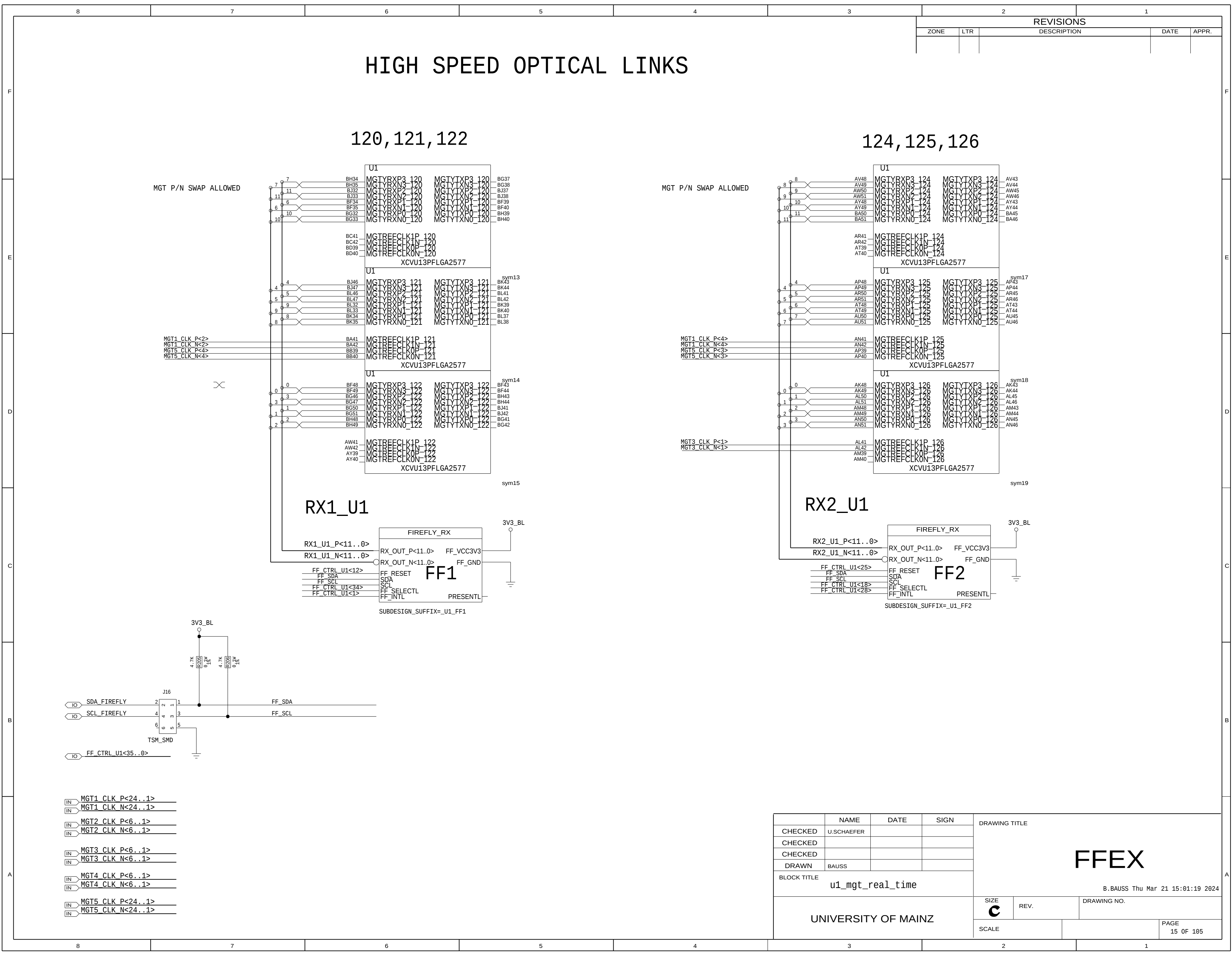
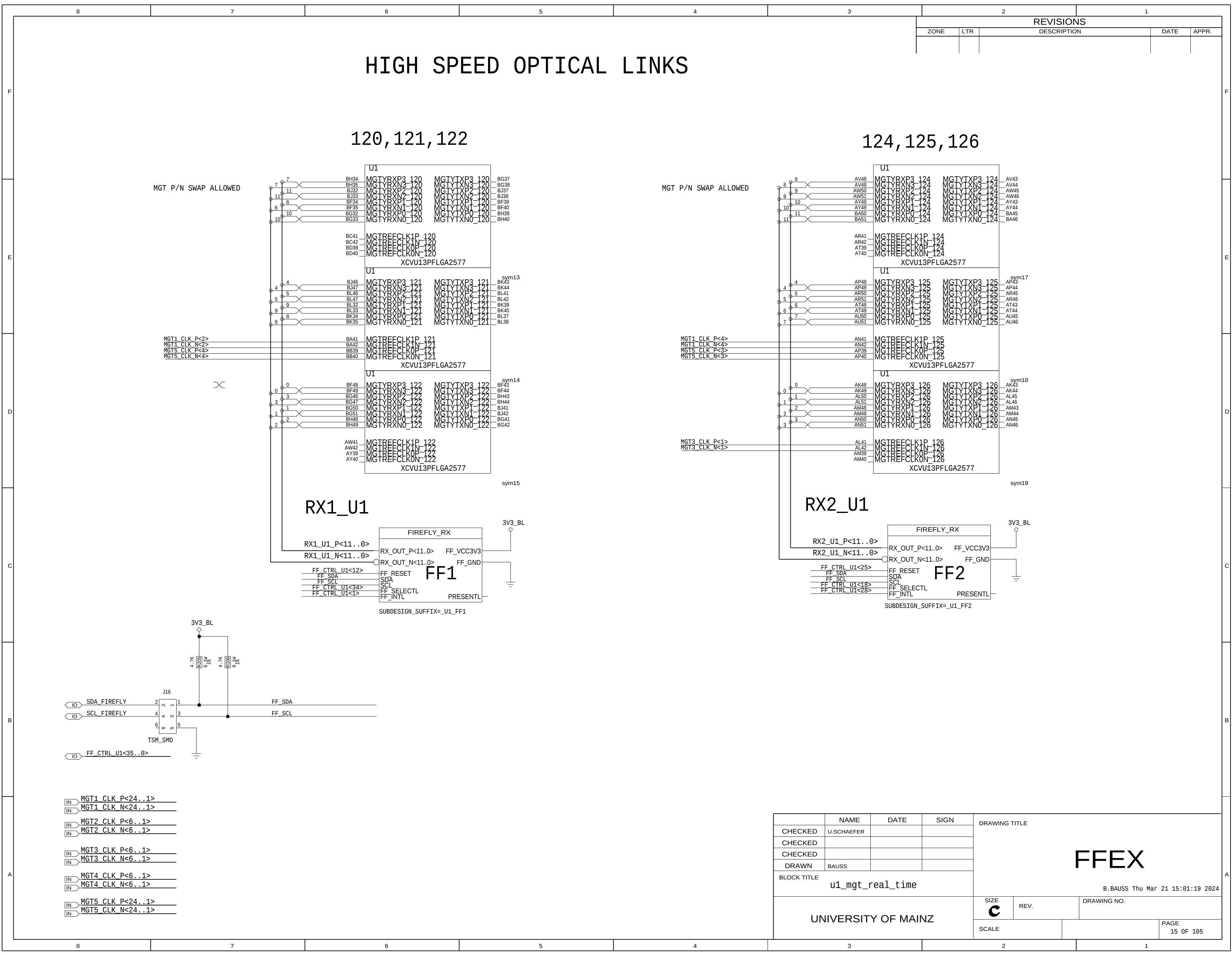


Diagram illustrating the connection of three XCVU13PFLGA2577 FPGAs (U1, RX1_U1, RX2_U1) to a high-speed optical link system, specifically for the 120, 121, 122 and 124, 125, 126 pin configurations.

The diagram shows the internal routing and pin connections for each device, including the MGT (Management) and RX (Receiver) blocks.

Device 1 (U1): Shows connections for pins 120, 121, and 122. The MGT block is connected to the RX block via the MGT P/N SWAP ALLOWED signal. The RX block is connected to the RX1_U1 block.

Device 2 (RX1_U1): Shows connections for pins 120, 121, and 122. The RX block is connected to the RX1_U1 block.

Device 3 (RX2_U1): Shows connections for pins 124, 125, and 126. The MGT block is connected to the RX block via the MGT P/N SWAP ALLOWED signal. The RX block is connected to the RX2_U1 block.

Legend:

- IO: Input/Output
- IN: Input
- FF: Firefly
- FF_CTRL: Firefly Control
- FF_SDA: Firefly Serial Data
- FF_SCL: Firefly Serial Clock
- FF_SELECT: Firefly Select
- FF_INTL: Firefly Internal
- FF_VCC3V3: Firefly VCC3V3
- FF_GND: Firefly Ground
- FF_RESET: Firefly Reset
- FF_INTL: Firefly Internal
- FF_SELECT: Firefly Select
- FF_CTRL: Firefly Control
- FF_SDA: Firefly Serial Data
- FF_SCL: Firefly Serial Clock
- FF_VCC3V3: Firefly VCC3V3
- FF_GND: Firefly Ground
- FF_RESET: Firefly Reset

Table 1: MGT Signals

Signal	Pin
MGT1_CLK_P<2>	120
MGT1_CLK_N<2>	121
MGT5_CLK_P<4>	122
MGT5_CLK_N<4>	123

Table 2: RX Signals

Signal	Pin
RX1_U1_P<11..0>	120
RX1_U1_N<11..0>	121
RX2_U1_P<11..0>	124
RX2_U1_N<11..0>	125

Table 3: RX Signals

Signal	Pin
RX2_U1_P<11..0>	126
RX2_U1_N<11..0>	127

Table 4: RX Signals

Signal	Pin
RX2_U1_P<11..0>	128
RX2_U1_N<11..0>	129

Table 5: RX Signals

Signal	Pin
RX2_U1_P<11..0>	130
RX2_U1_N<11..0>	131

Table 6: RX Signals

Signal	Pin
RX2_U1_P<11..0>	132
RX2_U1_N<11..0>	133

Table 7: RX Signals

Signal	Pin
RX2_U1_P<11..0>	134
RX2_U1_N<11..0>	135

Table 8: RX Signals

Signal	Pin
RX2_U1_P<11..0>	136
RX2_U1_N<11..0>	137

Table 9: RX Signals

Signal	Pin
RX2_U1_P<11..0>	138
RX2_U1_N<11..0>	139

Table 10: RX Signals

Signal	Pin
RX2_U1_P<11..0>	140
RX2_U1_N<11..0>	141

Table 11: RX Signals

Signal	Pin
RX2_U1_P<11..0>	142
RX2_U1_N<11..0>	143

Table 12: RX Signals

Signal	Pin
RX2_U1_P<11..0>	144
RX2_U1_N<11..0>	145

Table 13: RX Signals

Signal	Pin
RX2_U1_P<11..0>	146
RX2_U1_N<11..0>	147

Table 14: RX Signals

Signal	Pin
RX2_U1_P<11..0>	148
RX2_U1_N<11..0>	149

Table 15: RX Signals

Signal	Pin
RX2_U1_P<11..0>	150
RX2_U1_N<11..0>	151

Table 16: RX Signals

Signal	Pin
RX2_U1_P<11..0>	152
RX2_U1_N<11..0>	153

Table 17: RX Signals

Signal	Pin
RX2_U1_P<11..0>	154
RX2_U1_N<11..0>	155

Table 18: RX Signals

Signal	Pin
RX2_U1_P<11..0>	156
RX2_U1_N<11..0>	157

Table 19: RX Signals

Signal	Pin
RX2_U1_P<11..0>	158
RX2_U1_N<11..0>	159

Table 20: RX Signals

Signal	Pin
RX2_U1_P<11..0>	160
RX2_U1_N<11..0>	161

Table 21: RX Signals

Signal	Pin
RX2_U1_P<11..0>	162
RX2_U1_N<11..0>	163

Table 22: RX Signals

Signal	Pin
RX2_U1_P<11..0>	164
RX2_U1_N<11..0>	165

Table 23: RX Signals

Signal	Pin
RX2_U1_P<11..0>	166
RX2_U1_N<11..0>	167

Table 24: RX Signals

Signal	Pin
RX2_U1_P<11..0>	168
RX2_U1_N<11..0>	169

Table 25: RX Signals

Signal	Pin
RX2_U1_P<11..0>	170
RX2_U1_N<11..0>	171

Table 26: RX Signals

Signal	Pin
RX2_U1_P<11..0>	172
RX2_U1_N<11..0>	173

Table 27: RX Signals

Signal	Pin
RX2_U1_P<11..0>	174
RX2_U1_N<11..0>	175

Table 28: RX Signals

Signal	Pin
RX2_U1_P<11..0>	176
RX2_U1_N<11..0>	177

Table 29: RX Signals

Signal	Pin
RX2_U1_P<11..0>	178
RX2_U1_N<11..0>	179

Table 30: RX Signals

Signal	Pin
RX2_U1_P<11..0>	180
RX2_U1_N<11..0>	181

Table 31: RX Signals

Signal	Pin
RX2_U1_P<11..0>	182
RX2_U1_N<11..0>	183

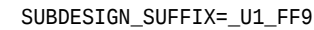
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Signal	Pin
RX2_U1_P<11..0>	184
RX2_U1_N<11..0>	185

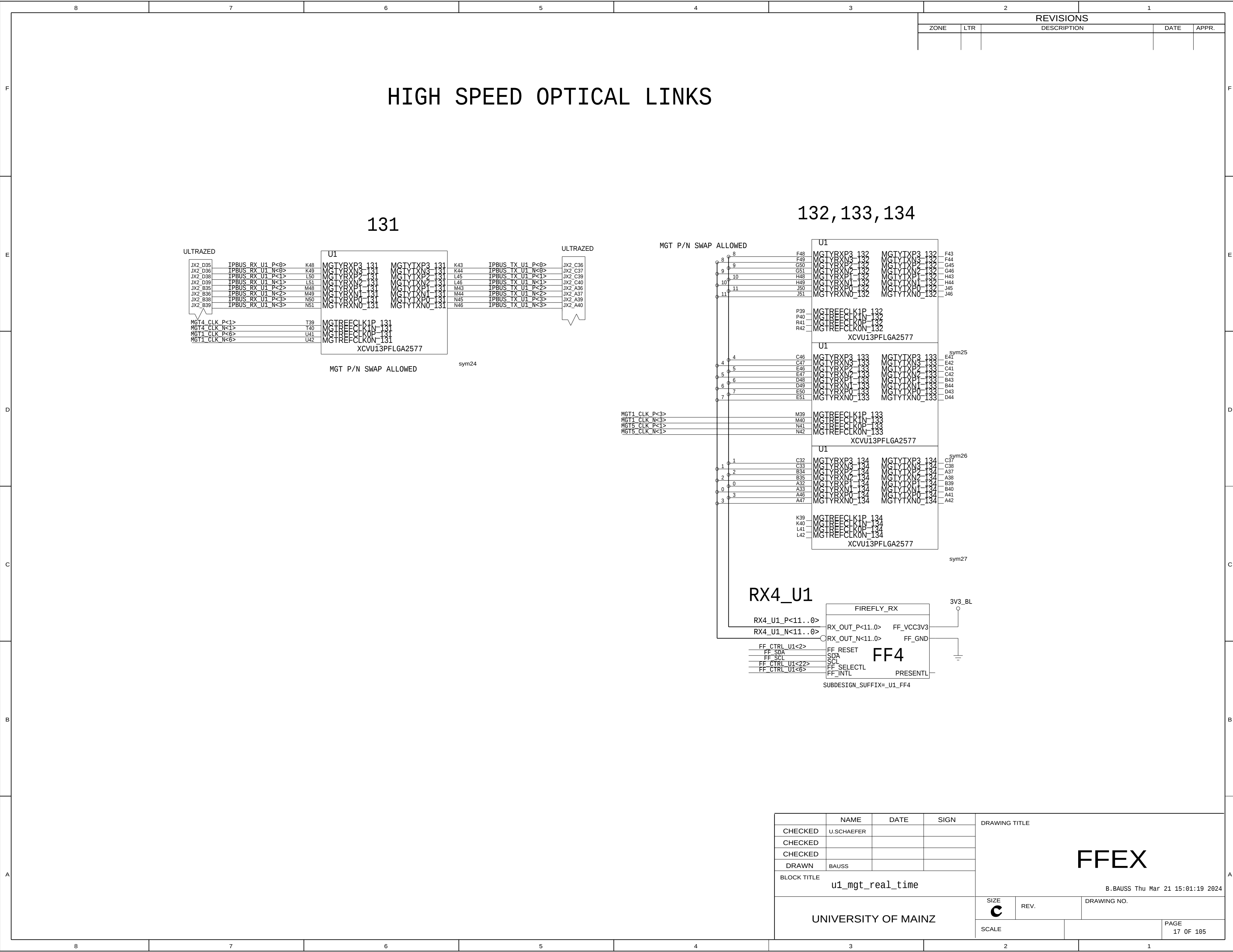
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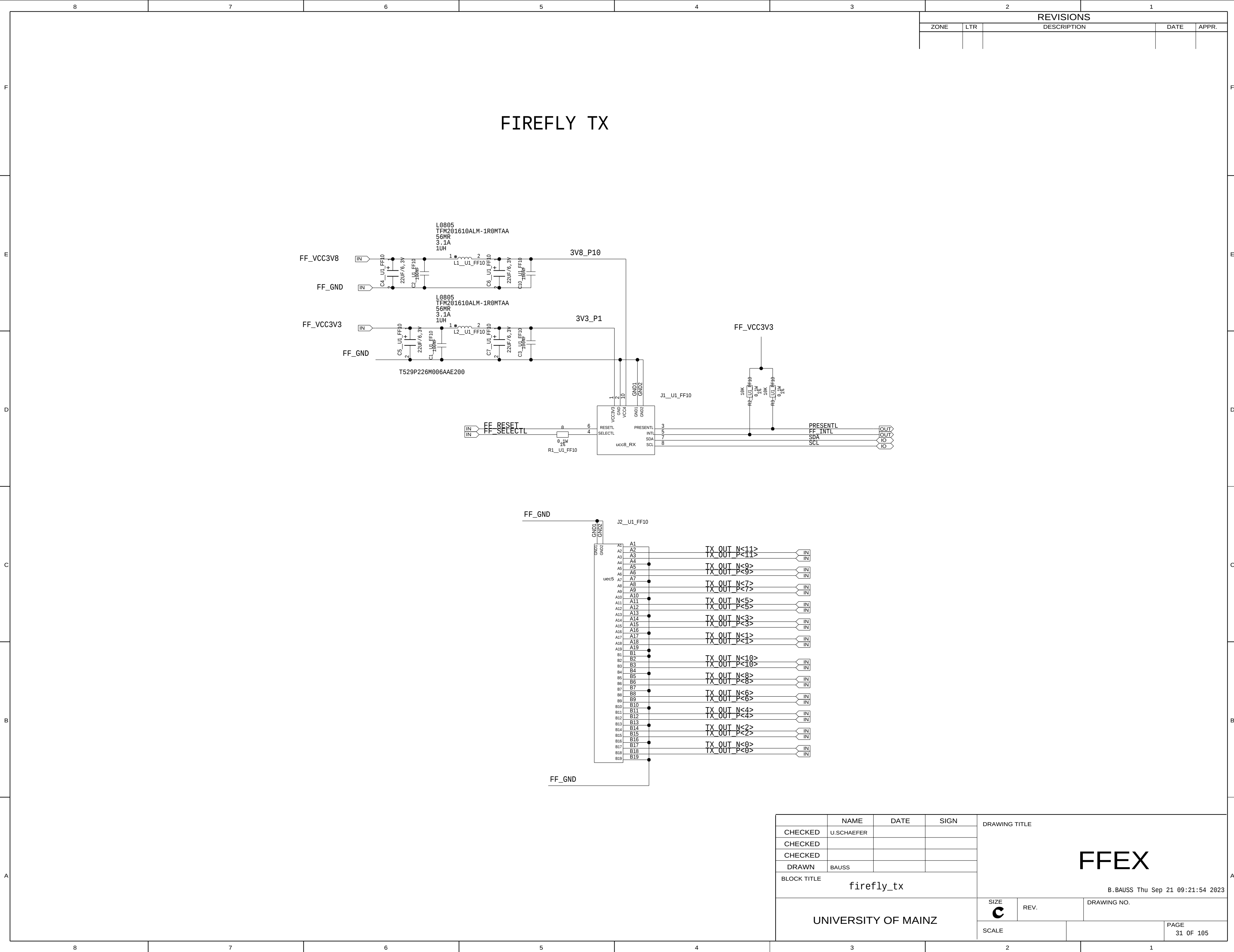
Signal	Pin
RX2_U1_P<11..0>	186

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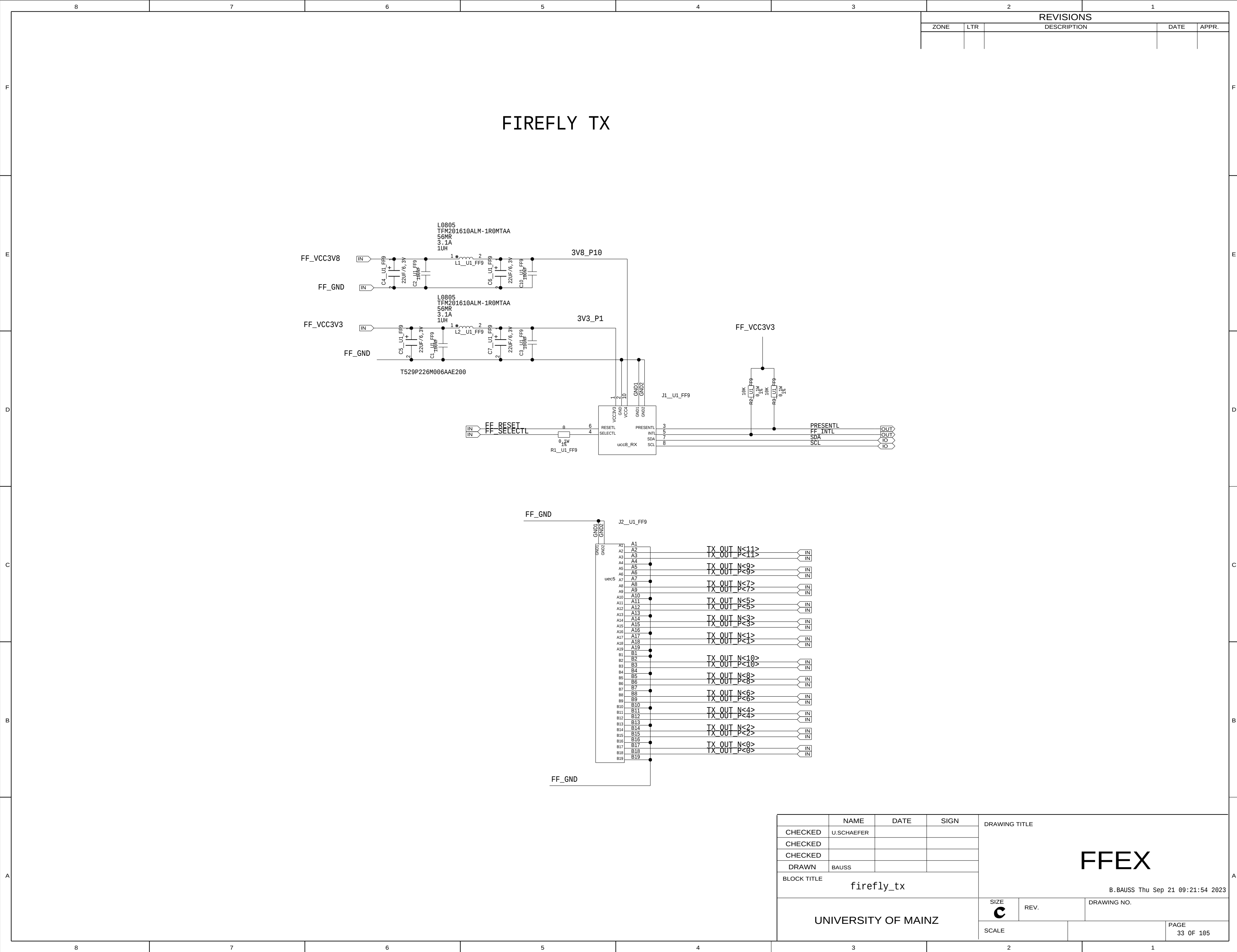
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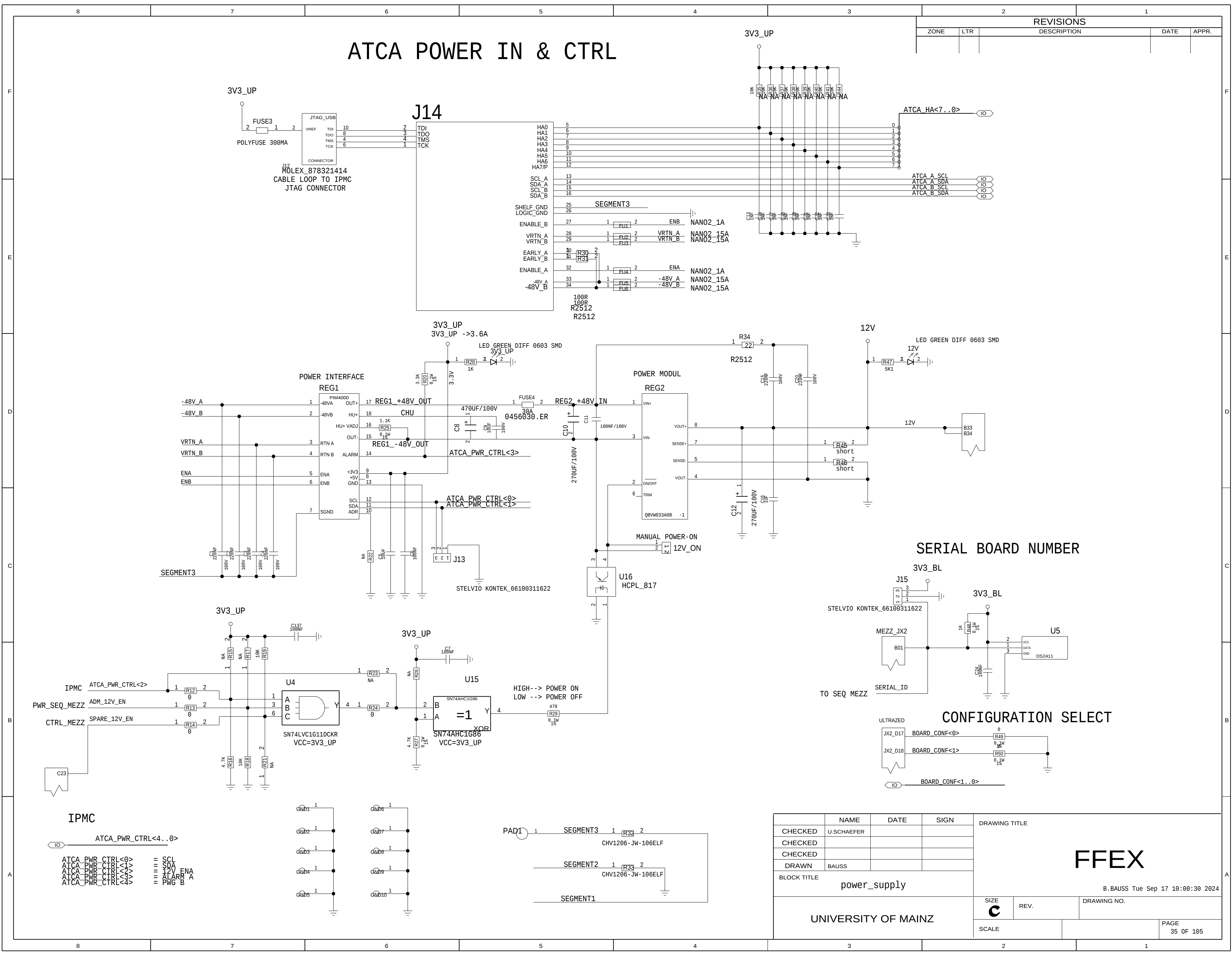
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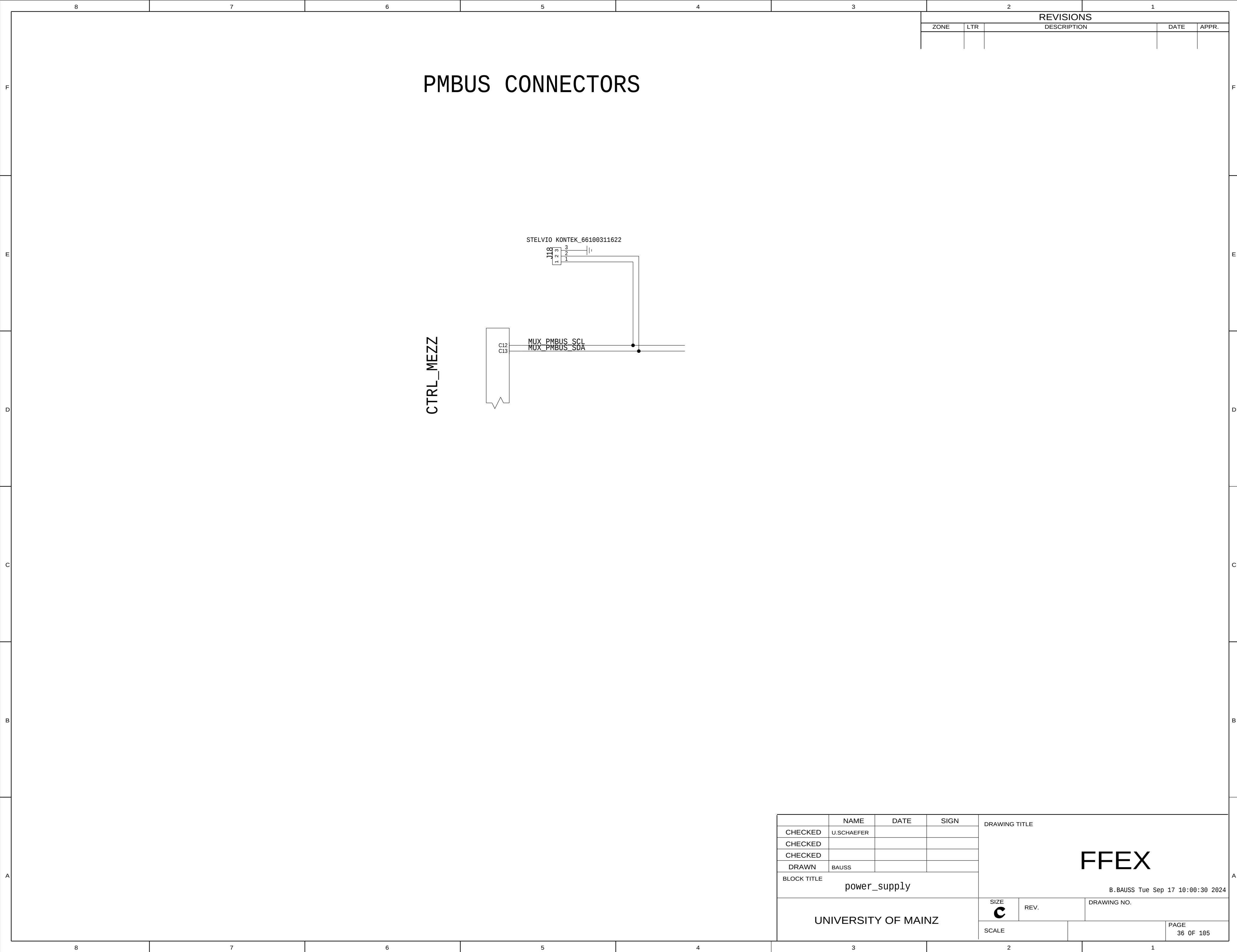
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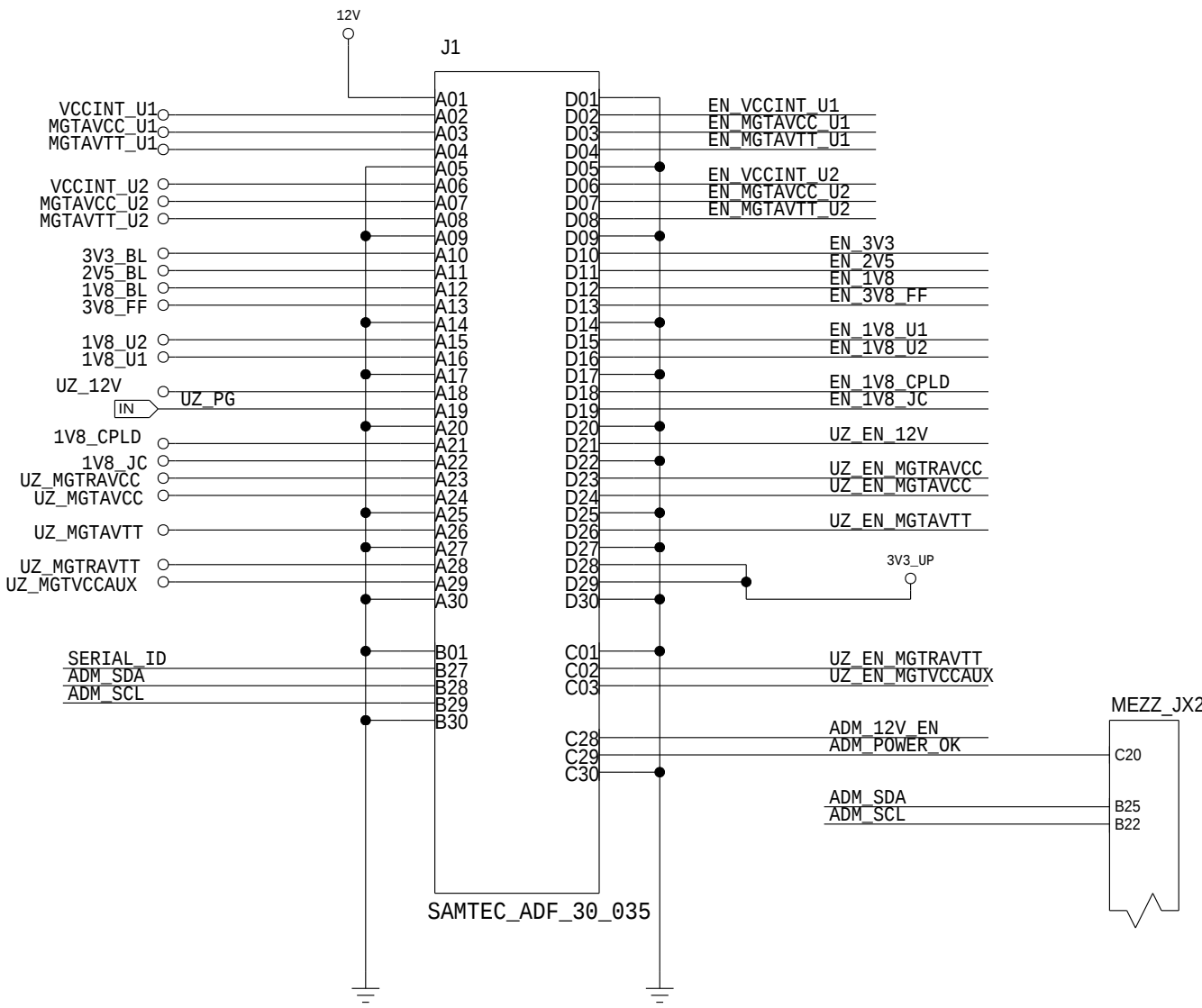
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POWER SEQUENCING MEZZ CONNECTOR

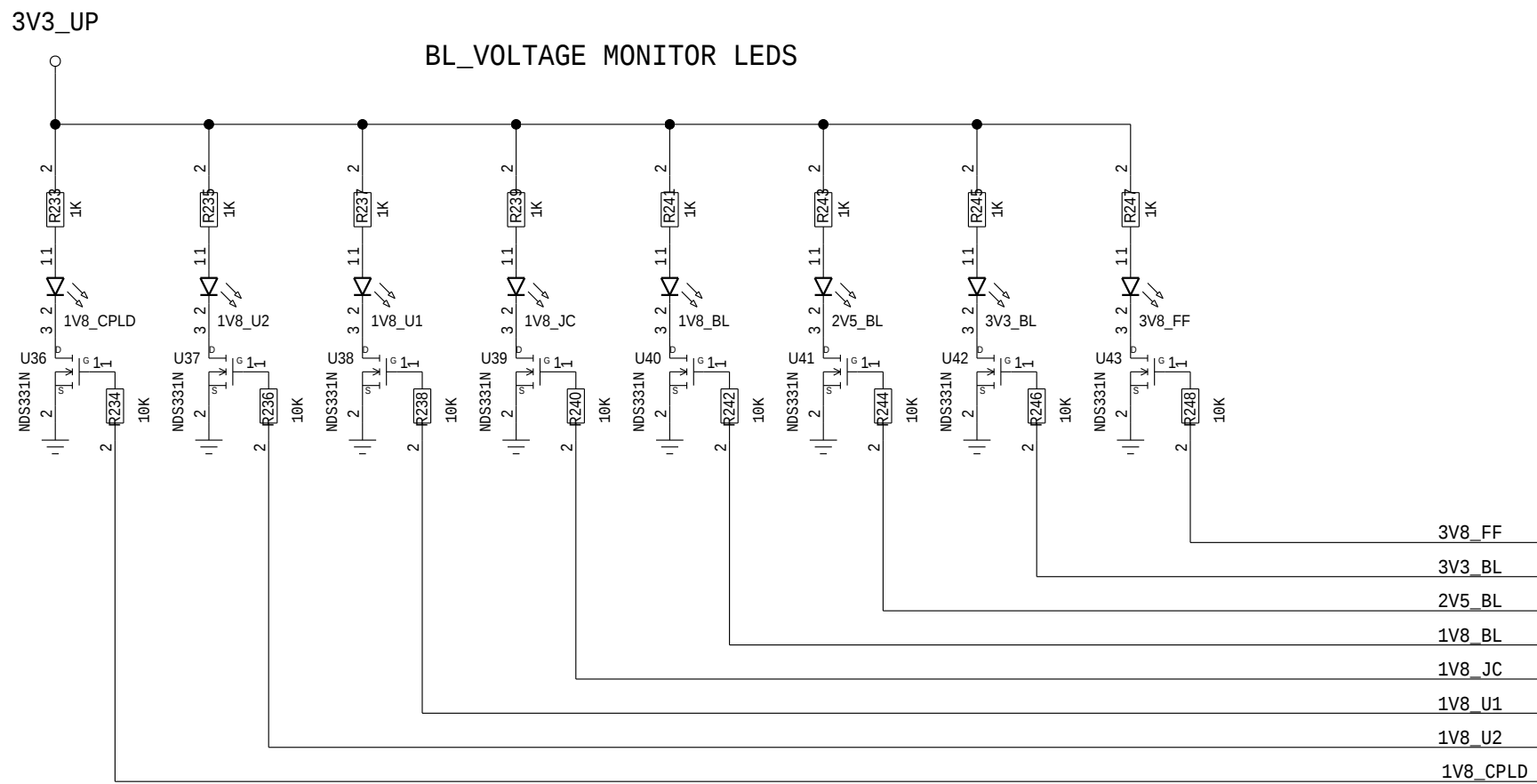
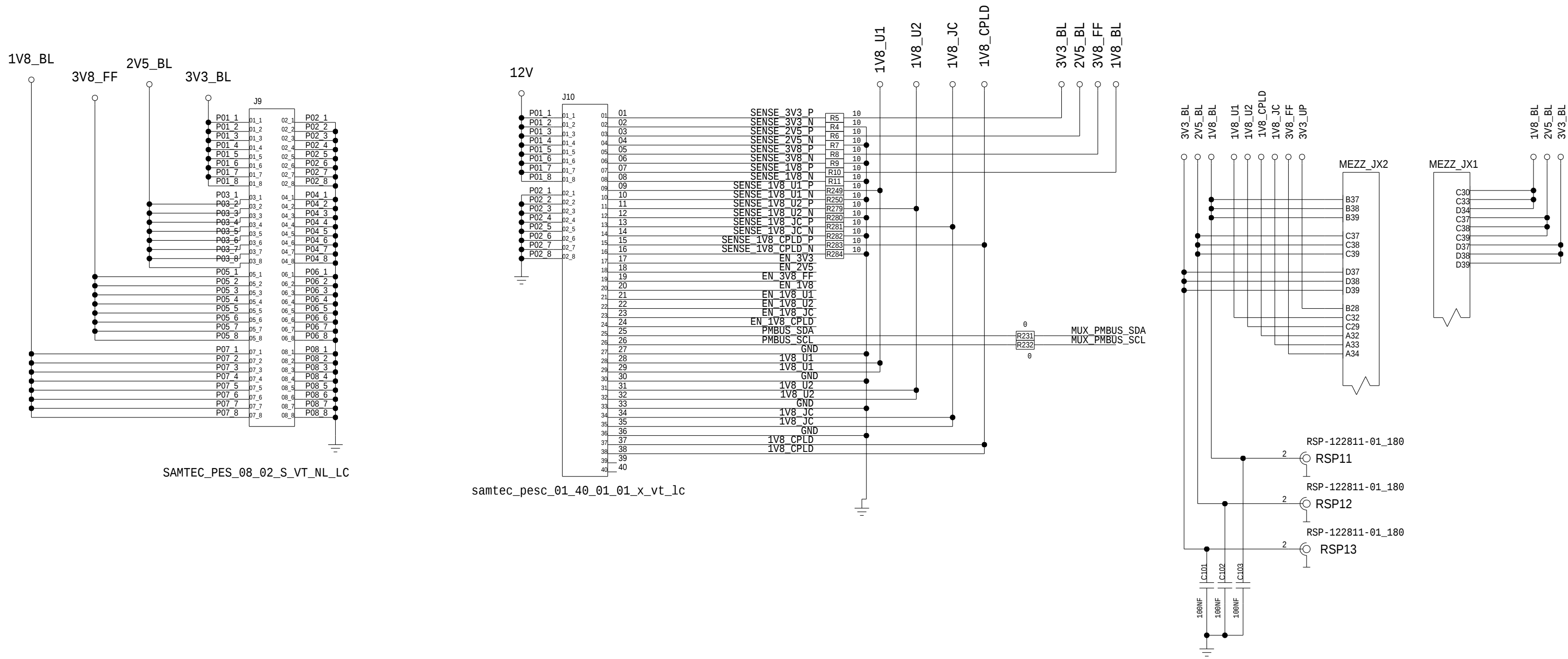


UPDATE EXCEL

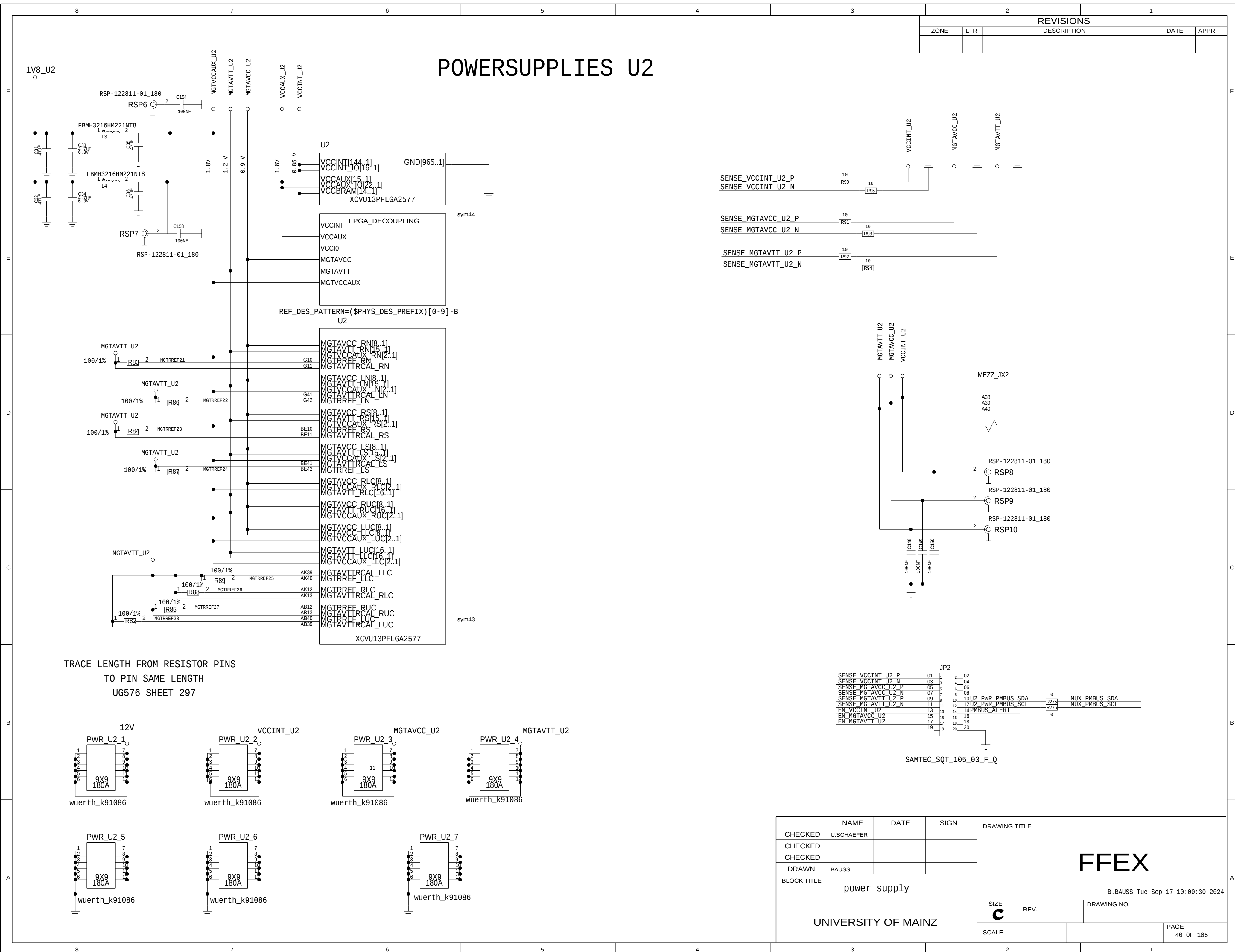
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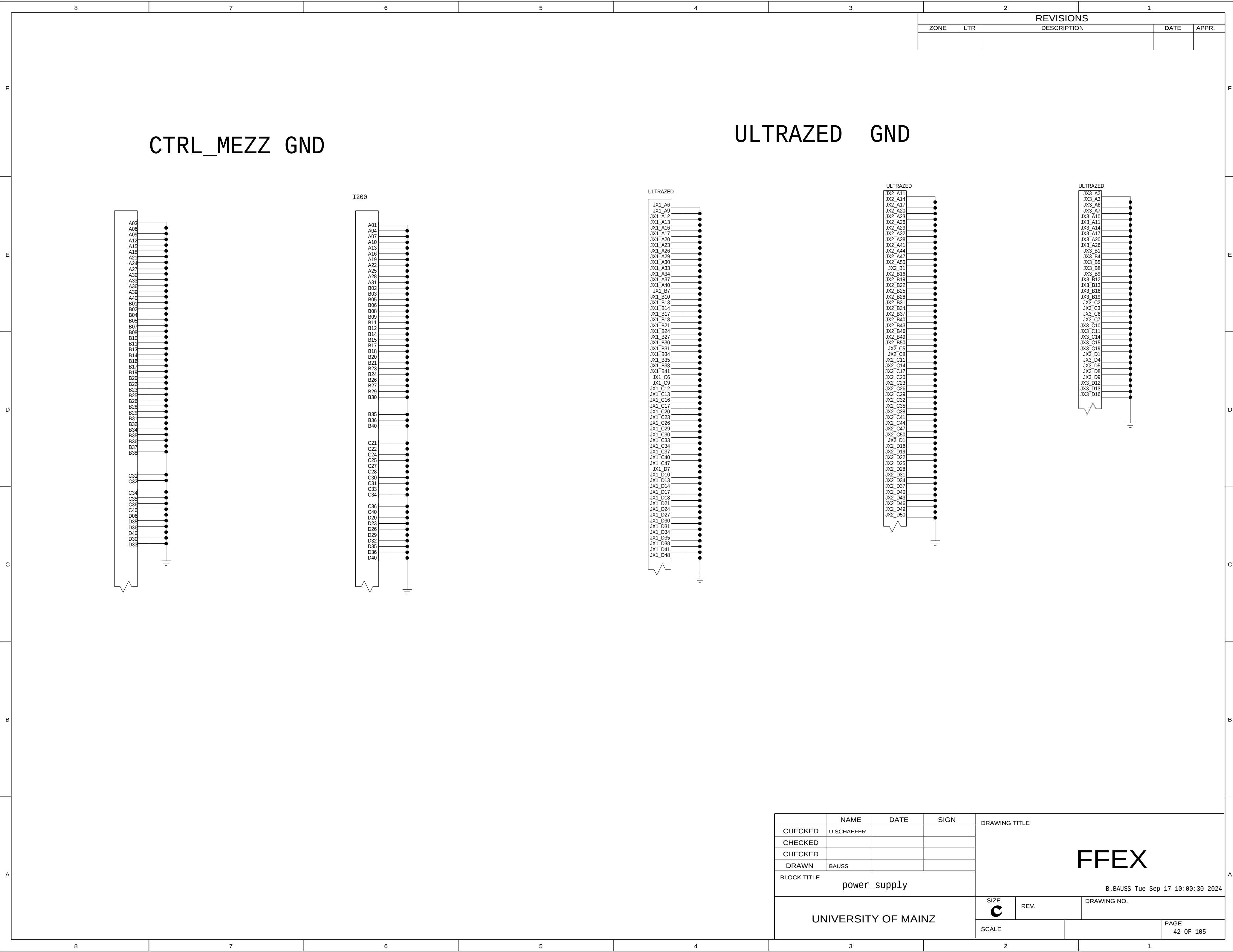
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1V8_CPLD, 1V8_JC



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VCCINT/VCC_IO/VCCBRAM

VCCAUX/VCCAUX_IO

FROM UG583

VCCINT

330U 5X

GRM32EC80E337ME05

FROM UG583

VCCAUX

47U 2X 10U 2X

VCCIO HPIO/HDIO

BANK65

BANK0

BANK71

MGT DECOUPLING

FROM UG578

MGTAVCC

4.7U X8

FROM UG578 1 PER GROUP

MGTAVTT

4.7U X8

FROM UG578 1 PER GROUP

MGTVCCAUX

4.7U X8

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VCCIO

C370F

C280F

VCCIO

C370F

C280F

MGTAVCC

C470F

C470F

C470F

C470F

C470F

C470F

C470F

MGTAVTT

C470F

C470F

C470F

C470F

C470F

C470F

C470F

MGTVCCAUX

C470F

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C470F

C470F

Package	Device	Package to Device Transceiver Mapping																								Unbonded GT Quads							
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X		Y	Z	AA	AB	AC	AD	AE
Power Supply Group		RLC 1		RUC 2				RN 3				RS 4				RLC		LLC 5		LUC 6				LN 7				LS 8				LLC	
FLGA2577	XCVU190	224	225	226	227	228	229	230	231	232	233		219	220	221	222	223	124	125	126	127	128	129	130	131	132	133		119	120	121	122	123
	XCVU9P	224	225	226	227	228	229	230	231	232	233		219	220	221	222	223	124	125	126	127	128	129	130	131	132	133		119	120	121	122	123
	XCVU11P	225	226	227	228	229	230	231	232	233	234	235						224	125	126	127	128	129	130	131	132	133	134	135				124
	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124
FSGA2577	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124
	XCVU27P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124
	XCVU29P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124

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FFEX

B.BAUSS Tue Sep 17 10:00:30 2024

SIZE

C

REV.

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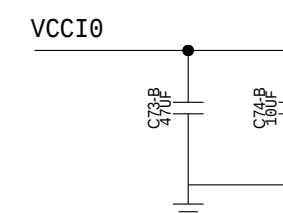
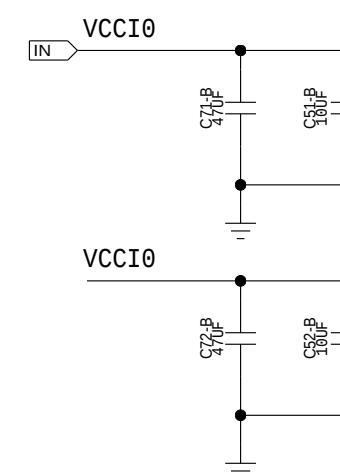
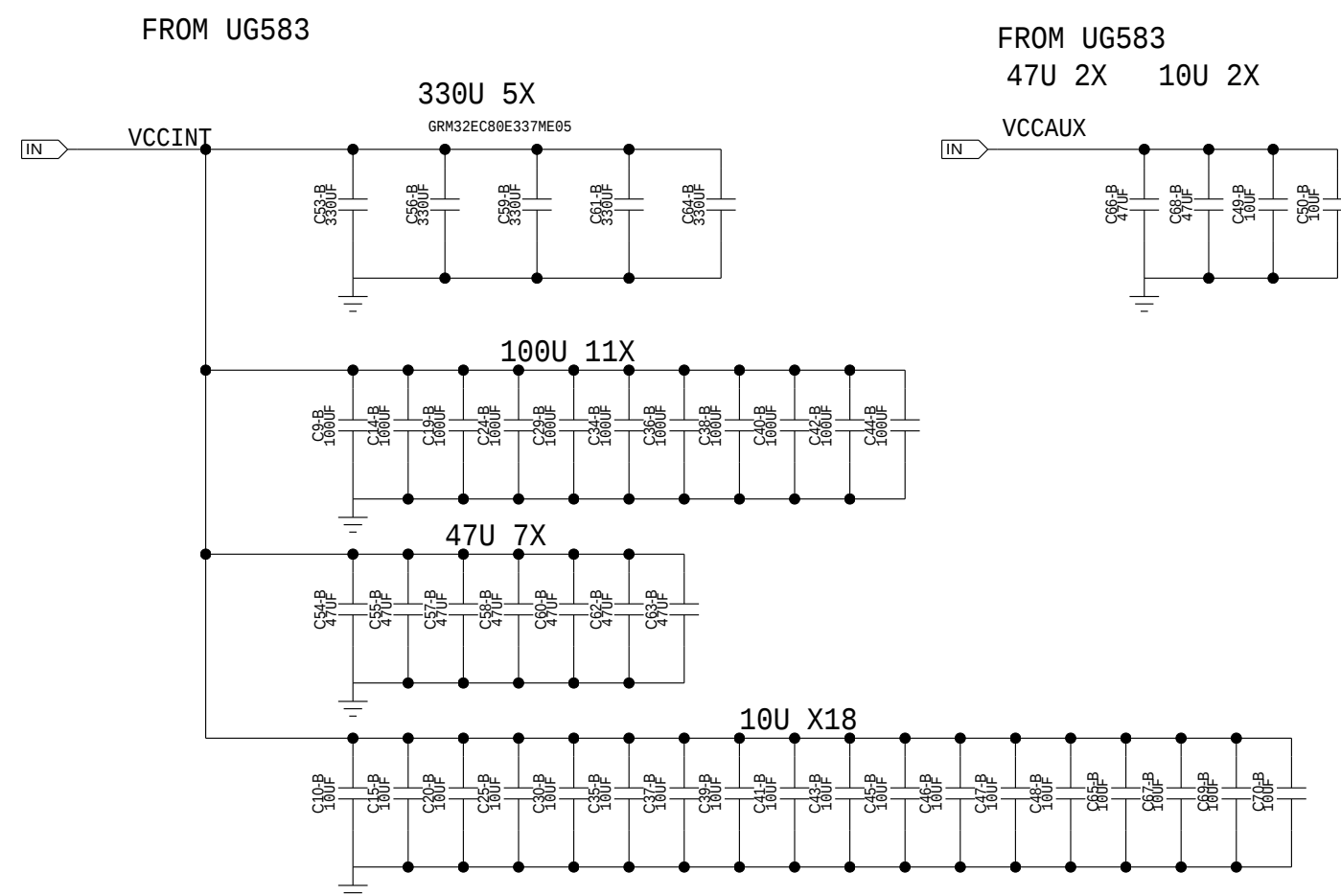
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VCCIO HPIO/HDIO

BANK65

BANK71



MGT DECOUPLING

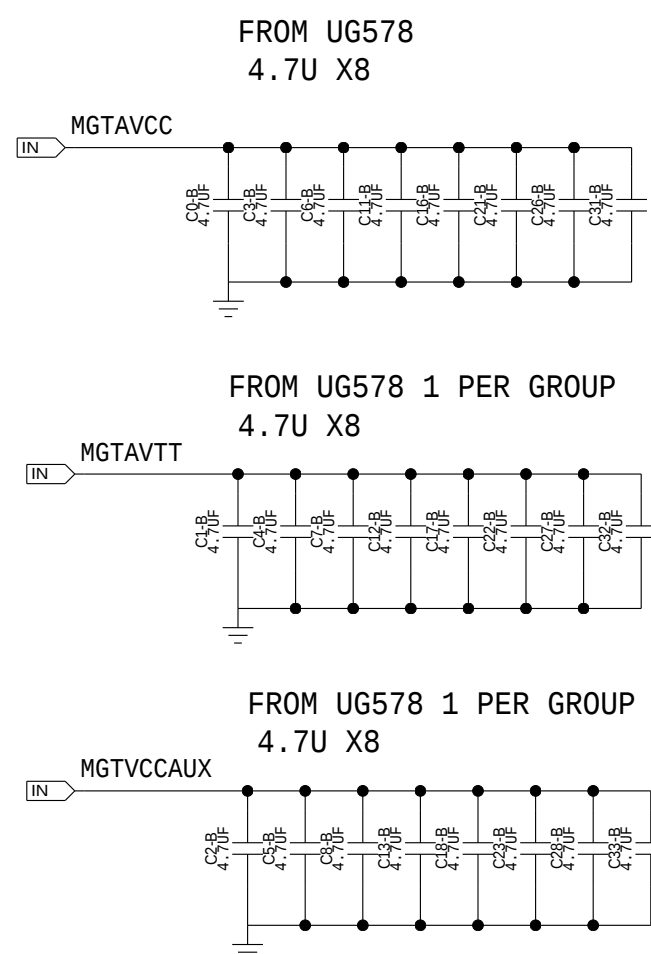


Table 1-9: Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray) (Cont'd)

Package	Device	Package to Device Transceiver Mapping																														Unbonded GT Quads							
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD		AE	AF					
Power Supply Group		R1C 1			RUC 2				RN 3				RS 4				R1C 5		LUC 6				LN 7				LS 8				LLC								
FLGA2577	XCVU190	224	225	226	227	228	229	230	231	232	233					219	220	221	222	223	124	125	126	127	128	129	130	131	132	133					119	120	121	122	123
	XCVU9P	224	225	226	227	228	229	230	231	232	233					219	220	221	222	223	124	125	126	127	128	129	130	131	132	133					119	120	121	122	123
	XCVU11P	225	226	227	228	229	230	231	232	233	234	235									224	125	126	127	128	129	130	131	132	133	134	135					124		
	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124						
F5GA2577	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124						
	XCVU27P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124						
	XCVU29P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124						

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				SCALE						

HIGH SPEED OPTICAL LINKS

220, 221, 222

MGT P/N SWAP ALLOWED

224, 225, 226

MGT P/N SWAP ALLOWED

RX5_U2

RX6_U2

HSDP 223

TX2_U2

FFEX

UNIVERSITY OF MAINZ

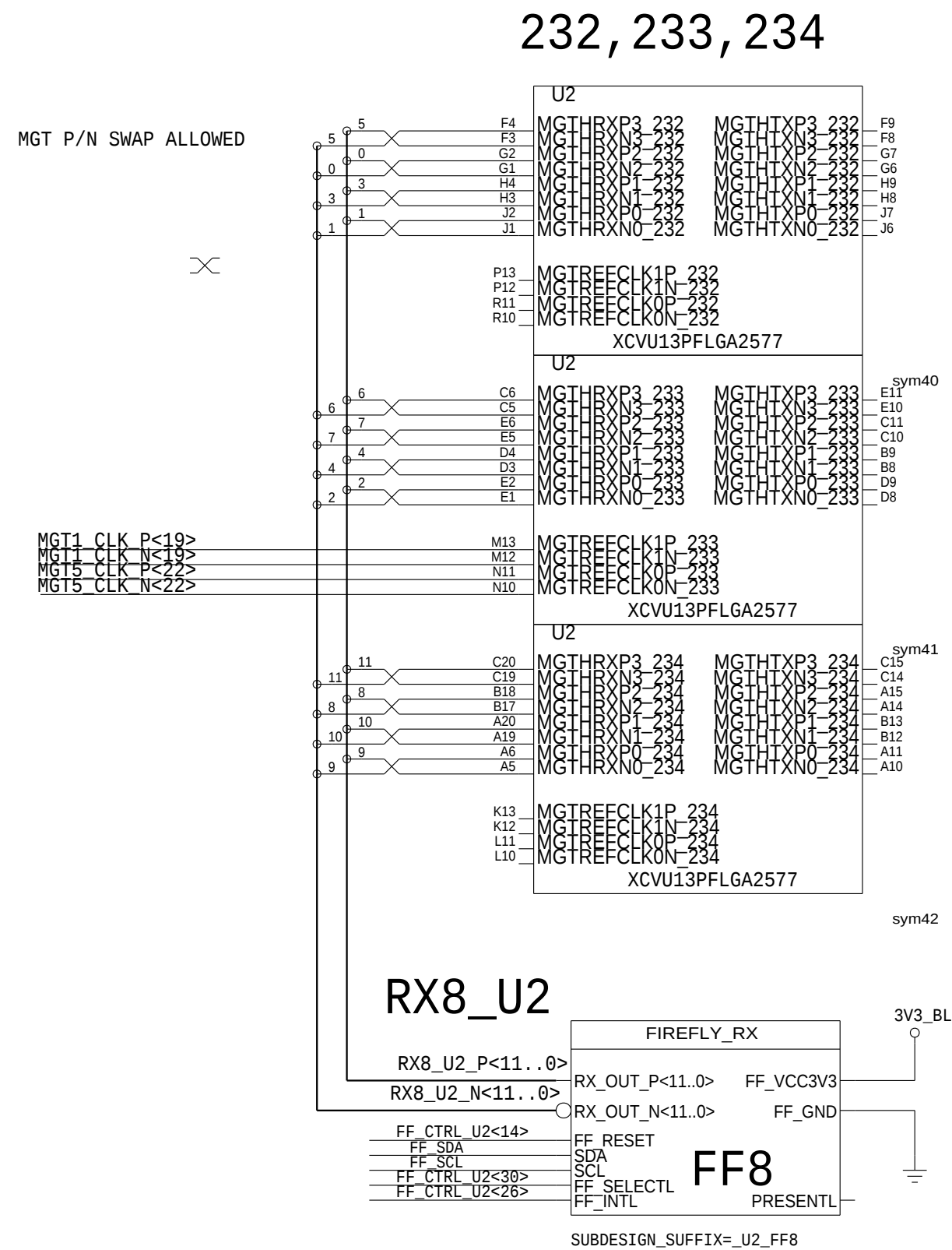
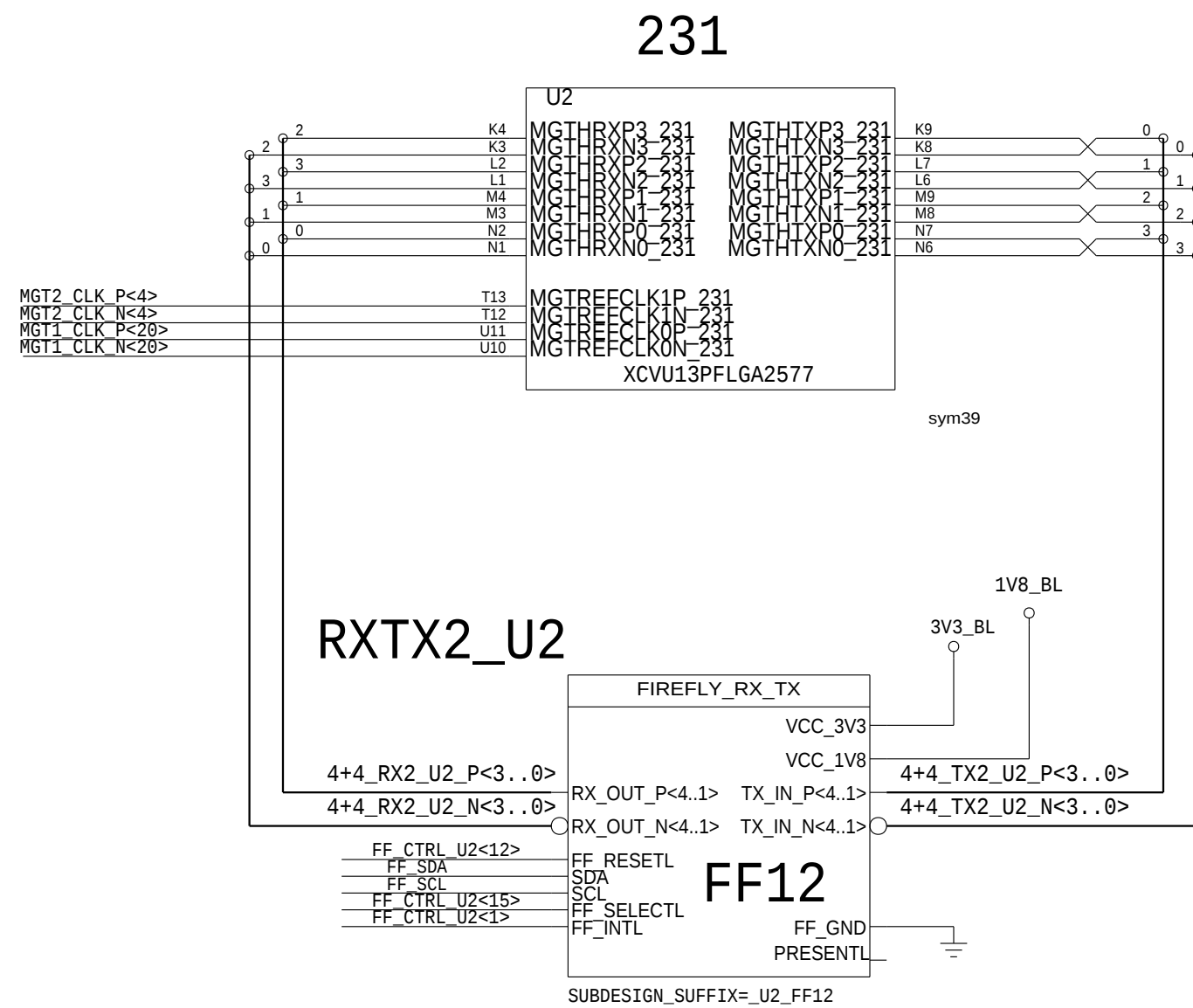
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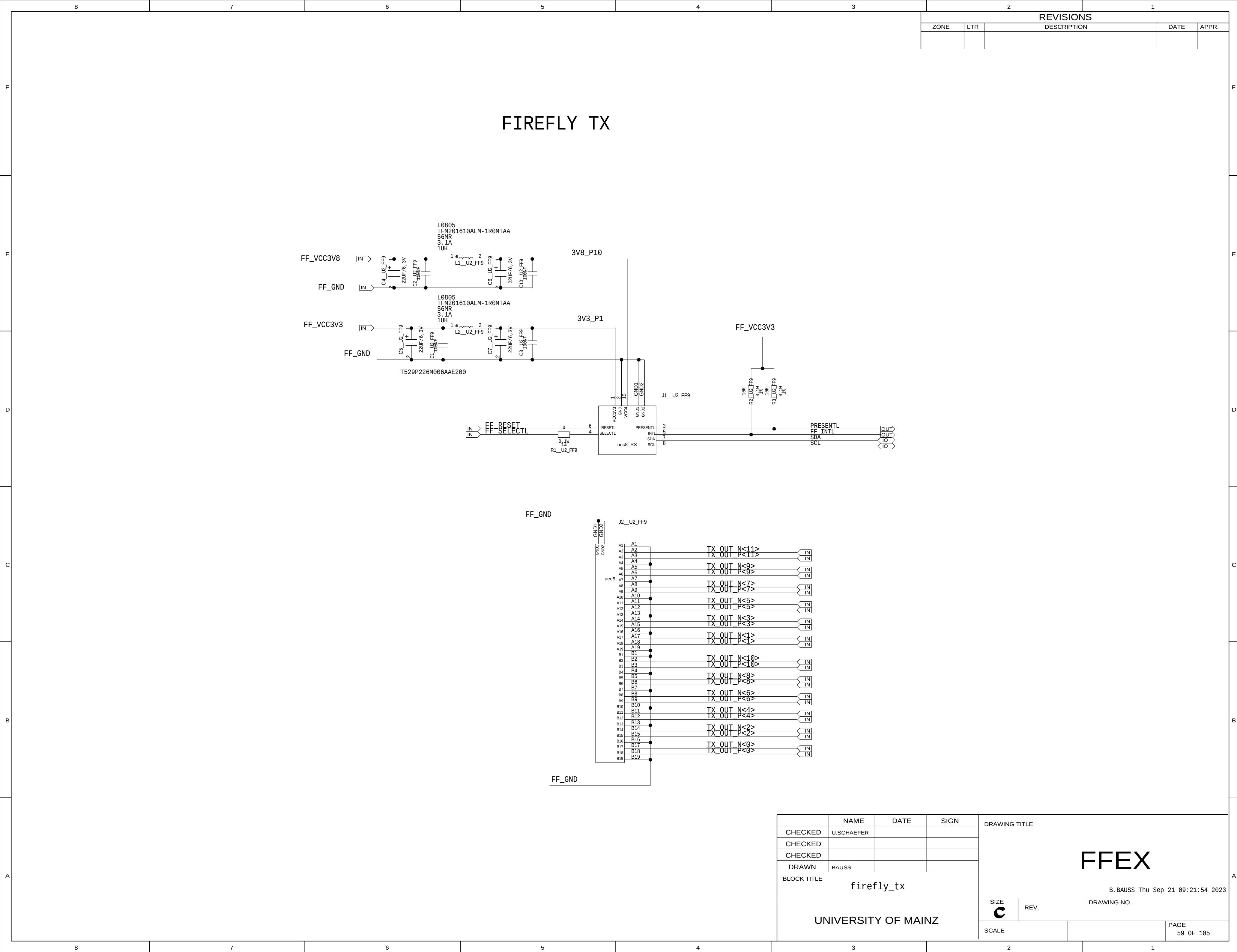
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HIGH SPEED OPTICAL LINKS

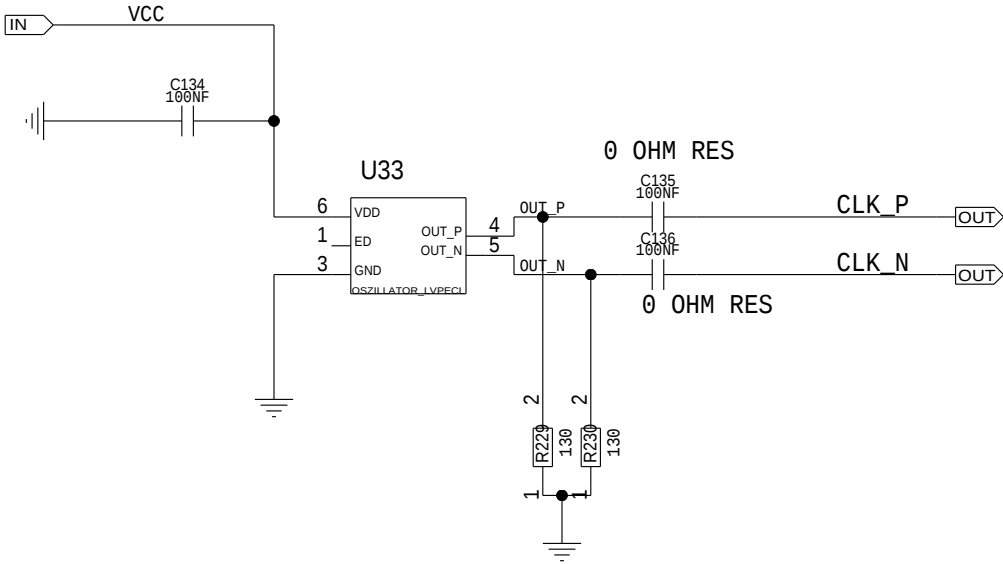


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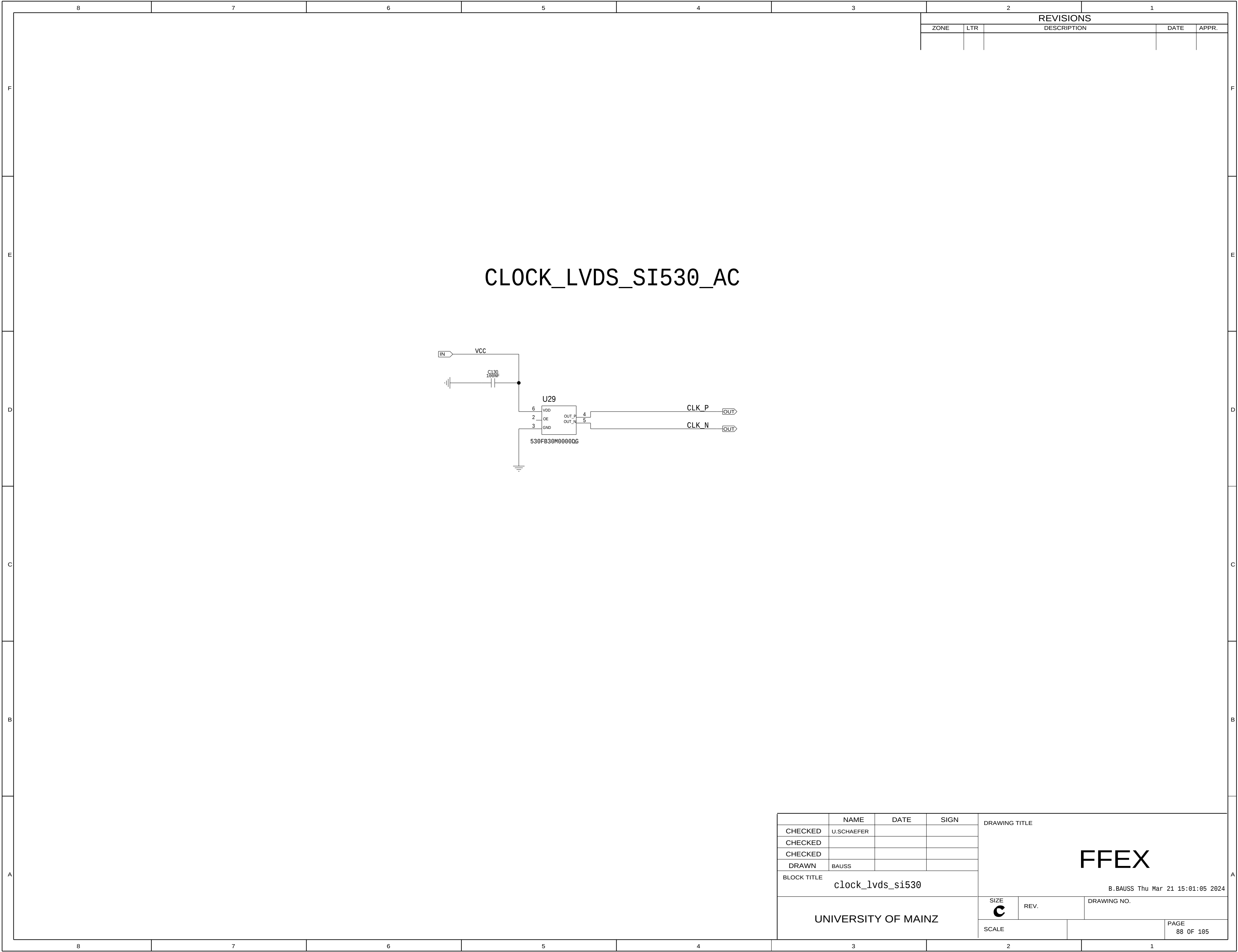


FIREFLY TX

CLOCK_LVPECL_SI591_AC



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clock_lvpecl_si591_ac						
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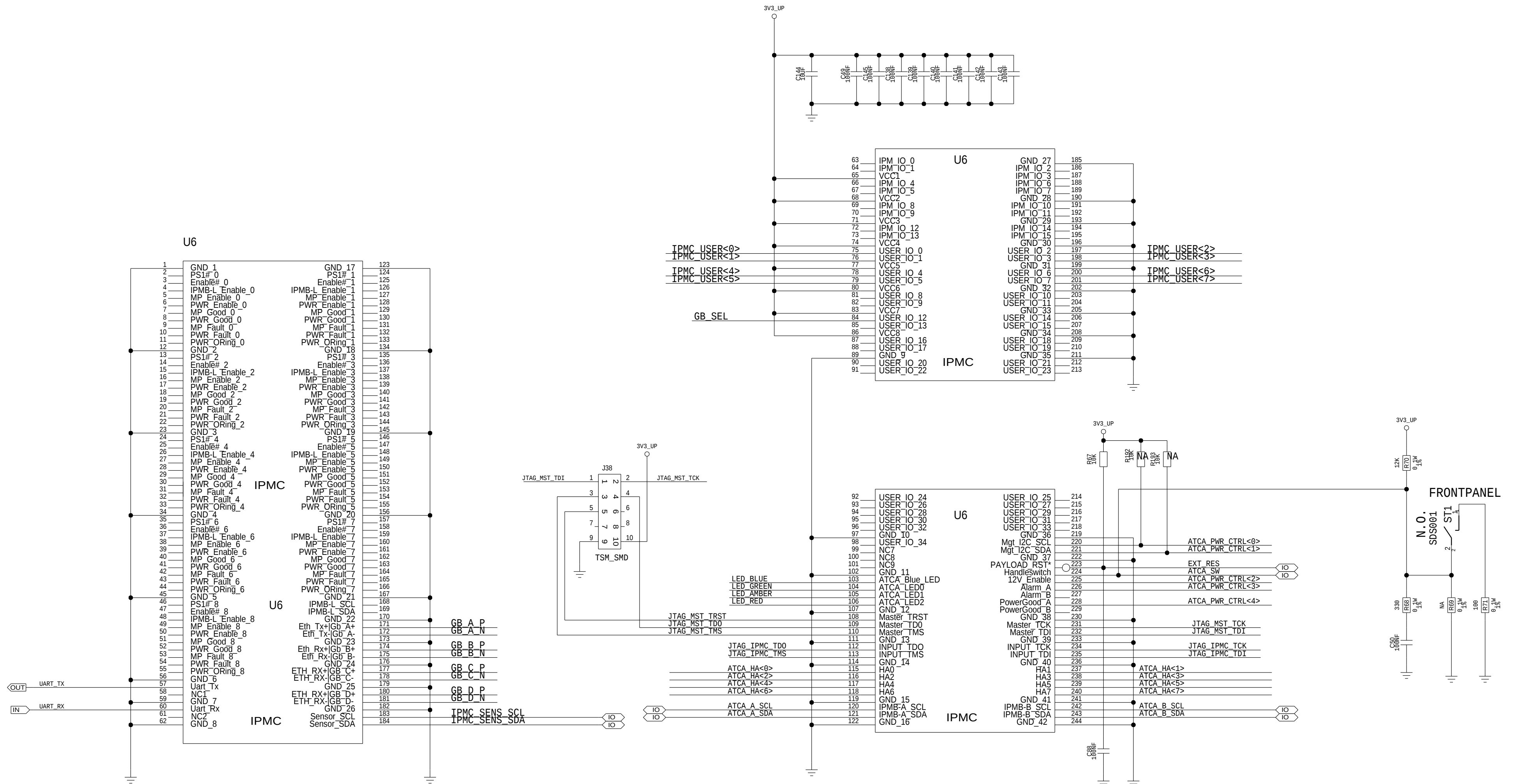
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IPMC CONNECTOR

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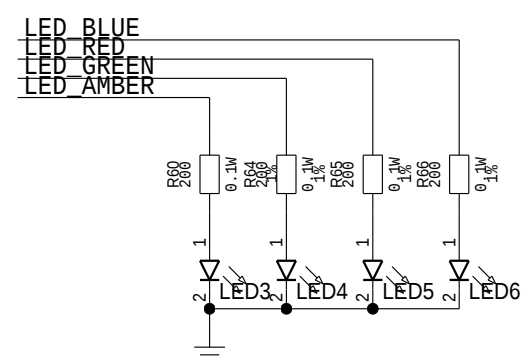
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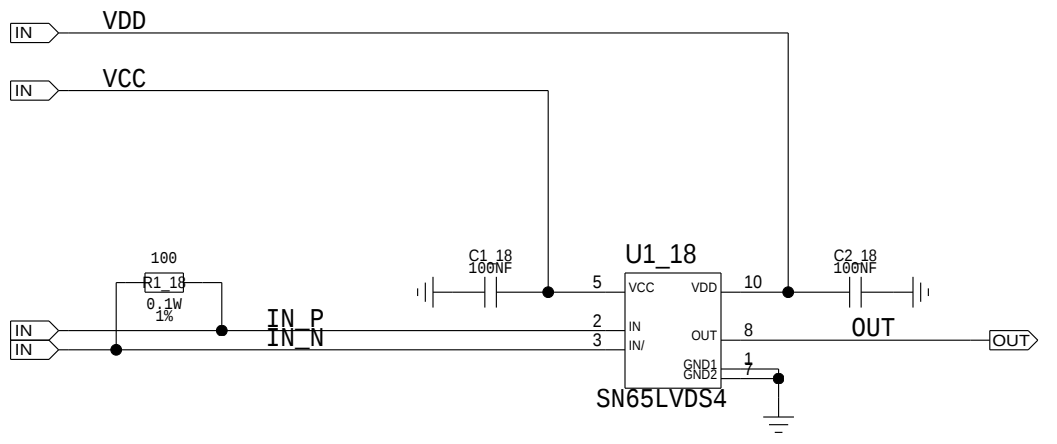
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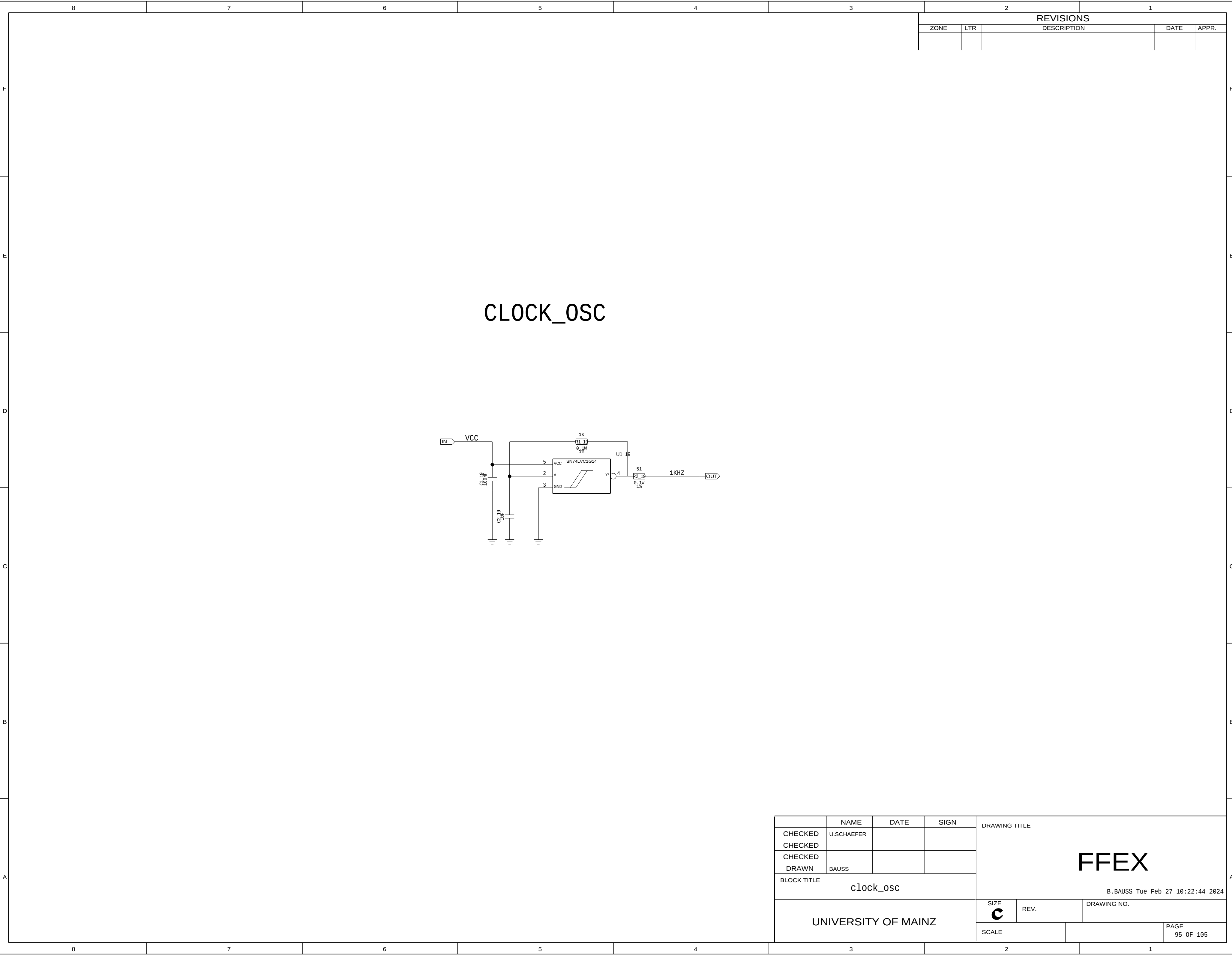


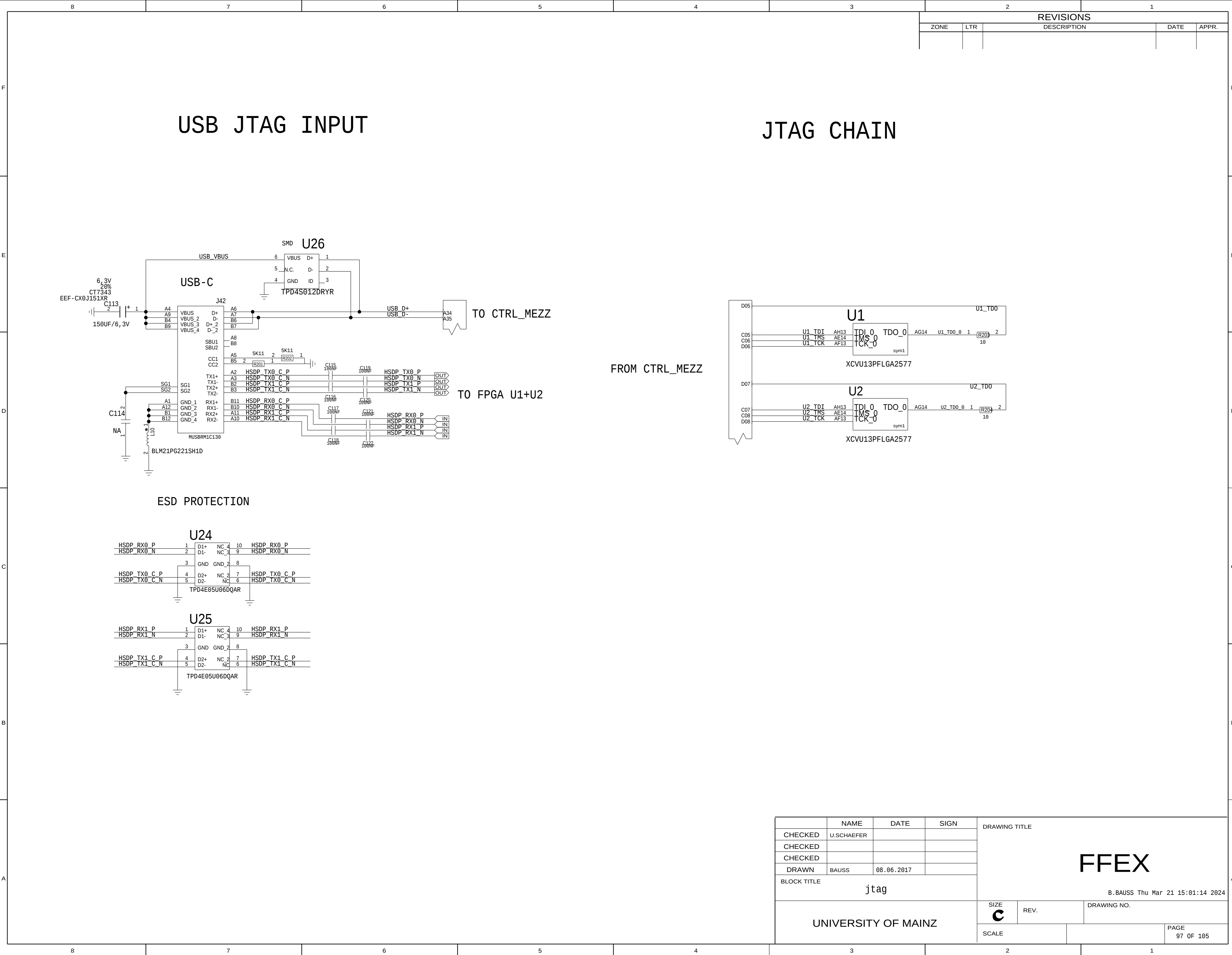
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				SCALE			PAGE 91 OF 105

CLOCK_LVDS_LVCMOS



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USB JTAG INPUT

JTAG CHAIN

REVISIONS

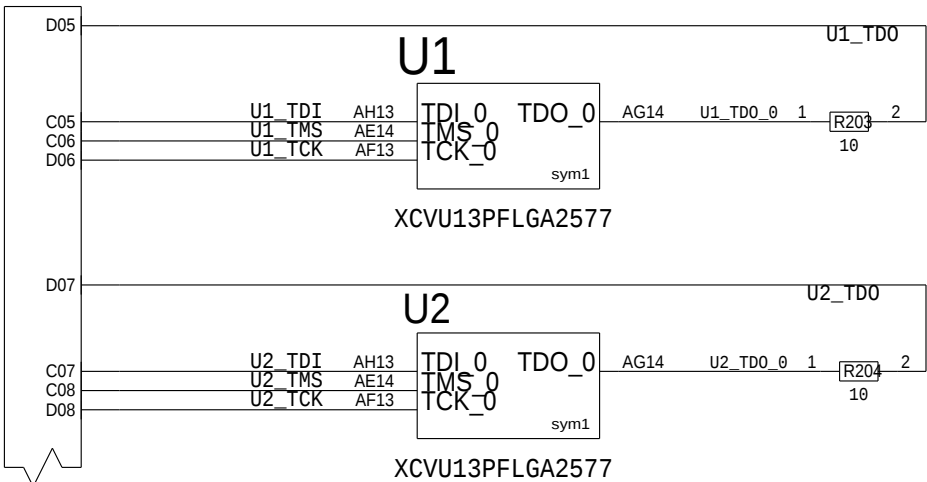
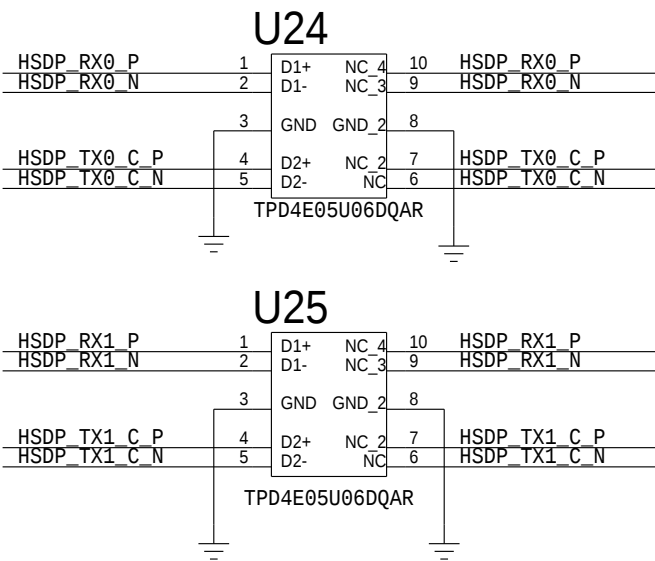
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FROM CTRL_MEZZ

TO CTRL_MEZZ

TO FPGA U1+U2

ESD PROTECTION

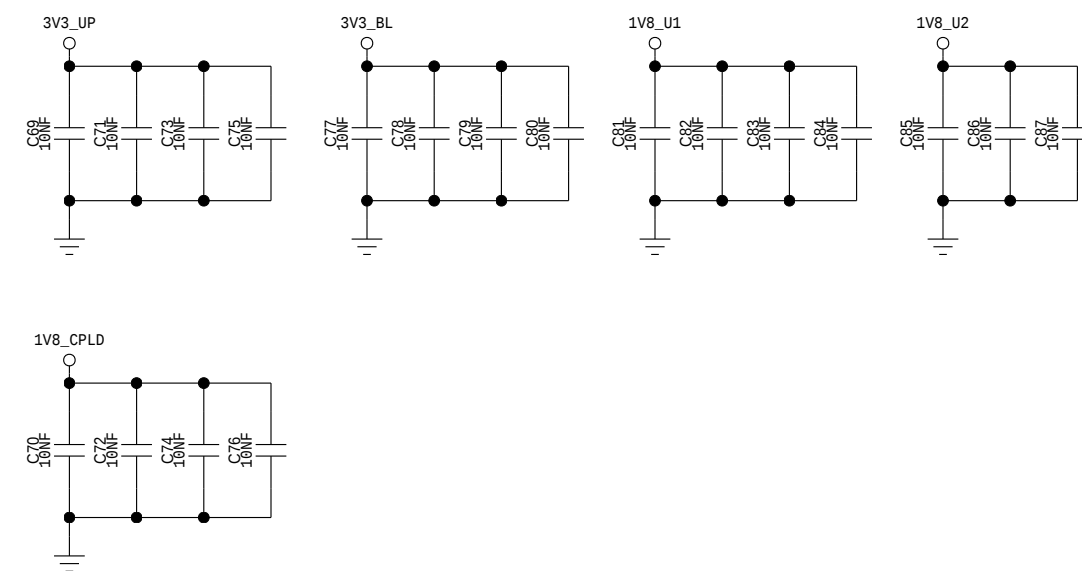
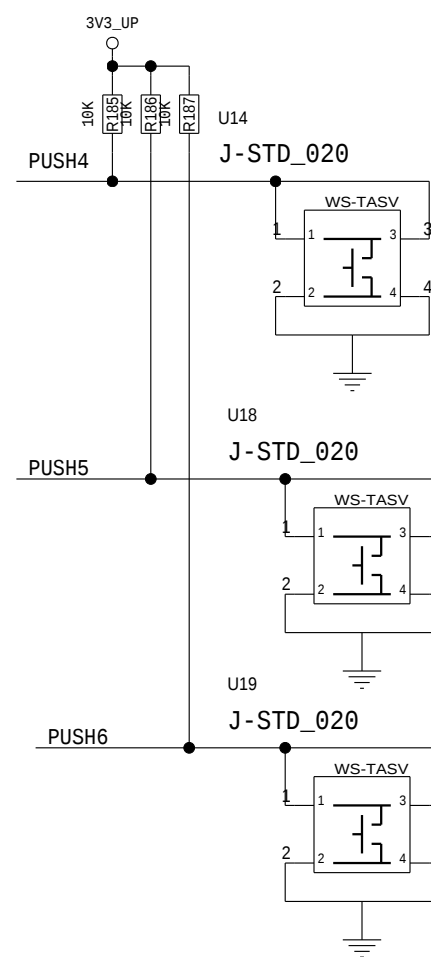
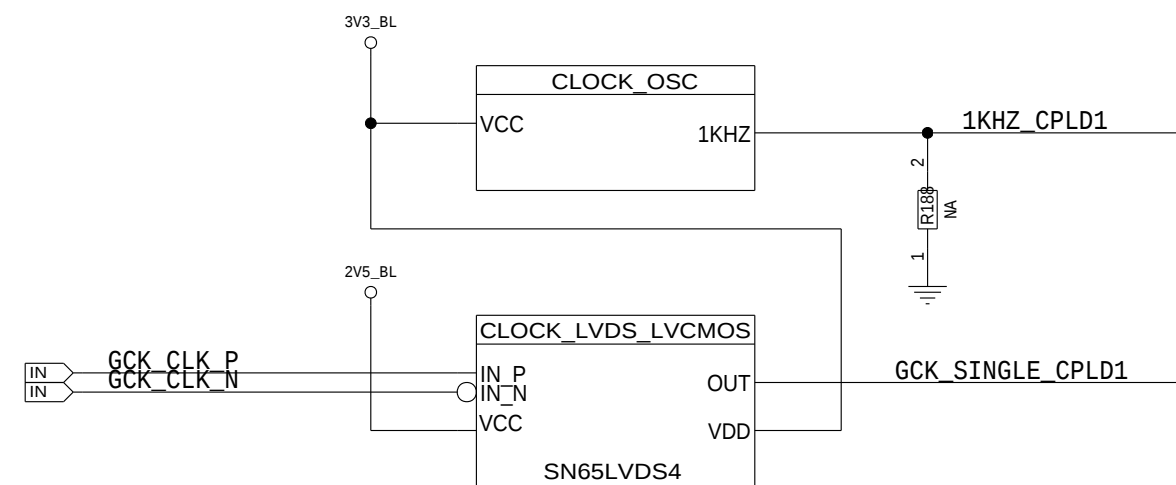


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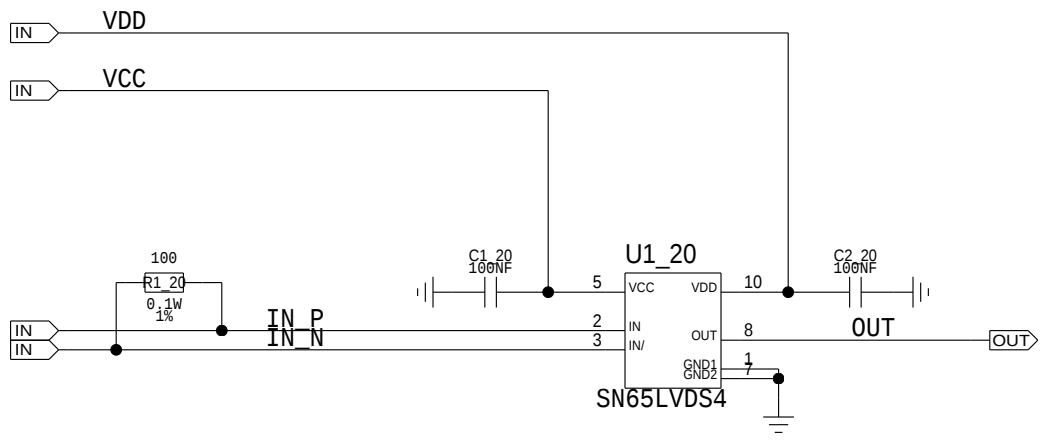
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CLOCK_LVDS_LVCMOS



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