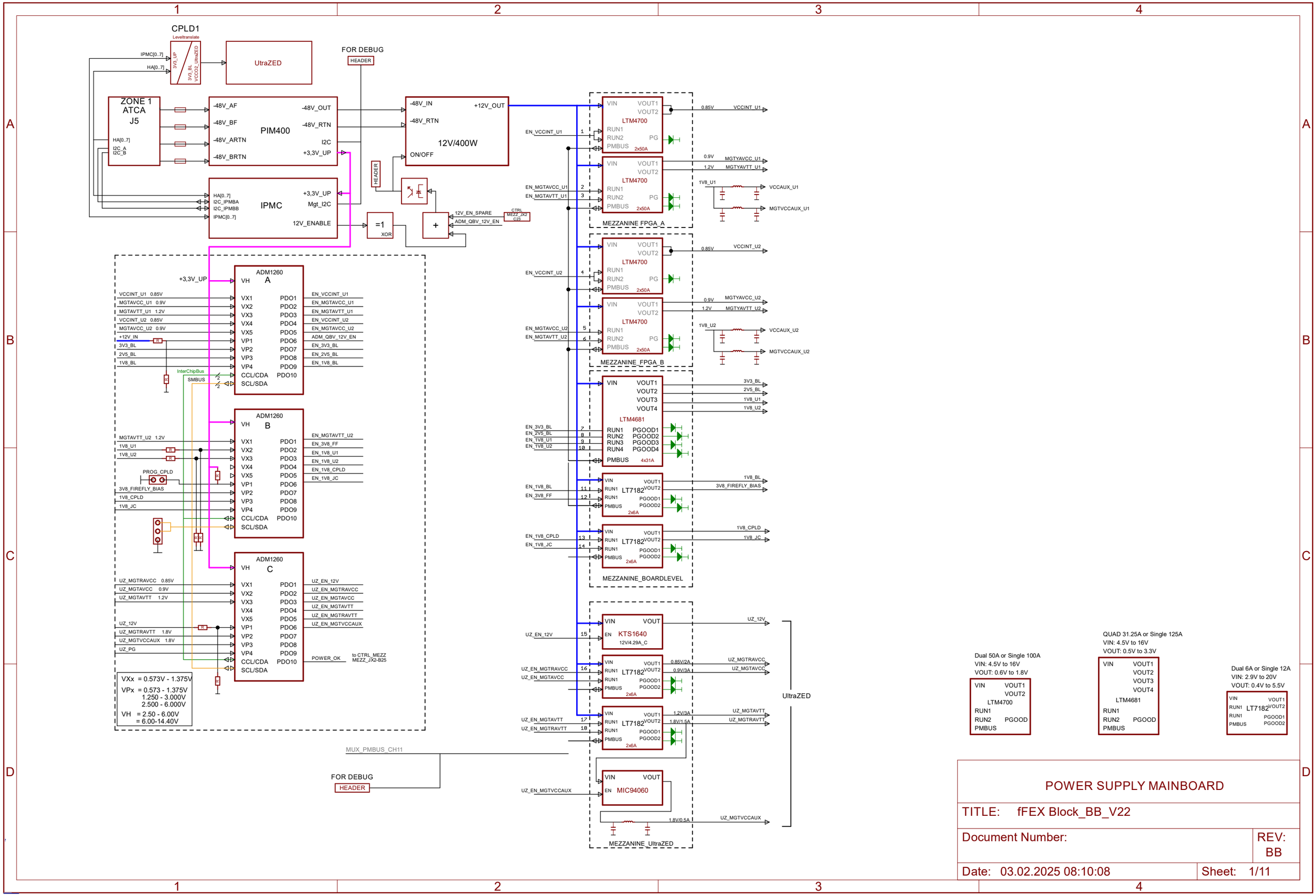

POWER SUPPLY MAINBOARD

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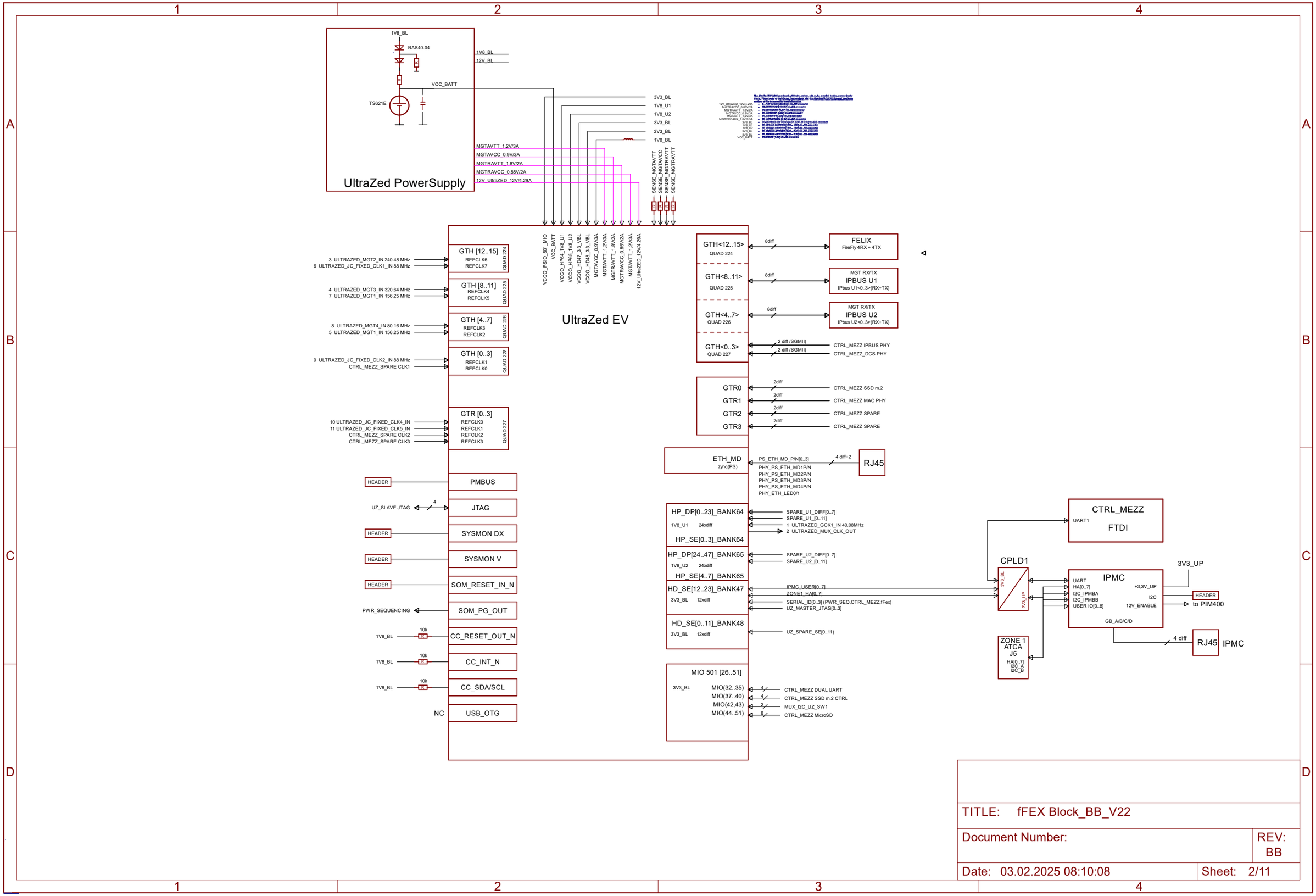

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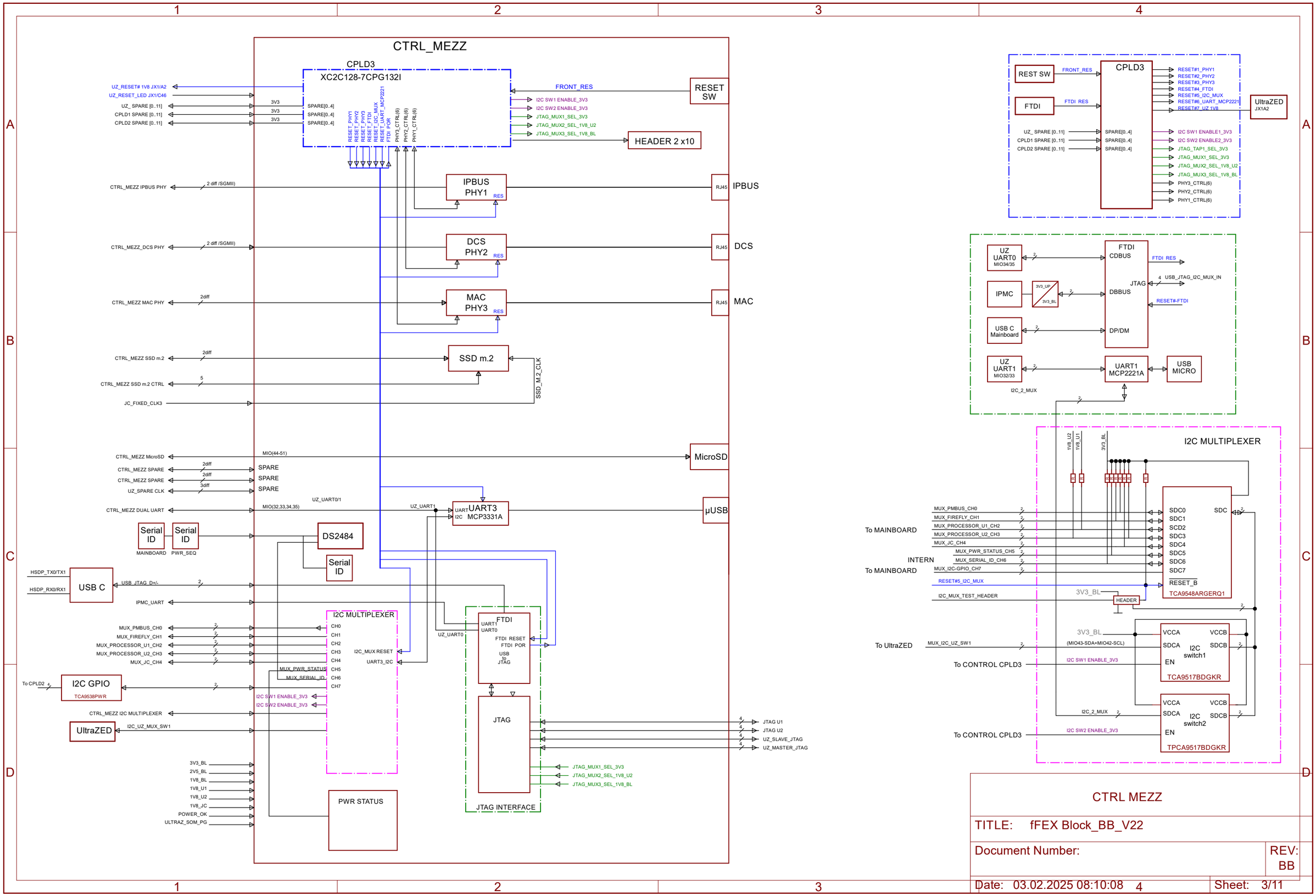
CTRL_MEZZ
CPLD3
XC2C128-7CPG132I
UZ_RESET# 1V8 JX1/A2
UZ_RESET_LED JX1/C46
UZ_ SPARE [0..11]
CPLD1 SPARE [0..11]
CPLD2 SPARE [0..11]
3V3
SPARE[0..4]
RESET_PHY1
RESET_PHY2
RESET_PHY3
RESET_FTDI
RESET_I2C_MUX
RESET_UART_MCP2221
FTDI_POR
PHY3_CTRL(6)
PHY2_CTRL(6)
PHY1_CTRL(6)
FRONT_RES
RESET SW
I2C SW1 ENABLE_3V3
I2C SW2 ENABLE_3V3
JTAG_MUX1_SEL_3V3
JTAG_MUX2_SEL_1V8_U2
JTAG_MUX3_SEL_1V8_BL
HEADER 2 x10
CTRL_MEZZ IPBUS PHY
2 diff /SGMII)
IPBUS PHY1
RES
RJ45
IPBUS
CTRL_MEZZ_DCS PHY
DCS PHY2
DCS
CTRL_MEZZ MAC PHY
2diff
MAC PHY3
MAC
CTRL_MEZZ SSD m.2
SSD m.2
SSD_M.2_CLK
CTRL_MEZZ SSD m.2 CTRL
5
JC_FIXED_CLK3
CTRL_MEZZ MicroSD
MIO(44-51)
MicroSD
CTRL_MEZZ SPARE
SPARE
UZ_SPARE CLK
3diff
UZ_UART0/1
CTRL_MEZZ DUAL UART
MIO(32,33,34,35)
UZ_UART1
UART3
MCP3331A
µUSB
Serial ID
MAINBOARD
PWR_SEQ
DS2484
HSDP_TX0/TX1
HSDP_RX0/RX1
USB C
USB_JTAG_D+/-
IPMC_UART
I2C MULTIPLEXER
MUX_PMBUS_CH0
MUX_FIREFLY_CH1
MUX_PROCESSOR_U1_CH2
MUX_PROCESSOR_U2_CH3
MUX_JC_CH4
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
I2C_MUX RESET
UART3_I2C
MUX_PWR_STATUS
MUX_SERIAL_ID
To CPLD2
I2C GPIO
TCA9538PWR
CTRL_MEZZ I2C MULTIPLEXER
UltraZED
I2C_UZ_MUX_SW1
FTDI
UART1
UART0
FTDI RESET
FTDI POR
USB to JTAG
UZ_UART0
JTAG
JTAG U1
JTAG U2
UZ_SLAVE_JTAG
UZ_MASTER_JTAG
JTAG_MUX1_SEL_3V3
JTAG_MUX2_SEL_1V8_U2
JTAG_MUX3_SEL_1V8_BL
JTAG INTERFACE
3V3_BL
2V5_BL
1V8_BL
1V8_U1
1V8_U2
1V8_JC
POWER_OK
ULTRAZ_SOM_PG
PWR STATUS
REST SW
FRONT_RES
FTDI
FTDI_RES
RESET#1_PHY1
RESET#2_PHY2
RESET#3_PHY3
RESET#4_FTDI
RESET#5_I2C_MUX
RESET#6_UART_MCP2221
RESET#7_UZ 1V8
UltraZED
JX1A2
I2C SW1 ENABLE1_3V3
I2C SW2 ENABLE2_3V3
JTAG_TAP1_SEL_3V3
JTAG_MUX1_SEL_3V3
JTAG_MUX2_SEL_1V8_U2
JTAG_MUX3_SEL_1V8_BL
PHY3_CTRL(6)
PHY2_CTRL(6)
PHY1_CTRL(6)
UZ UART0
MIO34/35
IPMC
3V3_UP
3V3_BL
USB C Mainboard
UZ UART1
MIO32/33
I2C_2_MUX
FTDI CDBUS
JTAG
DBBUS
DP/DM
FTDI_RES
USB_JTAG_I2C_MUX_IN
RESET#-FTDI
UART1 MCP2221A
USB MICRO
I2C MULTIPLEXER
1V8_U2
1V8_U1
3V3_BL
To MAINBOARD
INTERN
To MAINBOARD
MUX_PMBUS_CH0
MUX_FIREFLY_CH1
MUX_PROCESSOR_U1_CH2
MUX_PROCESSOR_U2_CH3
MUX_JC_CH4
MUX_PWR_STATUS_CH5
MUX_SERIAL_ID_CH6
MUX_I2C-GPIO_CH7
RESET#5_I2C_MUX
I2C_MUX_TEST_HEADER
HEADER
SDC0
SDC1
SCD2
SDC3
SDC4
SDC5
SDC6
SDC7
SDC
RESET_B
TCA9548ARGERQ1
To UltraZED
MUX_I2C_UZ_SW1
To CONTROL CPLD3
I2C SW1 ENABLE_3V3
VCCA
VCCB
SDCA
SDCB
EN
I2C switch1
TCA9517BDGKR
I2C_2_MUX
To CONTROL CPLD3
I2C SW2 ENABLE_3V3
I2C switch2
TPCA9517BDGKR
CTRL MEZZ
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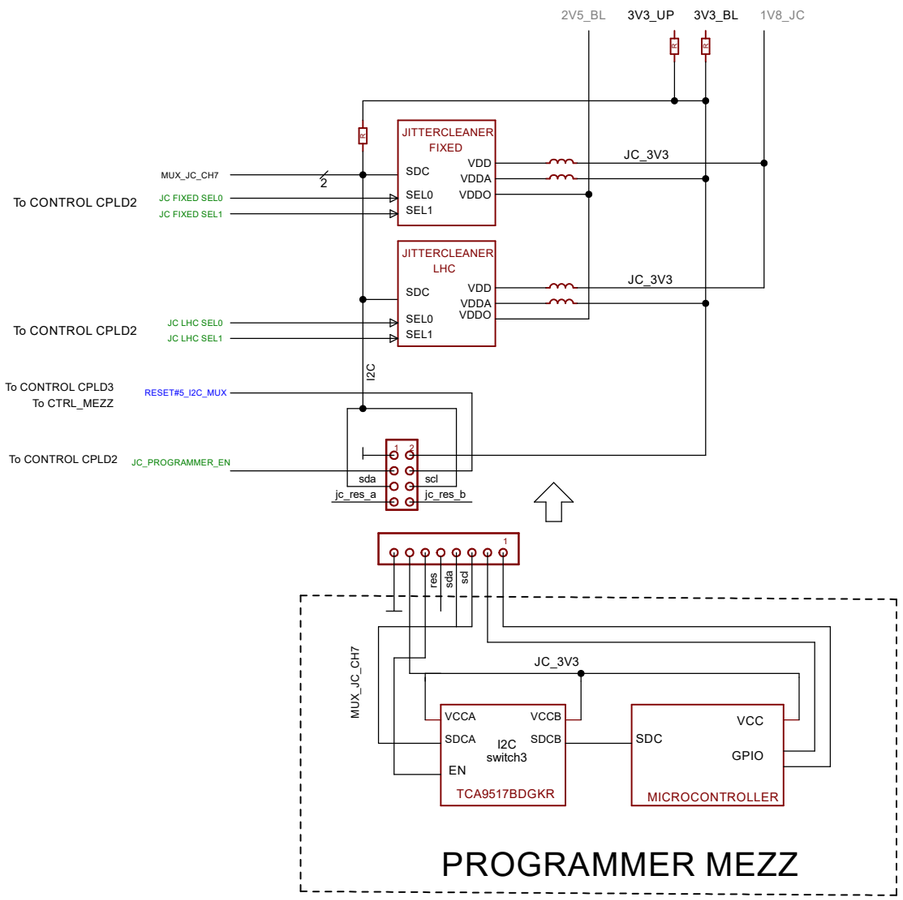
JITTER CLEANER I2C



Jitter Cleaner

TITLE: fFEX Block_BB_V22

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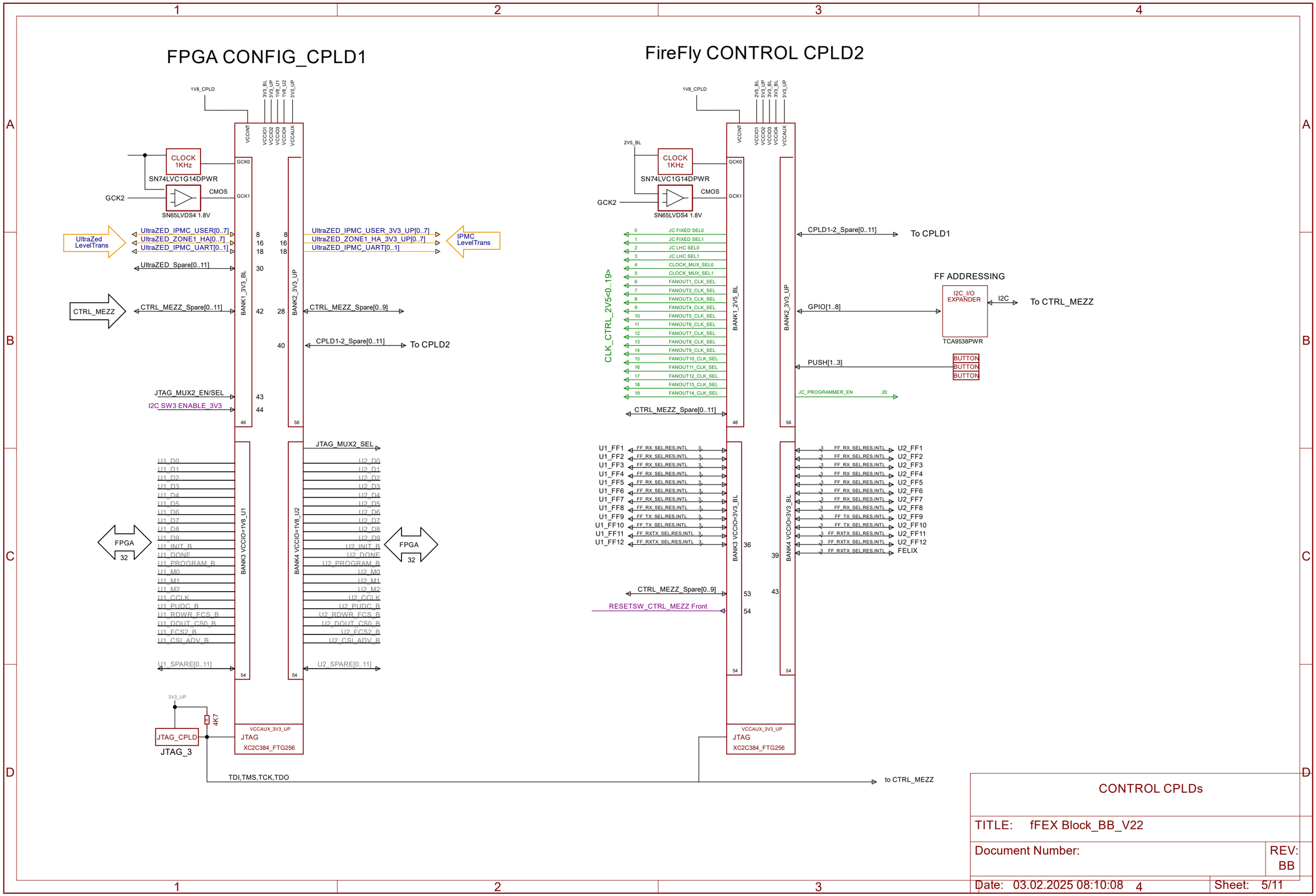
FPGA CONFIG_CPLD1
FireFly CONTROL CPLD2
1V8_CPLD
CLOCK 1KHz
SN74LVC1G14DPWR
CMOS
GCK2
SN65LVDS4 1.8V
UltraZed LevelTrans
UltraZED_IPMC_USER[0..7]
UltraZED_ZONE1_HA[0..7]
UltraZED_IPMC_UART[0..1]
UltraZED_Spare[0..11]
UltraZED_IPMC_USER_3V3_UP[0..7]
UltraZED_ZONE1_HA_3V3_UP[0..7]
UltraZED_IPMC_UART[0..1]
IPMC LevelTrans
CTRL_MEZZ
CTRL_MEZZ_Spare[0..11]
CTRL_MEZZ_Spare[0..9]
CPLD1-2_Spare[0..11]
To CPLD2
JTAG_MUX2_EN/SEL
I2C_SW3 ENABLE_3V3
JTAG_MUX2_SEL
BANK1_3V3_BL
BANK2_3V3_UP
BANK3 VCCIO=1V8_U1
BANK4 VCCIO=1V8_U2
FPGA 32
U1_SPARE[0..11]
U2_SPARE[0..11]
3V3_UP
4K7
JTAG_CPLD
JTAG_3
VCCAUX_3V3_UP
JTAG
XC2C384_FTG256
TDI,TMS,TCK,TDO
2V5_BL
CLK_CTRL_2V5<0..19>
JC FIXED SEL0
JC FIXED SEL1
JC LHC SEL0
JC LHC SEL1
CLOCK_MUX_SEL0
CLOCK_MUX_SEL1
FANOUT1_CLK_SEL
FANOUT2_CLK_SEL
FANOUT3_CLK_SEL
FANOUT4_CLK_SEL
FANOUT5_CLK_SEL
FANOUT6_CLK_SEL
FANOUT7_CLK_SEL
FANOUT8_CLK_SEL
FANOUT9_CLK_SEL
FANOUT10_CLK_SEL
FANOUT11_CLK_SEL
FANOUT12_CLK_SEL
FANOUT13_CLK_SEL
FANOUT14_CLK_SEL
CTRL_MEZZ_Spare[0..11]
BANK1_2V5_BL
CPLD1-2_Spare[0..11]
To CPLD1
FF ADDRESSING
I2C_I/O EXPANDER
I2C
To CTRL_MEZZ
TCA9538PWR
GPIO[1..8]
PUSH[1..3]
BUTTON
JC_PROGRAMMER_EN
FF_RX_SEL,RES,INTL
FF_TX_SEL,RES,INTL
FF_RXTX_SEL,RES,INTL
U1_FF1
U1_FF2
U1_FF3
U1_FF4
U1_FF5
U1_FF6
U1_FF7
U1_FF8
U1_FF9
U1_FF10
U1_FF11
U1_FF12
U2_FF1
U2_FF2
U2_FF3
U2_FF4
U2_FF5
U2_FF6
U2_FF7
U2_FF8
U2_FF9
U2_FF10
U2_FF11
U2_FF12
FELIX
CTRL_MEZZ_Spare[0..9]
RESETSW_CTRL_MEZZ Front
BANK3 VCCIO=3V3_BL
BANK4 VCCIO=3V3_BL
to CTRL_MEZZ
CONTROL CPLDs
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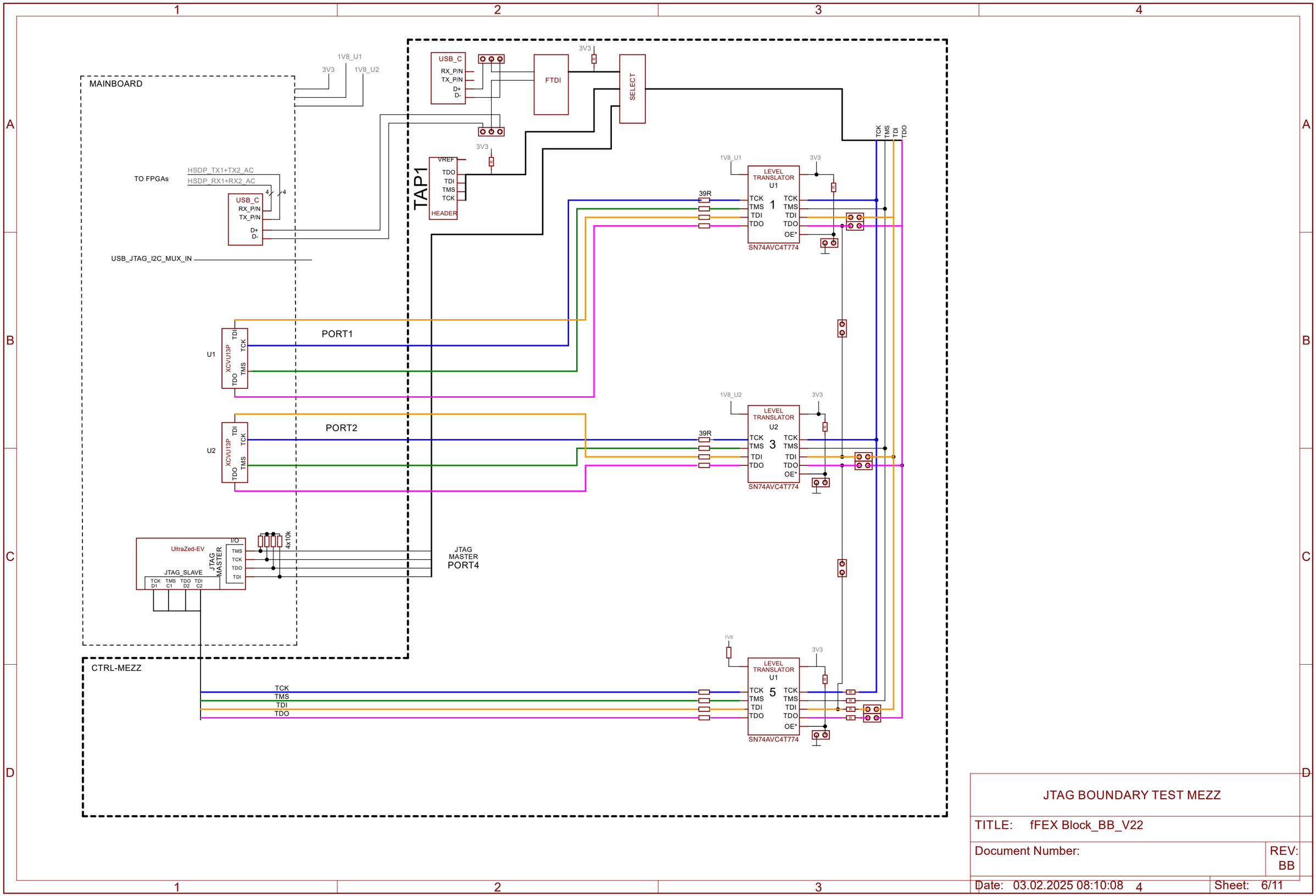

JTAG BOUNDARY TEST MEZZ

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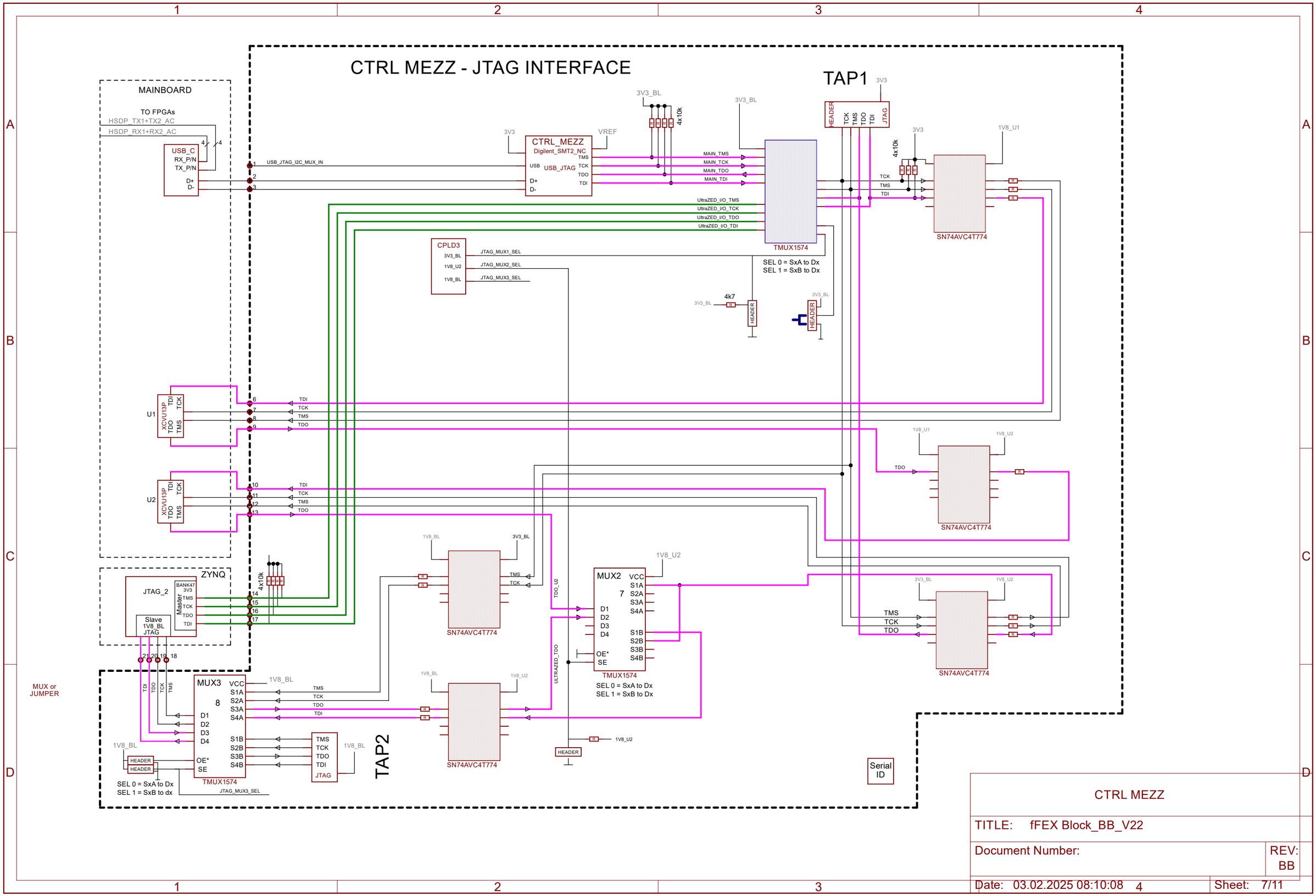
CTRL MEZZ - JTAG INTERFACE



CTRL MEZZ

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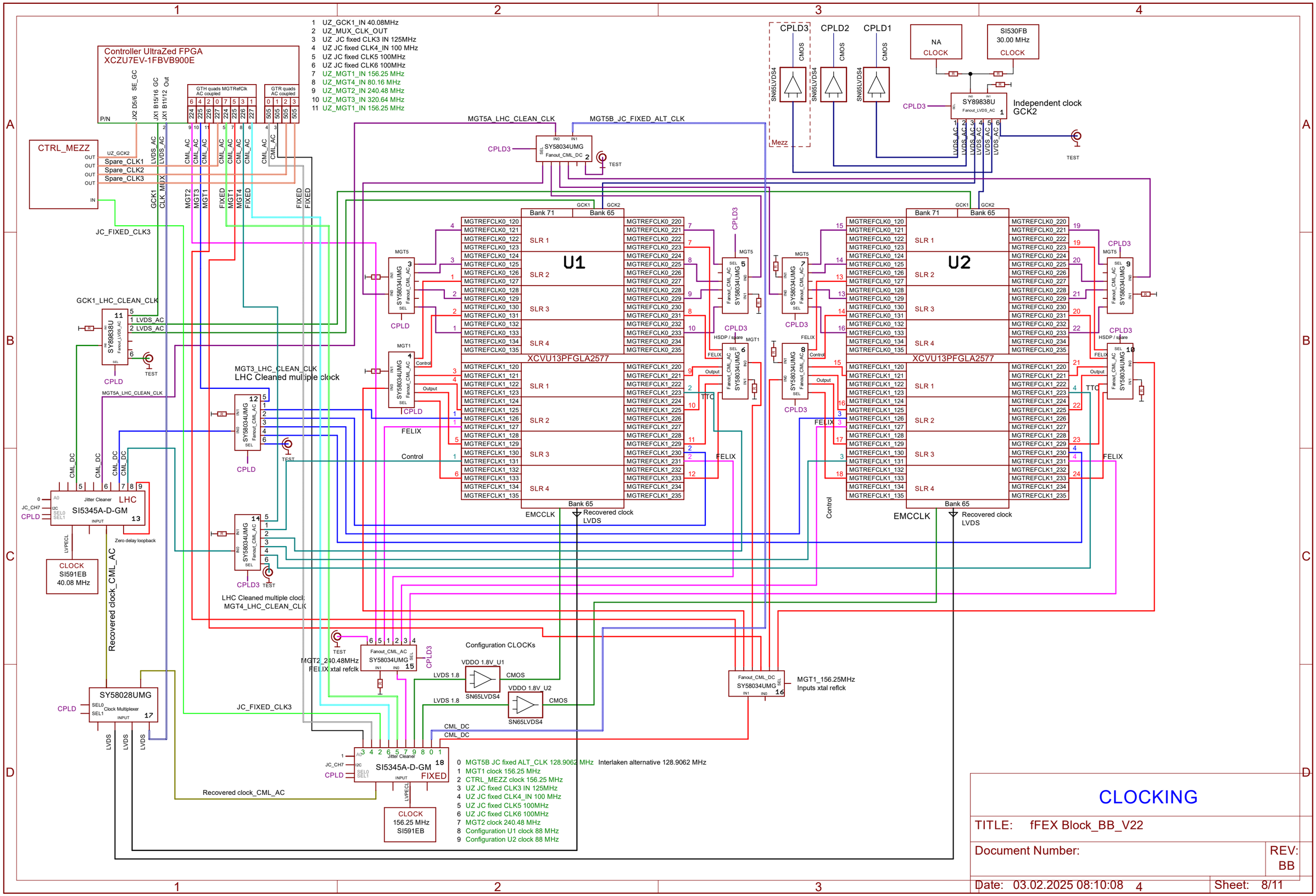
1 UZ_GCK1_IN 40.08MHz
2 UZ_MUX_CLK_OUT
3 UZ JC fixed CLK3 IN 125MHz
4 UZ JC fixed CLK4_IN 100 MHz
5 UZ JC fixed CLK5 100MHz
6 UZ JC fixed CLK6 100MHz
7 UZ_MGT1_IN 156.25 MHz
8 UZ_MGT4_IN 80.16 MHz
9 UZ_MGT2_IN 240.48 MHz
10 UZ_MGT3_IN 320.64 MHz
11 UZ_MGT1_IN 156.25 MHz
Controller UltraZed FPGA
XCZU7EV-1FBVB900E
CTRL_MEZZ
Spare_CLK1
Spare_CLK2
Spare_CLK3
JC_FIXED_CLK3
GCK1_LHC_CLEAN_CLK
MGT5A_LHC_CLEAN_CLK
MGT5B_JC_FIXED_ALT_CLK
MGT3_LHC_CLEAN_CLK
LHC Cleaned multiple clock
LHC Cleaned multiple clock
MGT4_LHC_CLEAN_CLK
SI5345A-D-GM
LHC
CLOCK
SI591EB
40.08 MHz
Recovered clock_CML_AC
SY58028UMG
Clock Multiplexer
SY58034UMG
SY89838U
SY58034UMG
CPLD3
CPLD2
CPLD1
NA
CLOCK
SI530FB
30.00 MHz
CLOCK
Independent clock
GCK2
Mezz
U1
U2
XCVU13PFGLA2577
Bank 71
Bank 65
SLR 1
SLR 2
SLR 3
SLR 4
EMCCLK
Recovered clock
LVDS
Configuration CLOCKs
VDDO 1.8V_U1
VDDO 1.8V_U2
SN65LVDS4
MGT2_240.48MHz
FELIX xtal refclk
MGT1_156.25MHz
Inputs xtal reflck
SI5345A-D-GM
FIXED
CLOCK
156.25 MHz
SI591EB
0 MGT5B JC fixed ALT_CLK 128.9062 MHz
Interlaken alternative 128.9062 MHz
1 MGT1 clock 156.25 MHz
2 CTRL_MEZZ clock 156.25 MHz
3 UZ JC fixed CLK3 IN 125MHz
4 UZ JC fixed CLK4_IN 100 MHz
5 UZ JC fixed CLK5 100MHz
6 UZ JC fixed CLK6 100MHz
7 MGT2 clock 240.48 MHz
8 Configuration U1 clock 88 MHz
9 Configuration U2 clock 88 MHz
CLOCKING
TITLE: fFEX Block_BB_V22
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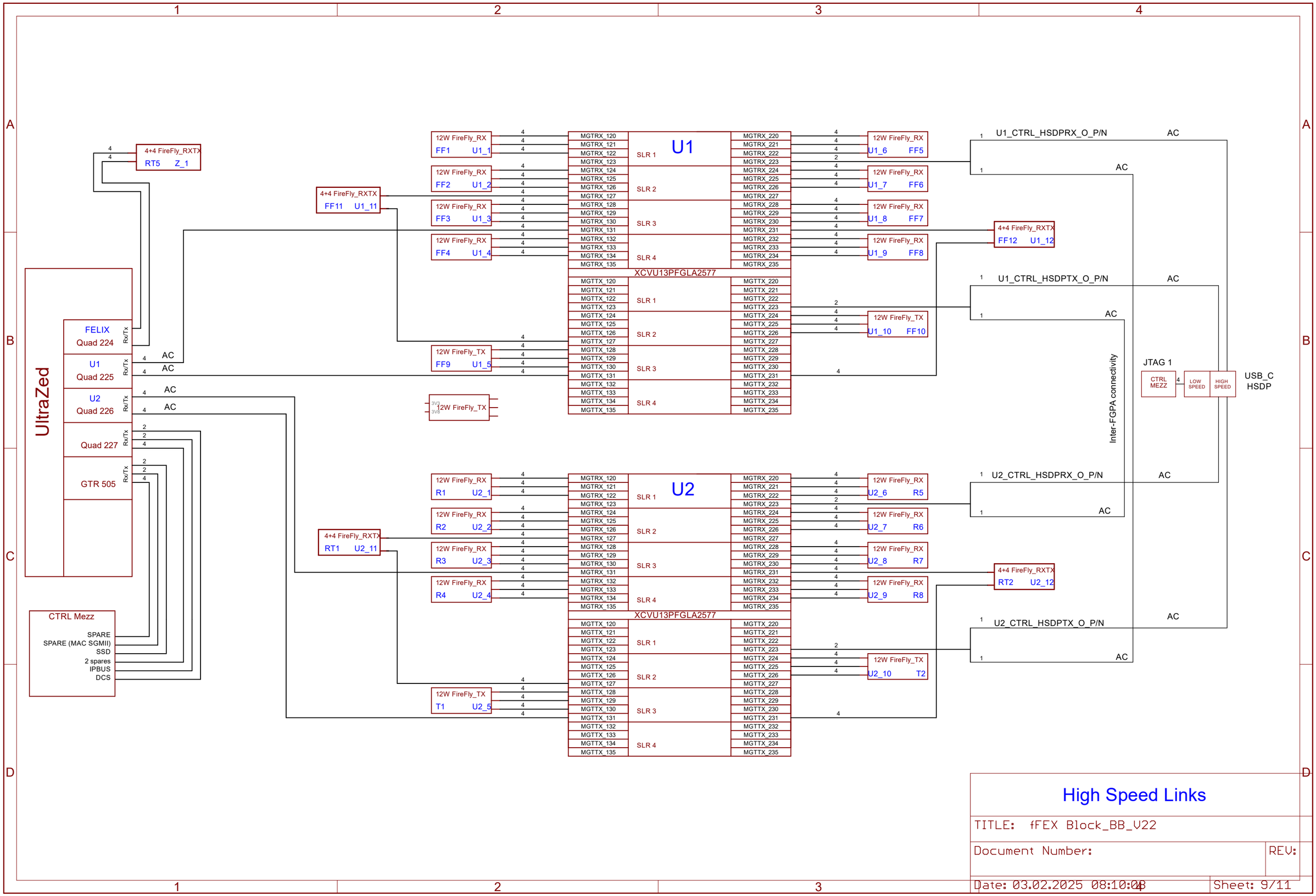

High Speed Links

TITLE: fFEX Block_BB_V22

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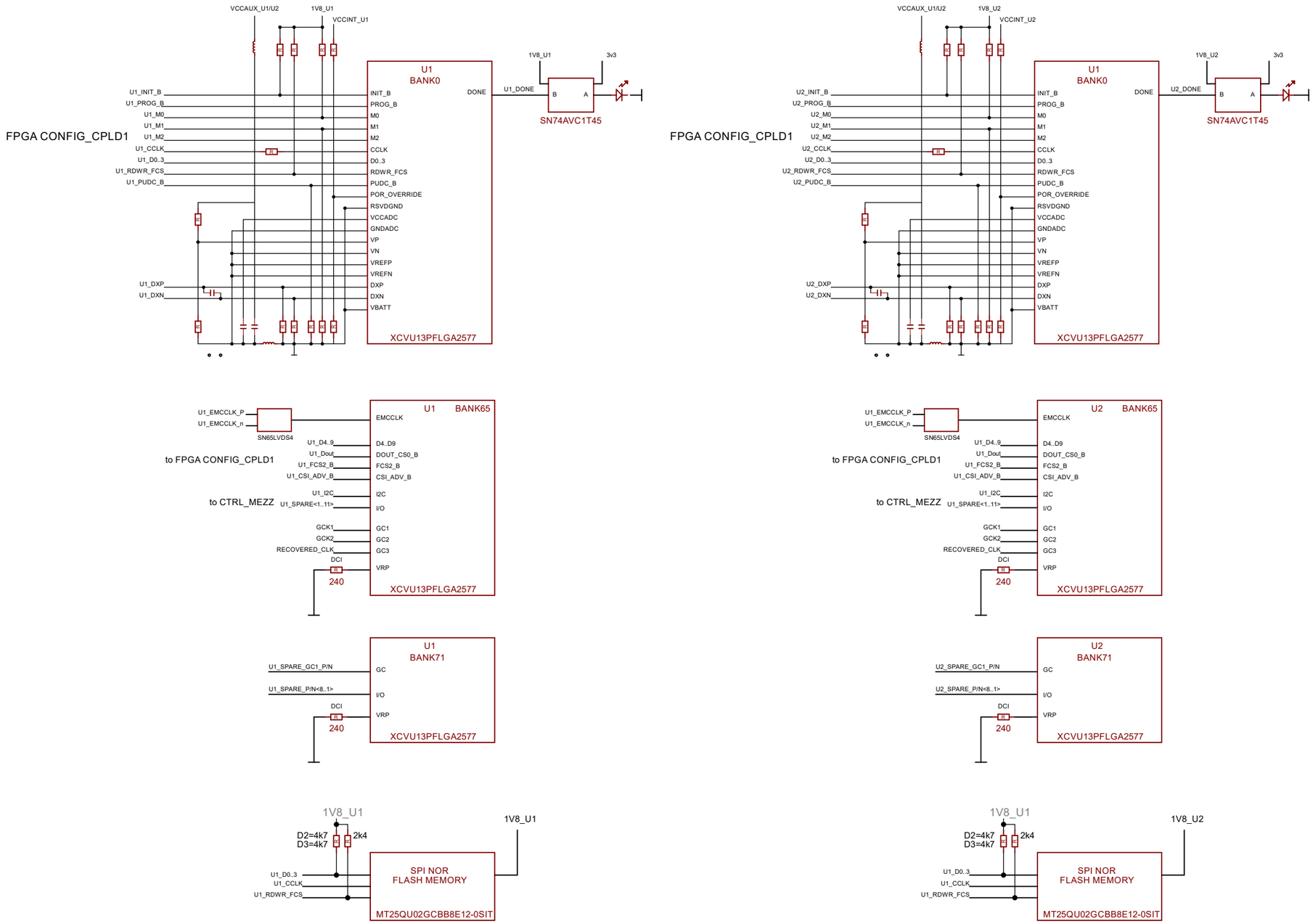

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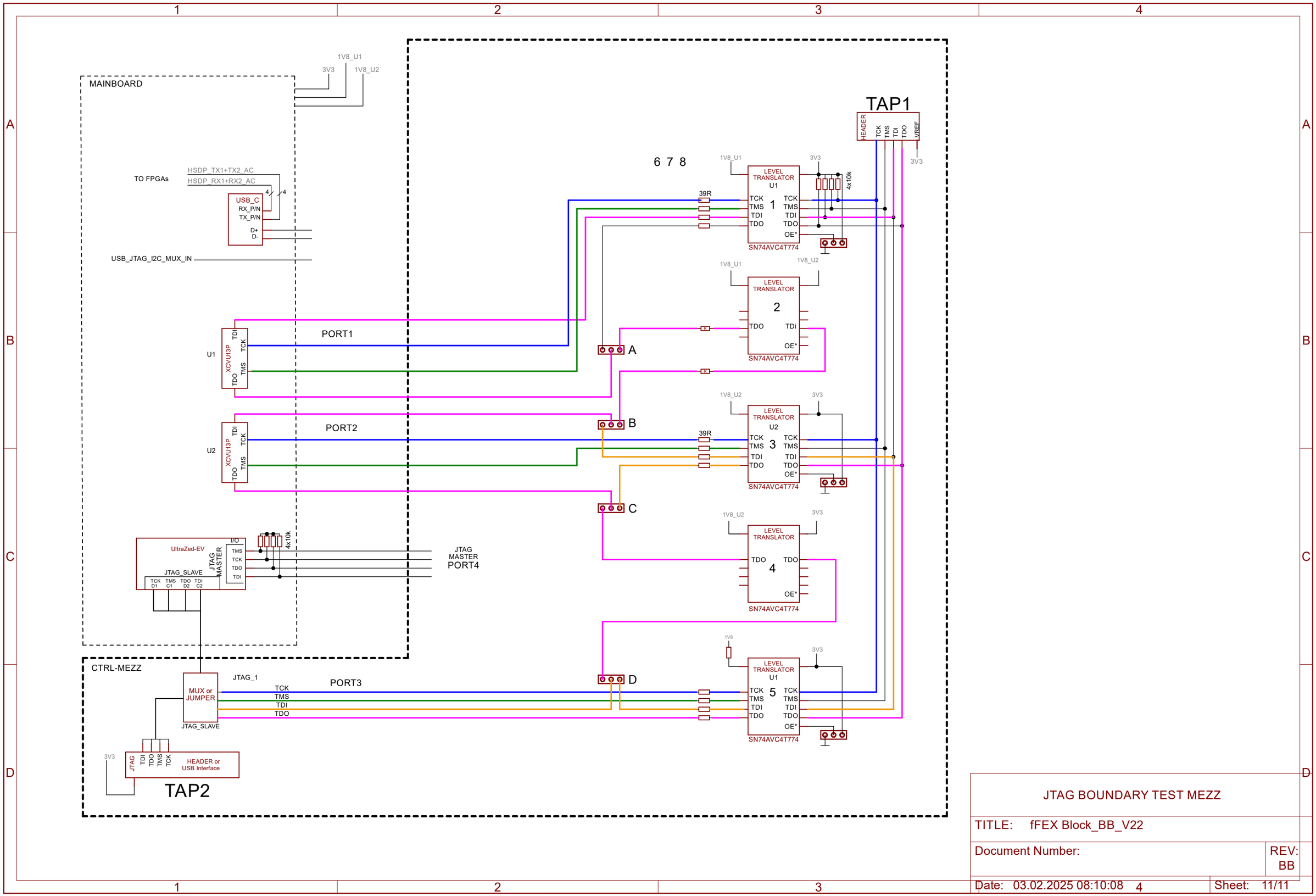

JTAG BOUNDARY TEST MEZZ

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