New TTCDec (TTC decoder card) Specification

Draft 0.5

Weiming, June 04, 2003

1. Scope

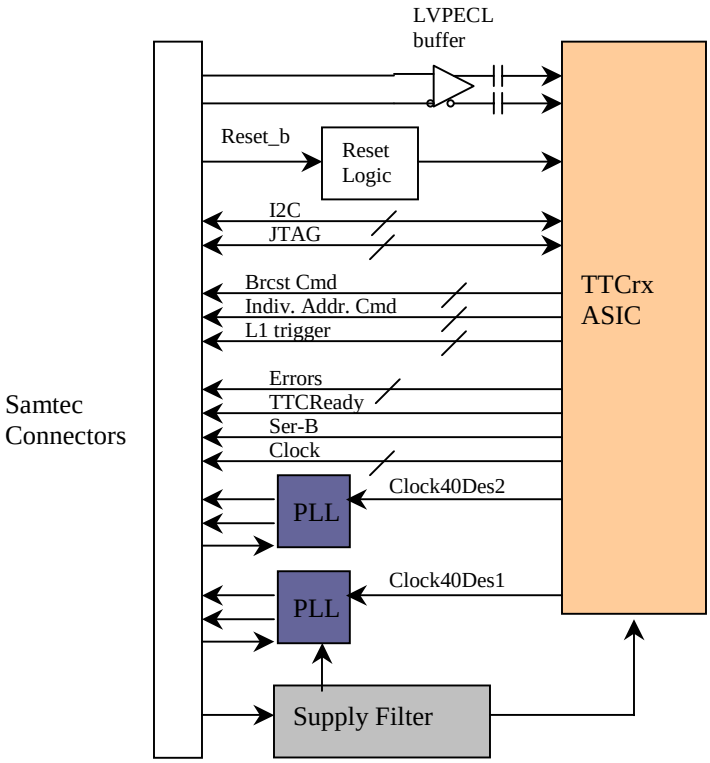
The TTC system of LHC provides all signals necessary to synchronize the detectors, the level 1 trigger accept signal and arbitrary control data, which are distributed on a single optical fiber. The TTCrx ASIC acts as an interface between the TTC system and its receiving end users.

In ATLAS calorimeter level 1 trigger system, the optical TTC signal from the ATLAS TTC optical fiber distribution tree is first received by a TCM 9U module, where it is converted into electrical differential PECL signal and distributed to other 9U modules (PPM, CPM, JEM, CMM, ROD) within the same crate via the custom 9U VME processor backplane. The new TTCrxDec cards are used on these modules to decode the incoming electrical TTC signal. This new TTCDec card will be used in the final production of ATLAS calorimeter level 1 trigger system.

The new TTCrxDec is implemented as a plug-on daughter card. Basically, all the TTCrx ASIC decoded output signals are made directly available on the connectors of the TTCDec card. The recovered clocks from TTCrx ASIC are too jittery to be used as the reference clock for high-speed serial link (e.g. G-Link). Commercial PLLs are used to clean these clocks and clean clocks are available on the connectors of TTCDec card.

2. Requirement and specifications

2.1 Block diagram



2.2 TTCrx Version

TTCrx fpBGA144 Ver3.2, TTCrx Reference Manual Version 3.8.

2.3 TTC signal receiver

A LVPECL MAX9321 line receiver is used on the TTCDec to receive the TTC differential signal.

2.4 Power supply

The TTCDec operates with only +3.3V.
Supply filter generates quiet analog supply for analog parts of the PLLs and the TTCrx.

2.5 Reset

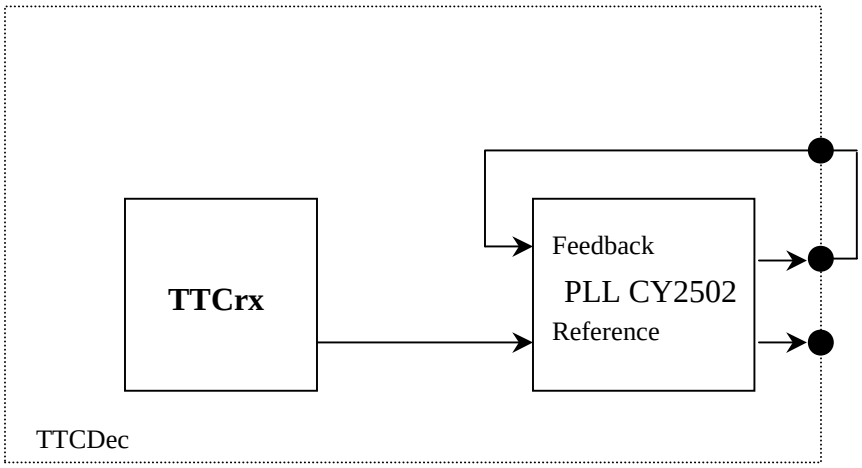
External active low Reset_b signal is ANDed with TTCDec on-board power-up reset signal, which resets the TTCrx upon power-up. The external Reset_b pulse should be provided by 9U motherboard with a minimum width of 50us.

2.6 Clocks and PLLs

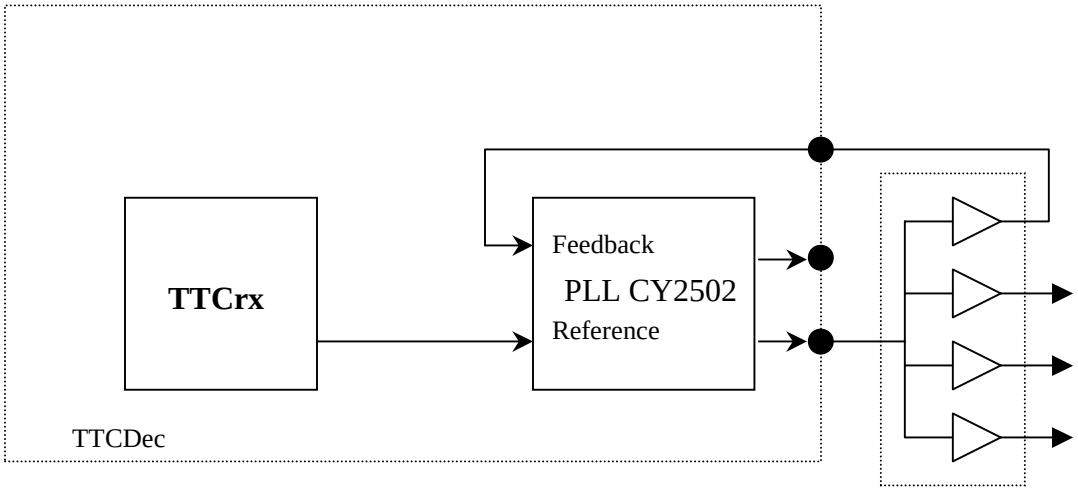
The raw Clock40 is directly connected to the H2 connector.

The Clock40Des1 and Clock40Des2 are cleaned by two individual LVCMOS PLLs, which provide zero-delay single-ended LVCMOS output clocks. Both the PLL output clocks and the PLL feedback signal are connected to the connector, allowing external fanout to be placed within the feedback loop without adding any delay to the clock. (As show below)

PLL chip: CY2502, 25MHz to 85MHz, 150ps Max Cycle-Cycle Jitter.



TTCDec in normal use (showing one of the two PLLs)



TTCDec used to compensate the delay of an external fanout buffer

2.6 Signal timing

All signal tracks are of minimum length. The time skew due to the signal track length difference is negligible (no more than 0.1ns).

2.7 Indicators

One LED for TTCReady. TTCReady is also available on SM connector.

2.8 Grounding

The internal ground planes in the middle of the Samtec Q-Strip connectors H1 and H2 should be connected to the PCB ground to improve electrical performance.

For high-speed signals (especially the clean clock), ground pins should also be assigned near the signal pins within the connectors.

2.9 Termination

TTC signal input termination: 100 ohms parallel.
Clean clock output termination: PLL CY2502 has a 25ohms internal series output resistor. A 35ohms external series resistor is put on TTCDec for each PLL output clock, resulting in the total source series termination of 60ohms.

All other signals: no termination on TTCDec.

2.10 Configuration

No EPROM is needed. EnProm/PromReset pin is connected to GND via a 100k resistor. SubAddr<7:6> are connected to GND via 100k resistors.

I2C_ID and Chip_ID addresses are set initially by resistors on SubAddr<5:0> and Dout<7:0> upon reset. Dout<5:0> are connected to GND via 100k resistors, Dout<7:6> and SubAddr<5:0> are connected to VCC via 100k resistors. So the initial I2C address is 00h, and the initial TTC chip address is 3FC0h.

The TTCrx can be configured through I2C interface. Two pull-up resistors on the TTCDec connect SCL and SDA to VCC for correct operation.

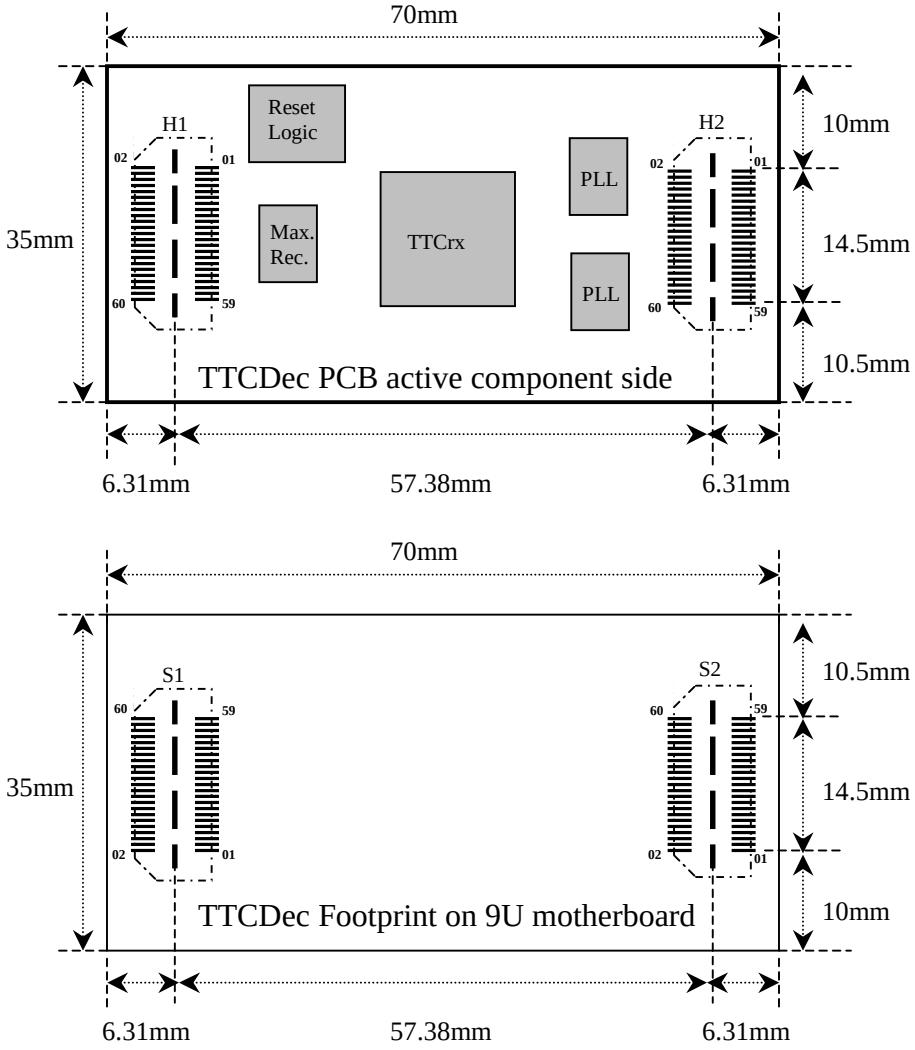
If JTAG signals are not used, the JTGATCK, JTAGTDI, JTAGTMS and JTAGTRST_b signals (CMOS inputs) should be fixed to logic 0 on the 9U motherboards.

3 Implementation

3.1 Physical dimensions

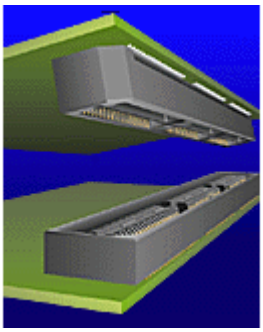
All active components (TTCrx, PLL etc.) are placed at the same side of PCB as the Samtec connectors H1 and H2. This arrangement allows for total TTCDec height of no more than 8mm (5mm connector height + 1.6mm PCB thickness + 1mm ceramics capacitor thickness). On 9U motherboard, no components should be placed underneath the TTCDec except for the two sockets S1 and S2.

The physical dimensions are given below. The datasheet of Samtec QStrip Mezzanine connectors should be referred to when making the footprints for the headers and sockets. The alignment pins of the connectors should be put within the footprints for assembly. Attention should be paid to the different numbering of pin assignment for header footprint and socket footprint.



3.2 Connector type and Pin Assignments

Samtec Q-Strip Mezzanine Connectors:
QSH-030-01-L-D-A (socket on 9U board)
QTH-030-01-L-D-A (header on TTCDec)
Pin pitch: 0.5mm
Pin number: 60 (30 per row, dual rows)
Stack height: 5mm



Two QTH-030-01-L-D-A headers (H1 and H2) are put on the TTCDec on both sides. The H1 and H2 headers' Pin assignments and the TTCrx Pin definition are given below.

H1 Connector

	1	2	3	4	5	6	7	8	9	10	11	12
A	-	-	-	Dout5	VDD	Dout5tr	DQ1	SubAddr5	SubAddr3	-	-	-
B	-	-	-	Dout6	Dout2	Dout0	DQ0	VDD	SubAddr2	-	-	-
C	PromD	Reset_b	-	Dout7	Dout3	Dout1	DQ2	GND	SubAddr4	-	-	DbEn5tr
D	VDD	TTCReady	PromReset	-	Dout4	GND	DQ3	SubAddr6	-	Brest3tr1	Brest3	Brest2
E	GND	GND	VDD	GND	PromClk	-	SubAddr1	SubAddr0	SimEn5tr	GND	GND	VDD
F	In	-	-	-	A_VDD	SubAddr7	GND	ClockL1A	-	-	-	Clock40Des2
G	In_b	GND	A_VDD	A_VDD	GND	-	BCnt2	GND	VDD	VDD	GND	Clock40Des1
H	VDD	GND	SCL	JTAGTDI	-	BCnt11	-	-	VDD	GND	Clock40	VDD
J	JTAGTDO	SDA	JTAGTMS	-	BCnt7	BCnt6	EvCntH5tr	L1Accept	-	Brest5	Brest4	VDD
K	JTAGTCK	-	-	Ser_B_Clk	GND	BCnt3	VDD	EvCntL5tr	Brest7	-	Brest6	Brest3tr2
L	-	-	-	BCnt10	BCnt9	BCnt5	BCnt0	BCnt3tr	EvCntRes	-	-	-
M	-	JTAGTRST_b	-	VDD	BCnt8	BCnt4	BCnt1	GND	BCntRes	-	-	-

H2 Connector

TTCrx fpBGA144 Ver3.2 Pin Definition

Pin No.	*Pin Name*	*Pin No.*	*Pin Name*
1	DoutStr	2	GND
3	DQ0	4	DQ1
5	DQ2	6	DQ3
7	GND	8	GND
9	SubAddr0	10	SubAddr1
11	SubAddr2	12	SubAddr3
13	SubAddr4	14	SubAddr5
15	SubAddr6	16	SubAddr7
17	GND	18	GND
19	Dout0	20	Dout1
21	Dout2	22	Dout3
23	Dout4	24	Dout5
25	Dout6	26	Dout7
27	GND	28	GND
29	Reset_b	30	TTCReady
31	GND	32	
33	GND	34	GND
35	In	36	GND
37	In_b	38	GND
39	GND	40	GND
41	GND	42	
43	SCL	44	
45	SDA	46	VCC
47	GND	48	VCC
49	JTAGTDI	50	VCC
51	JTAGTMS	52	VCC
53	JTAGTDO	54	VCC
55	JTAGTCK	56	VCC
57	JTAGTRST_b	58	VCC
59	GND	60	VCC

H1 Header Pin Assignment

Pin No.	*Pin Name*	*Pin No.*	*Pin Name*
1	SinErrStr	2	DbErrStr
3	GND	4	GND
5	Clock40	6	Clock40L1A
7	GND	8	GND
9	Clock40Des2_FBIN	10	GND
11	GND	12	Clock40Des1_FBIN
13	Clock40Des2_Out1	14	GND
15	GND	16	Clock40Des1_Out1
17	Clock40Des2_Out2	18	GND
19	GND	20	Clock40Des1_Out2
21	GND	22	GND
23	GND	24	GND
25	BrcstStr1	26	Brcst2
27	Brcst3	28	Brcst4
29	Brcst5	30	BrcstStr2
31	Brcst7	32	Brcst6
33	BCntRes	34	EvCntRes
35	GND	36	GND
37	EvCntHStr	38	L1Accept
39	BCntStr	40	EvCntLStr
41	GND	42	GND
43	BCnt1	44	BCnt0
45	BCnt3	46	BCnt2
47	BCnt5	48	BCnt4
49	GND	50	GND
51	BCnt7	52	BCnt6
53	BCnt9	54	BCnt8
55	BCnt11	56	BCnt10
57	GND	58	GND
59	GND	60	Ser_B_Ch

H2 Header Pin Assignment

3.3 Testpoints

Since all the active components are placed on the connector side of the PCB, it will be very difficult to probe signals when the TTCDec resides on a 9U motherboard. So testpoints should be placed on the other side of the PCB.

Testpoints should be provided for TTC input, TTCReady, Reset, Clock40, VCC and GND.

4 Testing strategy

Two steps can be used to test the TTCDec card:

1. The TTCDec can initially be tested by a test card, which provide sockets to accept the TTCDec, the required supplies, terminations for required signals and Testpoints for Scope and Logic Analyzer. (This test card may be integrated into the TTCFanout module for test purpose.)
2. Online test needs a 9U module (PPM, CPM, JEM, CMM or ROD) that can accept the TTCDec and read out the data from it. Test software is required.