escaped between two pads, assuming a space constraint equal to the trace width. For a
discussion of signal routing specific to Virtex-II devices, see www.xilinx.com for currently
available application notes.

As packages are able to handle more I/Os with a minimum increase in size, the signal
integrity of those signals must be considered, regardless of clock frequency. Especially with
the largest packages, precise PCB layer stackup is required. Parameters such as board
material, trace width, pad type, and stackup must be defined based on simulation, and the
fabrication drawings must be marked with “precise layer stackup” and the stackup
specified. A number of board-level signal integrity simulators exist, and careful attention
to PCB design rules creates a robust design with low EMI and high signal reliability.

Board Routability Guidelines

Board-Level BGA Routing Challenges

Xilinx ball grid array (BGA) wire-bond and flip-chip packages contain a matrix of solder
balls (see Figure 4-46). These packages are made of multilayer BT substrates. Signal balls
are in a perimeter format. Power and ground pins are grouped together appropriately.

![Figure 4-46: Fine-Pitch BGA Pin Assignments](x157_.01_.112800)

The number of layers required for effective routing of these packages is dictated by the
layout of pins in each package. If several other technologies and components are already
present on the board, the system cost is factored with every added board layer. The intent
of a board designer is to optimize the number of layers required to route these packages,
considering both cost and performance. This section provides guidelines for minimizing
required board layers for routing BGA products using standard PCB technologies
(5 mils-wide lines and spaces or 6 mils-wide lines and spaces).

For high performance and other system needs, designers can use premium technologies
with finer lines/spaces on the board. The pin assignment and pin grouping scheme in BGA
packages enables efficient routing of the board with an optimum number of required
board layers.
Board Routing Strategy

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of board layout when designing the board pads to match component-side land geometry. Typical values for these land pads are described in Figure 4-47 and summarized in Table 4-5.

Table 4-5: Summary of Typical Land Pad Values (mm)

<table>
<thead>
<tr>
<th>Land Pad Characteristics</th>
<th>CS144</th>
<th>FG256</th>
<th>FG456</th>
<th>FG676</th>
<th>BG575</th>
<th>BG728</th>
<th>FF896</th>
<th>FF1152</th>
<th>FF1517</th>
<th>BF957</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Land Pad Diameter (SMD)</td>
<td>0.35</td>
<td>0.45</td>
<td>0.45</td>
<td>0.45</td>
<td>0.61</td>
<td>0.61</td>
<td>0.48</td>
<td>0.48</td>
<td>0.48</td>
<td>0.61</td>
</tr>
<tr>
<td>Solder Land (L) Diameter</td>
<td>0.33</td>
<td>0.40</td>
<td>0.40</td>
<td>0.40</td>
<td>0.56</td>
<td>0.56</td>
<td>0.45</td>
<td>0.45</td>
<td>0.45</td>
<td>0.56</td>
</tr>
<tr>
<td>Opening in Solder Mask (M) Diameter</td>
<td>0.44</td>
<td>0.50</td>
<td>0.50</td>
<td>0.50</td>
<td>0.66</td>
<td>0.66</td>
<td>0.55</td>
<td>0.55</td>
<td>0.55</td>
<td>0.66</td>
</tr>
<tr>
<td>Solder (Ball) Land Pitch (e)</td>
<td>0.80</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.27</td>
<td>1.27</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>1.27</td>
</tr>
<tr>
<td>Line Width Between Via and Land (w)</td>
<td>0.130</td>
<td>0.130</td>
<td>0.130</td>
<td>0.130</td>
<td>0.203</td>
<td>0.203</td>
<td>0.130</td>
<td>0.130</td>
<td>0.130</td>
<td>0.203</td>
</tr>
<tr>
<td>Distance Between Via and Land (D)</td>
<td>0.56</td>
<td>0.70</td>
<td>0.70</td>
<td>0.70</td>
<td>0.90</td>
<td>0.90</td>
<td>0.70</td>
<td>0.70</td>
<td>0.70</td>
<td>0.90</td>
</tr>
<tr>
<td>Via Land (VL) Diameter</td>
<td>0.51</td>
<td>0.61</td>
<td>0.61</td>
<td>0.61</td>
<td>0.65</td>
<td>0.65</td>
<td>0.61</td>
<td>0.61</td>
<td>0.61</td>
<td>0.65</td>
</tr>
<tr>
<td>Through Hole (VH), Diameter</td>
<td>0.250</td>
<td>0.300</td>
<td>0.300</td>
<td>0.300</td>
<td>0.356</td>
<td>0.356</td>
<td>0.300</td>
<td>0.300</td>
<td>0.300</td>
<td>0.356</td>
</tr>
<tr>
<td>Pad Array</td>
<td>-</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
</tr>
<tr>
<td>Matrix or External Row</td>
<td>13 x 13</td>
<td>16 x 16</td>
<td>22 x 22</td>
<td>26 x 26</td>
<td>24 x 24</td>
<td>27 x 27</td>
<td>30 x 30</td>
<td>34 x 34</td>
<td>39 x 39</td>
<td>31 x 31</td>
</tr>
<tr>
<td>Periphery Rows</td>
<td>4</td>
<td>-</td>
<td>7</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Notes:
1. Dimension in millimeters.
2. 3 x 3 matrix for illustration only, one land pad shown with via connection.
3. FG456 package has solder balls in the center in addition to the periphery rows of balls.
4. Component land pad diameter refers to the pad opening on the component side (solder-mask defined).
For Xilinx BGA packages, non-solder-mask defined (NSMD) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 4-47. The space between the NSMD pad and the solder mask, as well as the actual signal trace widths, depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Selection of pad types and sizes determines the available space between adjacent balls for signal escape. Based on PCB capability, the number of lines that can share the available space is described in Figure 4-48. Based on geometrical considerations, if one signal escapes between adjacent balls, then two signal rows can be routed on a single metal layer. This is illustrated in Figure 4-48 as routing with one line/channel, either at 6 mils-wide lines and spaces or 5 mils-wide lines and spaces. Using this suggested routing scheme, a minimum of eight PCB layers are required to route 10 signal rows in a package.

A slightly lower trace width can be used by the inner signal rows routed in internal layers than the width used in top and bottom external or exposed traces. Depending on the signal being handled, the practice of “necking down” a trace in the critical space between the BGA balls is allowable. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.

**Figure 4-48:** FG676 PC Board Layout/Land Pattern

Figure 4-48 describes a board-level layout strategy for a Xilinx 1.0 mm pitch FG676 package. Detail A in Figure 4-48 describes the opening geometry for the Land Pad and the Solder Mask. Routing with 5 mils-wide lines or spaces allows one signal per channel (between the balls). For successful routing, eight-row deep signal traces require six PCB layers. Figure 4-49 shows the suggested schematic of layers for the six-layer routing scheme.
Using premium board technology, such as Microvia Technology (allowing up to 4 mils-wide lines and spaces), efficient routing is possible with a reduced number of board layers. A grouping scheme for power, ground, control, and I/O pins, might also enable efficient routing.

Table 4-6: Layer-By-Layer Board Routing Examples

<table>
<thead>
<tr>
<th>Package</th>
<th>Standard Routing</th>
<th>Routing With LVDS Pairs</th>
</tr>
</thead>
<tbody>
<tr>
<td>FG256</td>
<td>Top and bottom layers</td>
<td>Top and bottom layers</td>
</tr>
<tr>
<td>FG456</td>
<td>Top, 2nd, and bottom layers</td>
<td>Top, 2nd, and bottom layers</td>
</tr>
<tr>
<td>FG676</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
</tr>
<tr>
<td>BG575</td>
<td>Top, 2nd, and bottom layers</td>
<td>Top, 2nd, and bottom layers</td>
</tr>
<tr>
<td>BG728</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
</tr>
<tr>
<td>FF896</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
</tr>
<tr>
<td>FF1152</td>
<td>Top, 2nd, 3rd, 4th, and bottom layers</td>
<td>Top, 2nd, 3rd, 4th, and bottom layers</td>
</tr>
<tr>
<td>FF1517</td>
<td>Top, 2nd, 3rd, 4th, 5th, and bottom layers</td>
<td>Top, 2nd, 3rd, 4th, 5th, and bottom layers</td>
</tr>
<tr>
<td>BF957</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
<td>Top, 2nd, 3rd, and bottom layers</td>
</tr>
</tbody>
</table>
Figure 4-50: FG256 Standard Routing
Figure 4-51: FG256 Routing With LVDS Pairs
Figure 4-52: FG456 Standard Routing
Figure 4-53: FG456 Routing With LVDS Pairs
Figure 4-54: FG676 Standard Routing
Figure 4-55: FG676 Routing With LVDS Pair

**FG676: ROUTING WITH LVDS PAIR**

**Top Layer**

**Layer 2**

**Layer 3**

**Bottom Layer**

**Component Attribute:**
1) Ball diameter 0.6 mm
2) Pad opening 0.45 mm Solder Mask Defined.

**Notes on Board:**
1) Solder land diameter 0.4 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-56: BG575 Standard Routing

**Top Layer**

**Layer 2**

**Bottom Layer**

**COMPONENT ATTRIBUTE:**

2) Pad opening 0.61 mm Solder Mask Defined.

**NOTES ON BOARD:**

1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-57: BG575 Routing With LVDS Pairs

NOTES ON BOARD:
1) Solder land diameter 0.56 mm. Non-Solder Mask Defined.
2) Via diameter 0.356 mm. on 0.65 mm diameter, Via; 0.127 mm.
3) Layer and bottom layer signal trace width 0.110 mm.
4) Inner layer signal trace 0.110 mm.

**Referring to the diagram:**
- The BG575 routing with LVDS pairs illustrates the placement and routing of signals.
- The bottom layer shows the overall layout with markers indicating signal paths.
- The middle layer highlights specific routing details with land patterns and via connections.
- The top layer focuses on the inner layers, showing further signal traces and connections.

**Legend:**
- Bottom Layer: Overall layout and connection points.
- Layer 2: Detailed routing with solder land and via diameter notes.
- Top Layer: Inner layer routing with specific trace widths.

**Component Attributes:**
- Pad opening 0.61 mm, Solder Mask Defined.
BG728: STANDARD ROUTING

COMPONENT ATTRIBUTE:
2) Pad opening 0.61 mm Solder Mask Defined.

NOTES ON BOARD:
1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
**BG728: ROUTING WITH LVDS PAIR**

**Component Attribute:**

2) Pad opening 0.61 mm Solder Mask Defined.

**Notes On Board:**

1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

*Figure 4-59: BG728 Routing With LVDS Pairs*
Figure 4-60: FF896 Standard Routing

**FF896: STANDARD ROUTING**

**Component Attribute:**
2) Pod opening 0.48 mm Solder Mask Defined.

**Notes on Board:**
1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-61: FF896 Routing With LVDS Pair

**Top Layer**

**Layer 2**

**Layer 3**

**Bottom Layer**

**Component Attribute:**
2) Pad opening 0.48 mm Solder Mask Defined.

**Notes on Board:**
1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-62: **FF1152 Standard Routing**
Figure 4-63: FF1152 Routing With LVDS Pair

COMPONENT ATTRIBUTE:
2) Pad opening 0.48 mm Solder Mask Defined.

NOTES ON BOARD:
1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-64: **FF1517 Standard Routing**
Figure 4-65: FF1517 Routing With LVDS Pairs
Figure 4-66: BF957 Standard Routing

**BF957: STANDARD ROUTING**

**Top Layer**

**Layer 2**

**Layer 3**

**Bottom Layer**

**Component Attribute:**
2) Pad opening 0.61 mm Solder Mask Defined.

**Notes on Board:**
1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.
Figure 4-67: BF957 Routing With LVDS Pairs