escaped between two pads, assuming a space constraint equal to the trace width. For a discussion of signal routing specific to Virtex-II devices, see www.xilinx.com for currently available application notes.

As packages are able to handle more I/Os with a minimum increase in size, the signal integrity of those signals must be considered, regardless of clock frequency. Especially with the largest packages, precise PCB layer stackup is required. Parameters such as board material, trace width, pad type, and stackup must be defined based on simulation, and the fabrication drawings must be marked with "precise layer stackup" and the stackup specified. A number of board-level signal integrity simulators exist, and careful attention to PCB design rules creates a robust design with low EMI and high signal reliability.

Board Routability Guidelines

Board-Level BGA Routing Challenges

Xilinx ball grid array (BGA) wire-bond and flip-chip packages contain a matrix of solder balls (see Figure 4-46). These packages are made of multilayer BT substrates. Signal balls are in a perimeter format. Power and ground pins are grouped together appropriately.

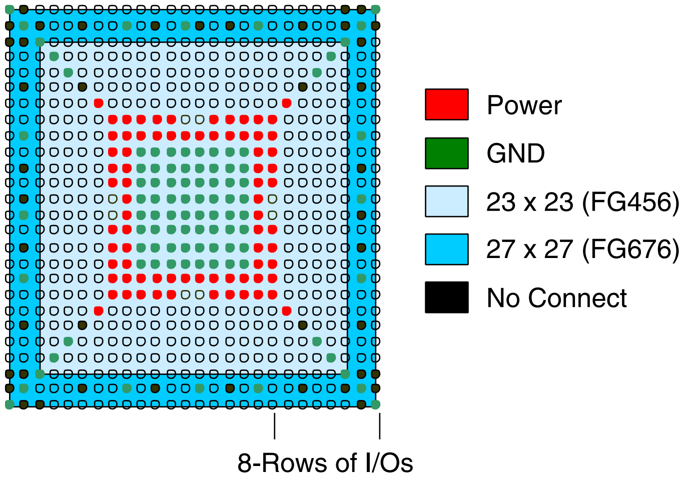


Figure 4-46: **Fine-Pitch BGA Pin Assignments**

The number of layers required for effective routing of these packages is dictated by the layout of pins in each package. If several other technologies and components are already present on the board, the system cost is factored with every added board layer. The intent of a board designer is to optimize the number of layers required to route these packages, considering both cost and performance. This section provides guidelines for minimizing required board layers for routing BGA products using standard PCB technologies (5 mils-wide lines and spaces or 6 mils-wide lines and spaces).

For high performance and other system needs, designers can use premium technologies with finer lines/spaces on the board. The pin assignment and pin grouping scheme in BGA packages enables efficient routing of the board with an optimum number of required board layers.

Board Routing Strategy

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of board layout when designing the board pads to match component-side land geometry. Typical values for these land pads are described in Figure 4-47 and summarized in Table 4-5.

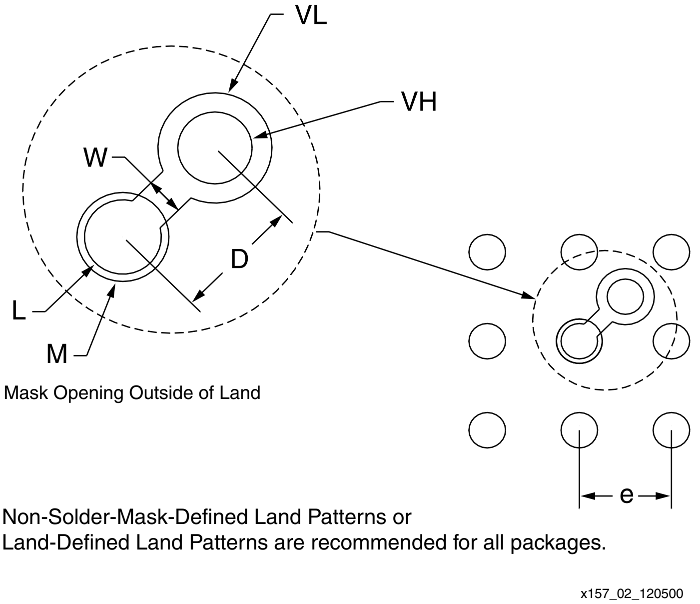


Figure 4-47: **Suggested Board Layout of Soldered Pads for BGA Packages**

Table 4-5: **Summary of Typical Land Pad Values (mm)**

Land Pad Characteristics	CS144	FG256	FG456	FG676	BG575	BG728	FF896	FF1152	FF1517	BF957
Component Land Pad Diameter (SMD)[4]	0.35	0.45	0.45	0.45	0.61	0.61	0.48	0.48	0.48	0.61
Solder Land (L) Diameter	0.33	0.40	0.40	0.40	0.56	0.56	0.45	0.45	0.45	0.56
Opening in Solder Mask (M) Diameter	0.44	0.50	0.50	0.50	0.66	0.66	0.55	0.55	0.55	0.66
Solder (Ball) Land Pitch (e)	0.80	1.00	1.00	1.00	1.27	1.27	1.00	1.00	1.00	1.27
Line Width Between Via and Land (w)	0.130	0.130	0.130	0.130	0.203	0.203	0.130	0.130	0.130	0.203
Distance Between Via and Land (D)	0.56	0.70	0.70	0.70	0.90	0.90	0.70	0.70	0.70	0.90
Via Land (VL) Diameter	0.51	0.61	0.61	0.61	0.65	0.65	0.61	0.61	0.61	0.65
Through Hole (VH), Diameter	0.250	0.300	0.300	0.300	0.356	0.356	0.300	0.300	0.300	0.356
Pad Array	-	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	13 x 13	16 x 16	22 x 22	26 x 26	24 x 24	27 x 27	30 x 30	34 x 34	39 x 39	31 x 31
Periphery Rows	4	-	7[3]	-	-	-	-	-	-	-

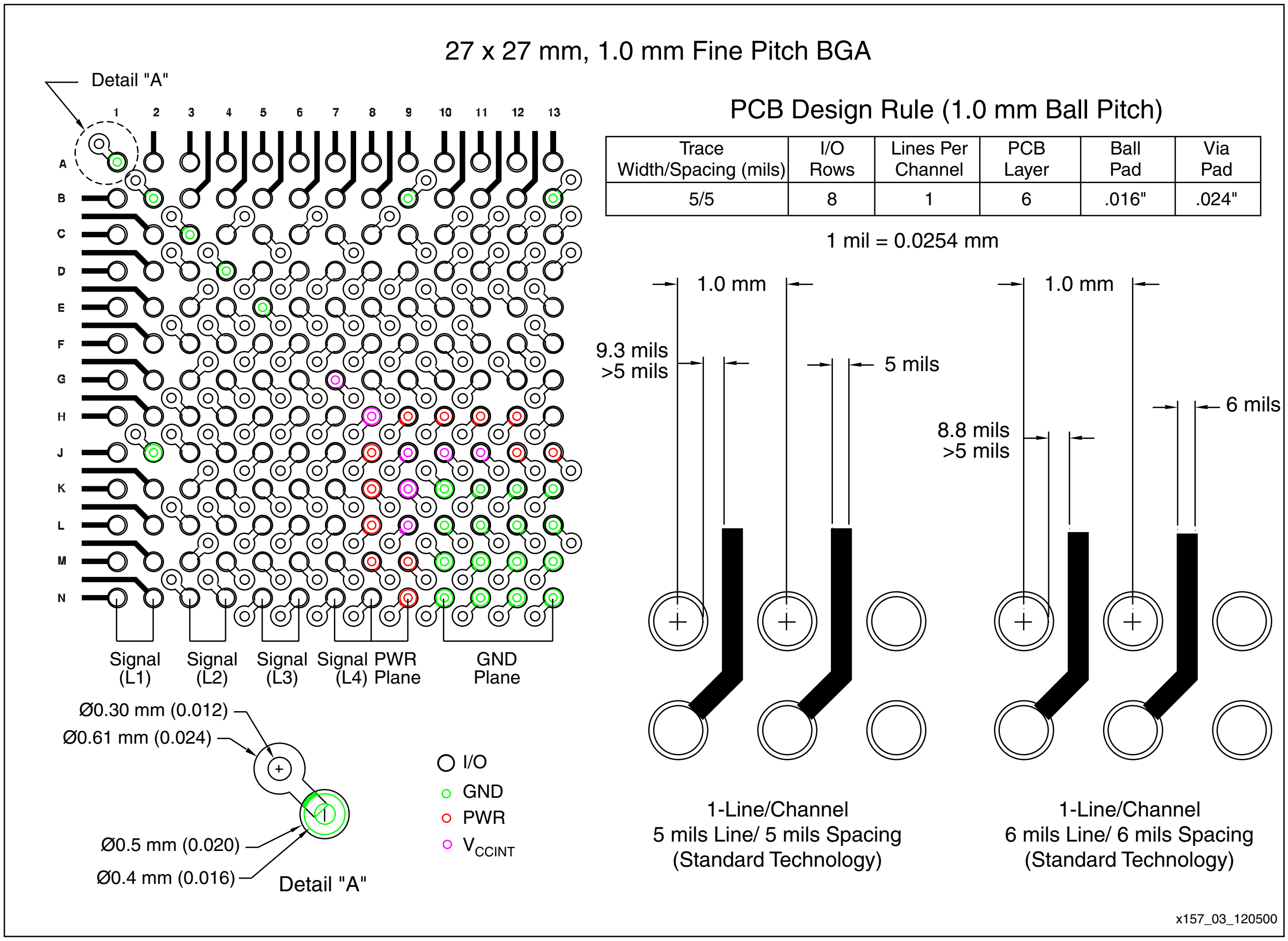
Notes:

1. Dimension in millimeters.
2. 3 x 3 matrix for illustration only, one land pad shown with via connection.
3. FG456 package has solder balls in the center in addition to the periphery rows of balls.
4. Component land pad diameter refers to the pad opening on the component side (solder-mask defined).

For Xilinx BGA packages, non-solder-mask defined (NSMD) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 4-47. The space between the NSMD pad and the solder mask, as well as the actual signal trace widths, depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Selection of pad types and sizes determines the available space between adjacent balls for signal escape. Based on PCB capability, the number of lines that can share the available space is described in Figure 4-48. Based on geometrical considerations, if one signal escapes between adjacent balls, then two signal rows can be routed on a single metal layer. This is illustrated in Figure 4-48 as routing with one line/channel, either at 6 mils-wide lines and spaces or 5 mils-wide lines and spaces. Using this suggested routing scheme, a minimum of eight PCB layers are required to route 10 signal rows in a package.

A slightly lower trace width can be used by the inner signal rows routed in internal layers than the width used in top and bottom external or exposed traces. Depending on the signal being handled, the practice of "necking down" a trace in the critical space between the BGA balls is allowable. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.



Trace Width/Spacing (mils)	I/O Rows	Lines Per Channel	PCB Layer	Ball Pad	Via Pad
5/5	8	1	6	.016"	.024"

Figure 4-48: **FG676 PC Board Layout/Land Pattern**

Figure 4-48 describes a board-level layout strategy for a Xilinx 1.0 mm pitch FG676 package. Detail A in Figure 4-48 describes the opening geometry for the Land Pad and the Solder Mask. Routing with 5 mils-wide lines or spaces allows one signal per channel (between the balls). For successful routing, eight-row deep signal traces require six PCB layers. Figure 4-49 shows the suggested schematic of layers for the six-layer routing scheme.

Using premium board technology, such as Microvia Technology (allowing up to 4 mils-wide lines and spaces), efficient routing is possible with a reduced number of board layers. A grouping scheme for power, ground, control, and I/O pins, might also enable efficient routing.

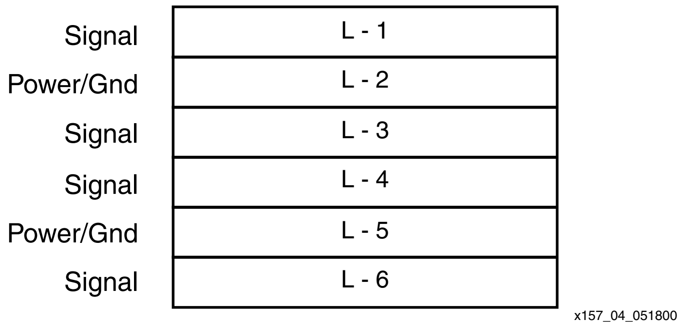
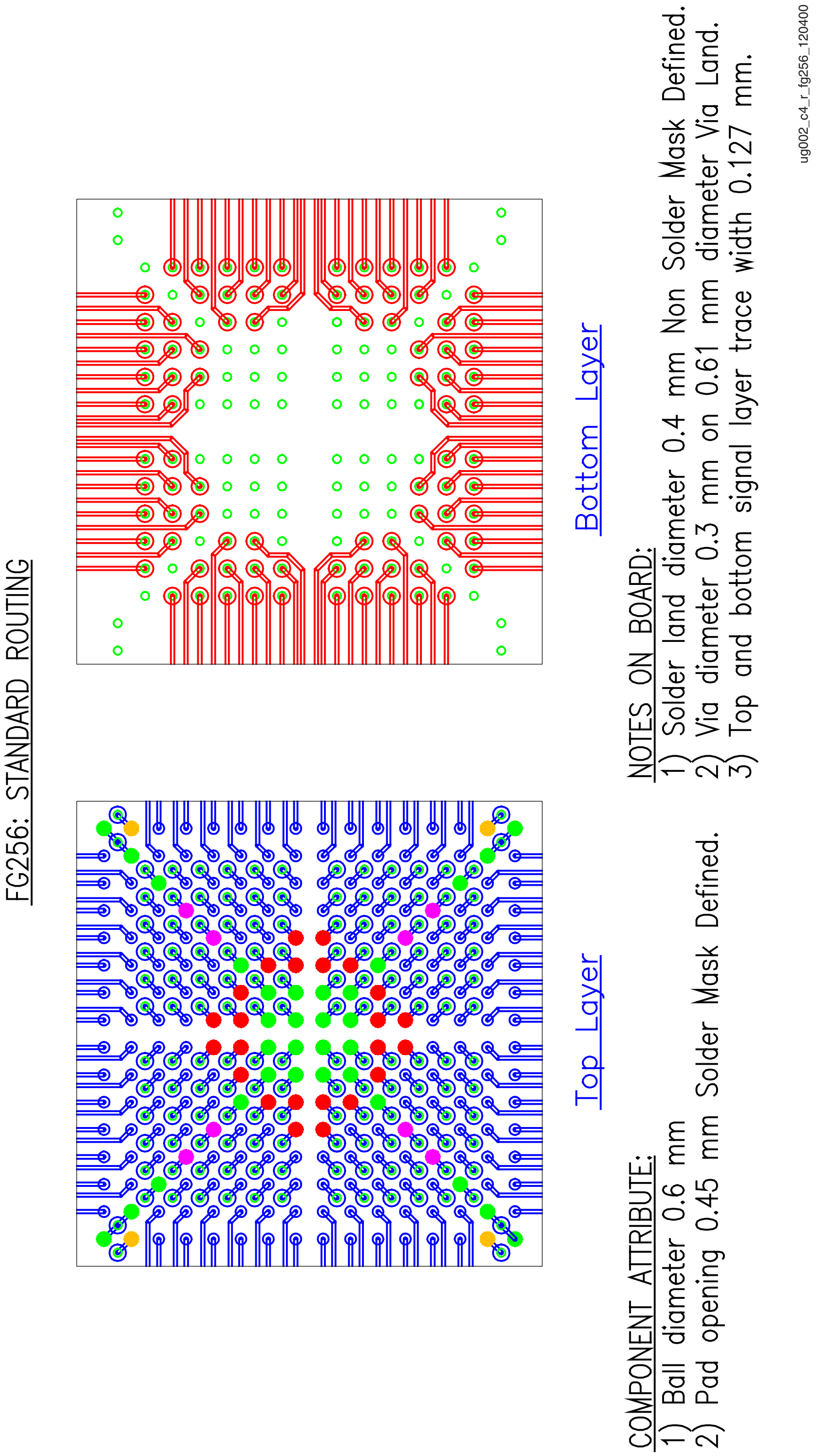


Figure 4-49: **Six-Layer Routing Scheme**

Figure 4-50 through Figure 4-67 show suggested layer-by-layer board routing for each Virtex-II package, including flip-chip packages. These drawings assume a standard PCB technology of 5 mils-wide lines and spaces. Table 4-6 lists the layer-by-layer routing examples provided. More details are contained in XAPP157, which is available on the web at **www.xilinx.com/xapp/xapp157.pdf**, as is a full-color (PDF) version of this document.

Table 4-6: **Layer-By-Layer Board Routing Examples**

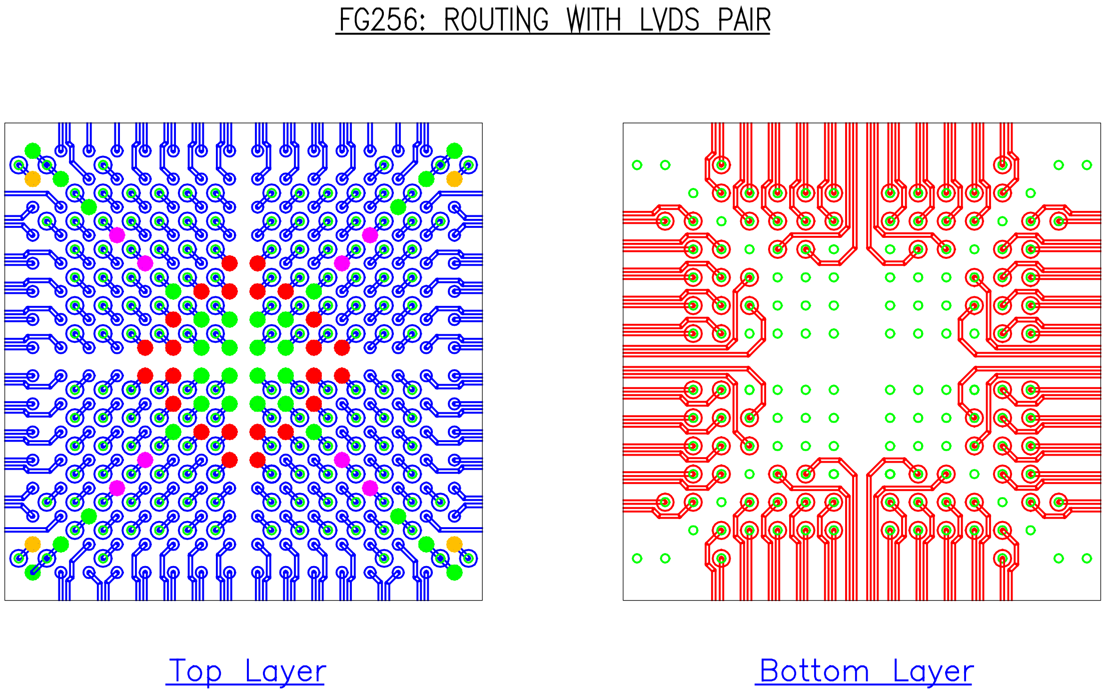
Package	Standard Routing	Routing With LVDS Pairs
FG256	Top and bottom layers	Top and bottom layers
FG456	Top, 2nd, and bottom layers	Top, 2nd, and bottom layers
FG676	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
BG575	Top, 2nd, and bottom layers	Top, 2nd, and bottom layers
BG728	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
FF896	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers
FF1152	Top, 2nd, 3rd, 4th, and bottom layers	Top, 2nd, 3rd, 4th, and bottom layers
FF1517	Top, 2nd, 3rd, 4th, 5th, and bottom layers	Top, 2nd, 3rd, 4th, 5th, and bottom layers
BF957	Top, 2nd, 3rd, and bottom layers	Top, 2nd, 3rd, and bottom layers



COMPONENT ATTRIBUTE:
1) Ball diameter 0.6 mm
2) Pad opening 0.45 mm Solder Mask Defined.

NOTES ON BOARD:
1) Solder land diameter 0.4 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom signal layer trace width 0.127 mm.

Figure 4-50: **FG256 Standard Routing**



COMPONENT ATTRIBUTE:

1) Ball diameter 0.6 mm
2) Pad opening 0.45 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.4 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom signal layer trace width 0.127 mm.

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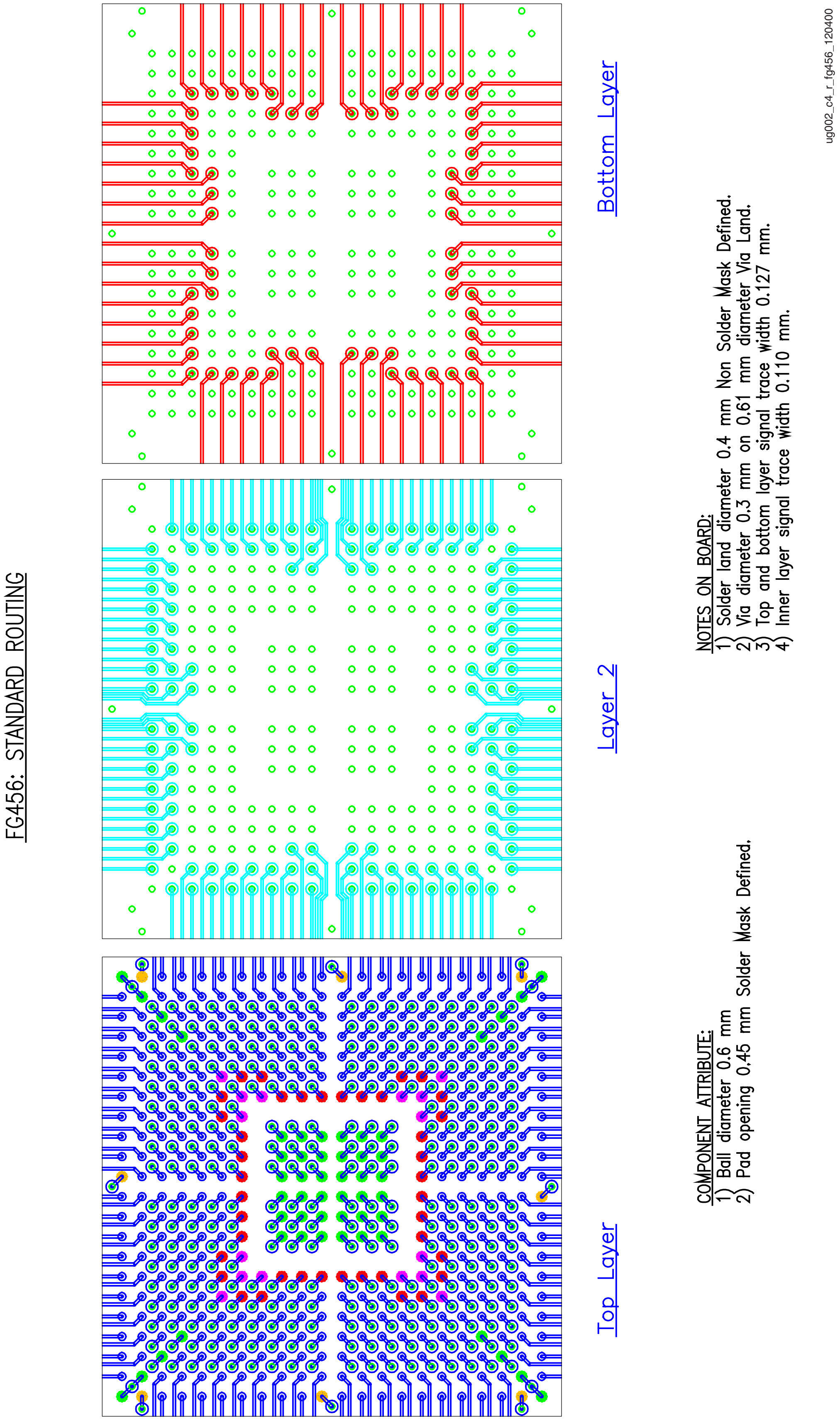
Figure 4-51: **FG256 Routing With LVDS Pairs**



COMPONENT ATTRIBUTE:
1) Ball diameter 0.6 mm
2) Pad opening 0.45 mm Solder Mask Defined.

NOTES ON BOARD:
1) Solder land diameter 0.4 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

Figure 4-52: **FG456 Standard Routing**

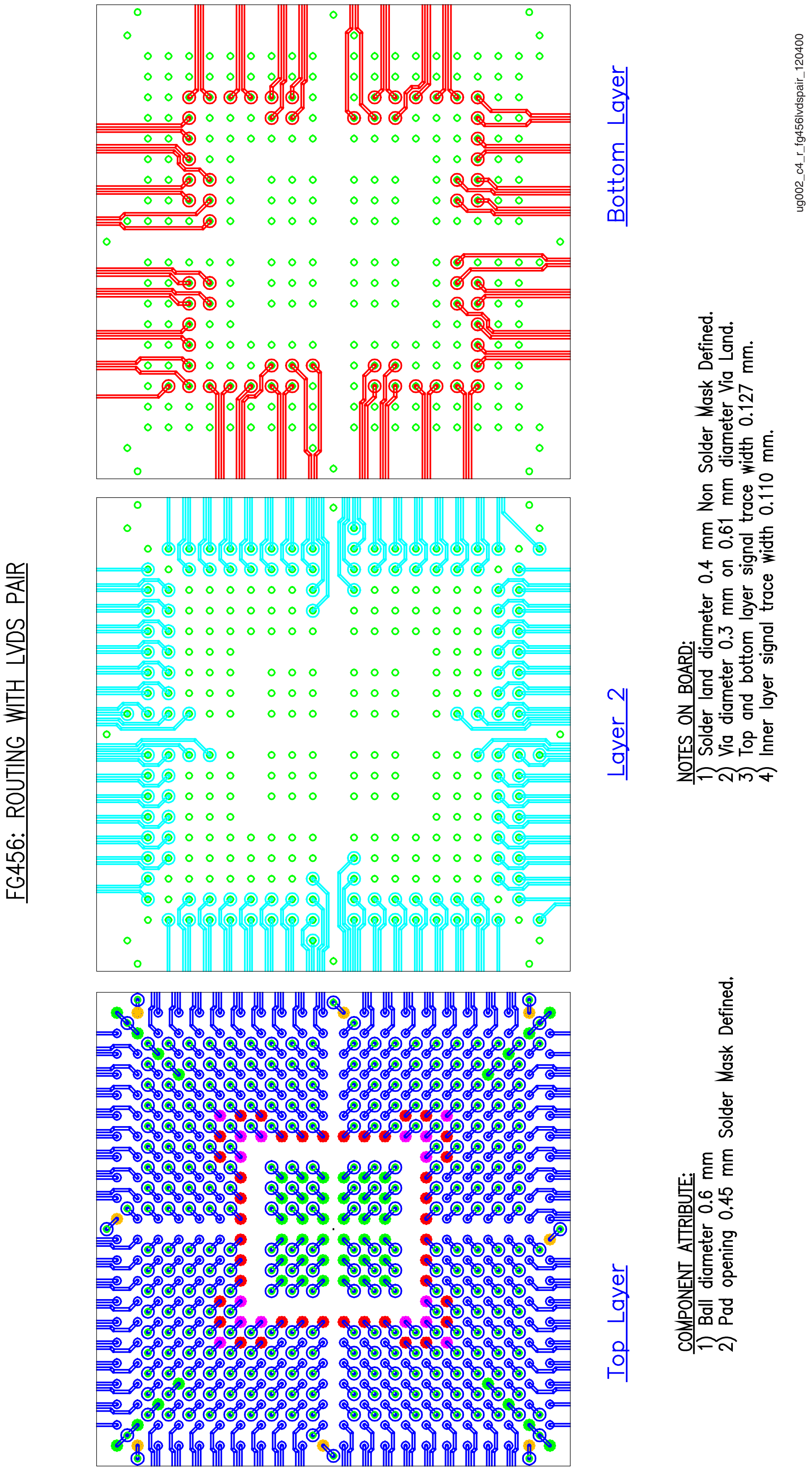
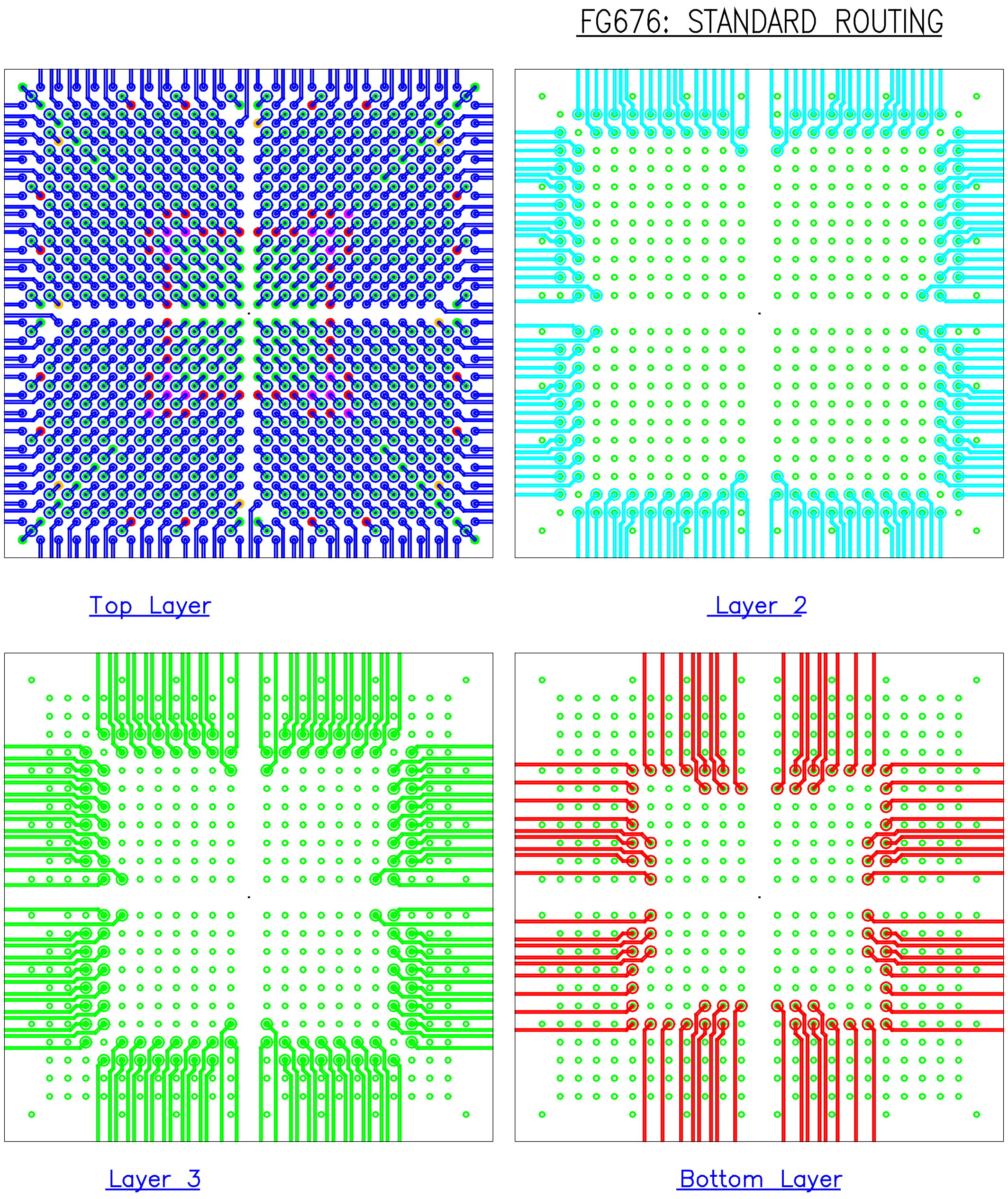


Figure 4-53: **FG456 Routing With LVDS Pairs**



COMPONENT ATTRIBUTE:
1) Ball diameter 0.6 mm
2) Pad opening 0.45 mm Solder Mask Defined.

NOTES ON BOARD:
1) Solder land diameter 0.4 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

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Figure 4-54: **FG676 Standard Routing**

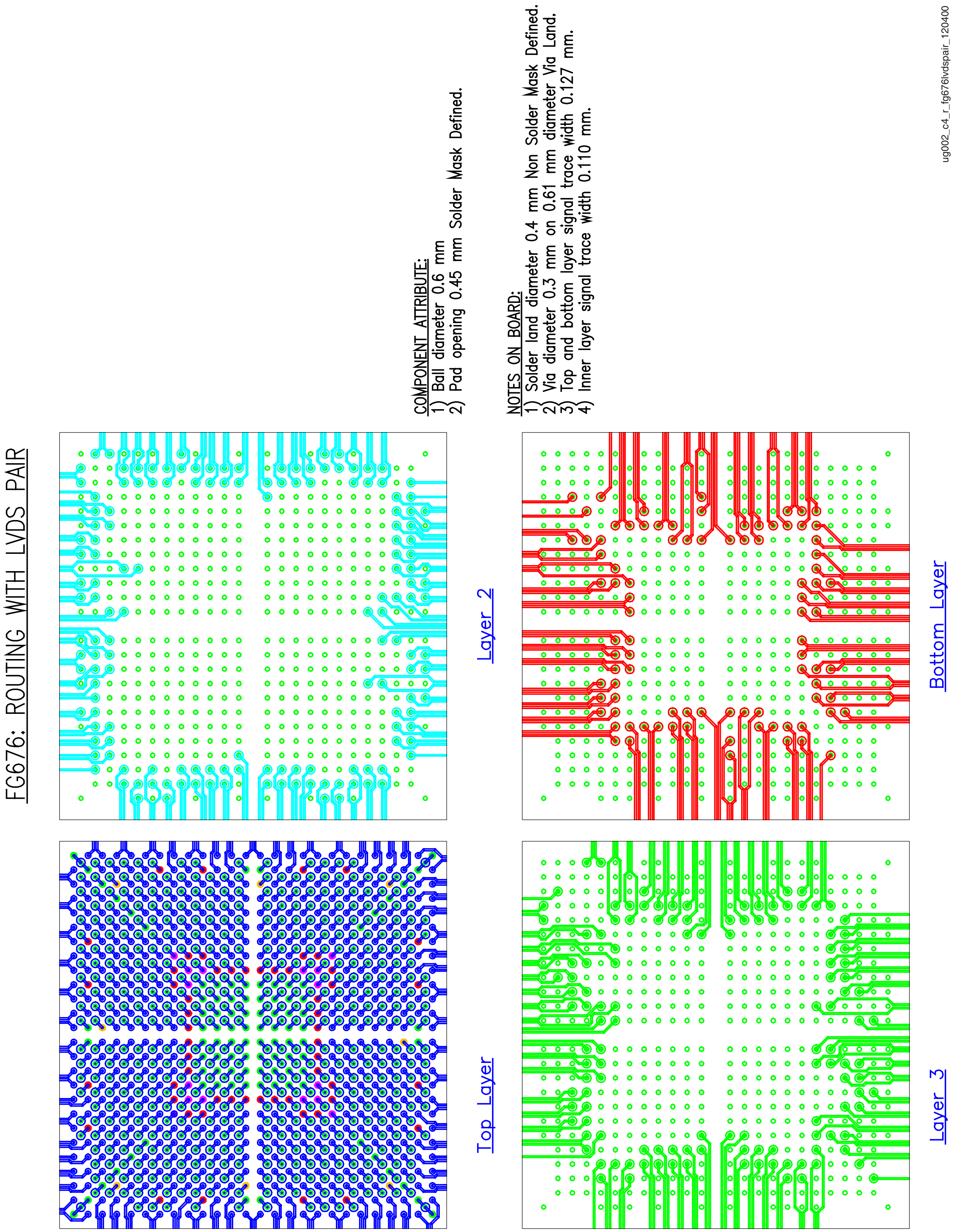


Figure 4-55: **FG676 Routing With LVDS Pairs**

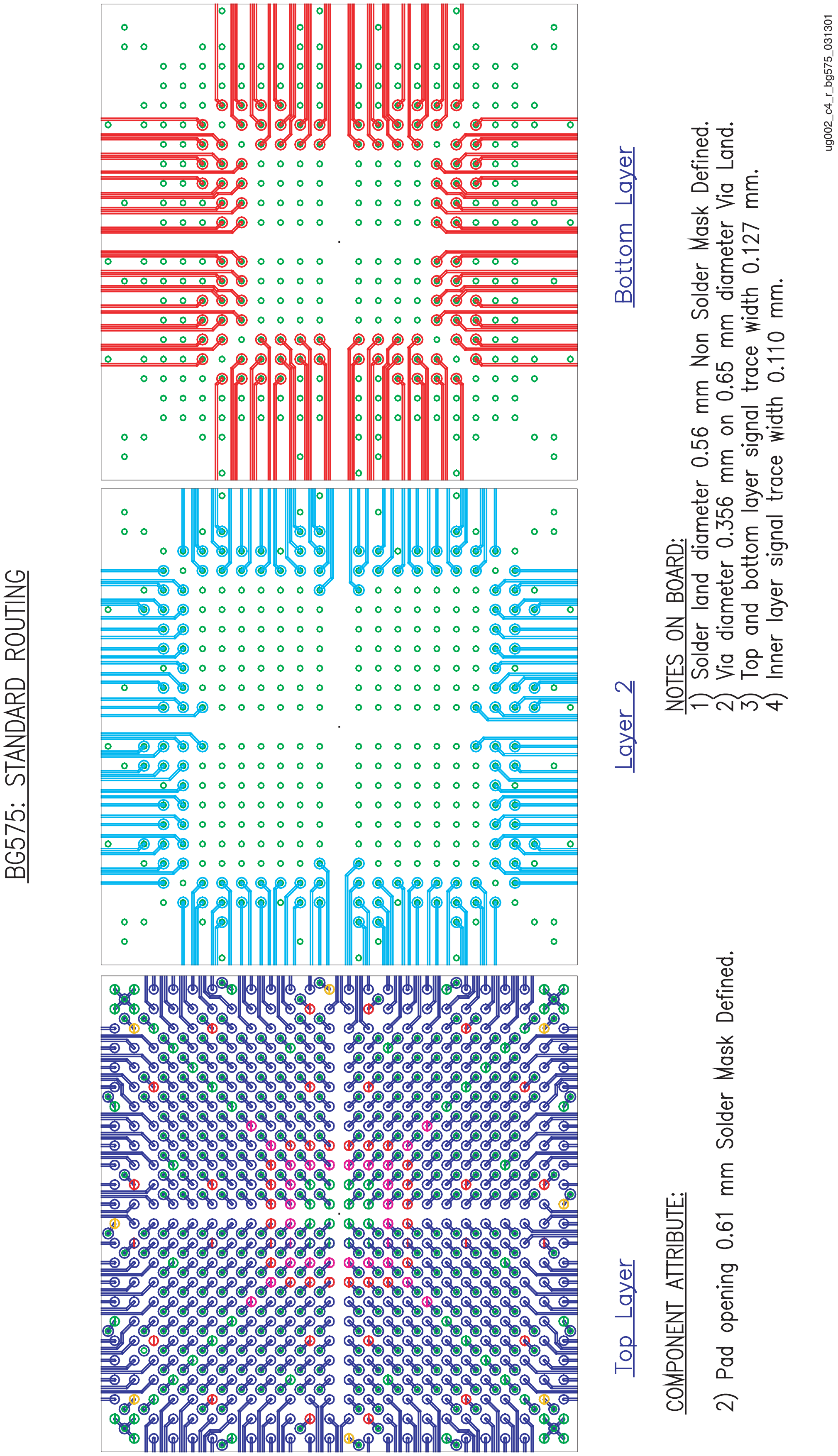


Figure 4-56: **BG575 Standard Routing**

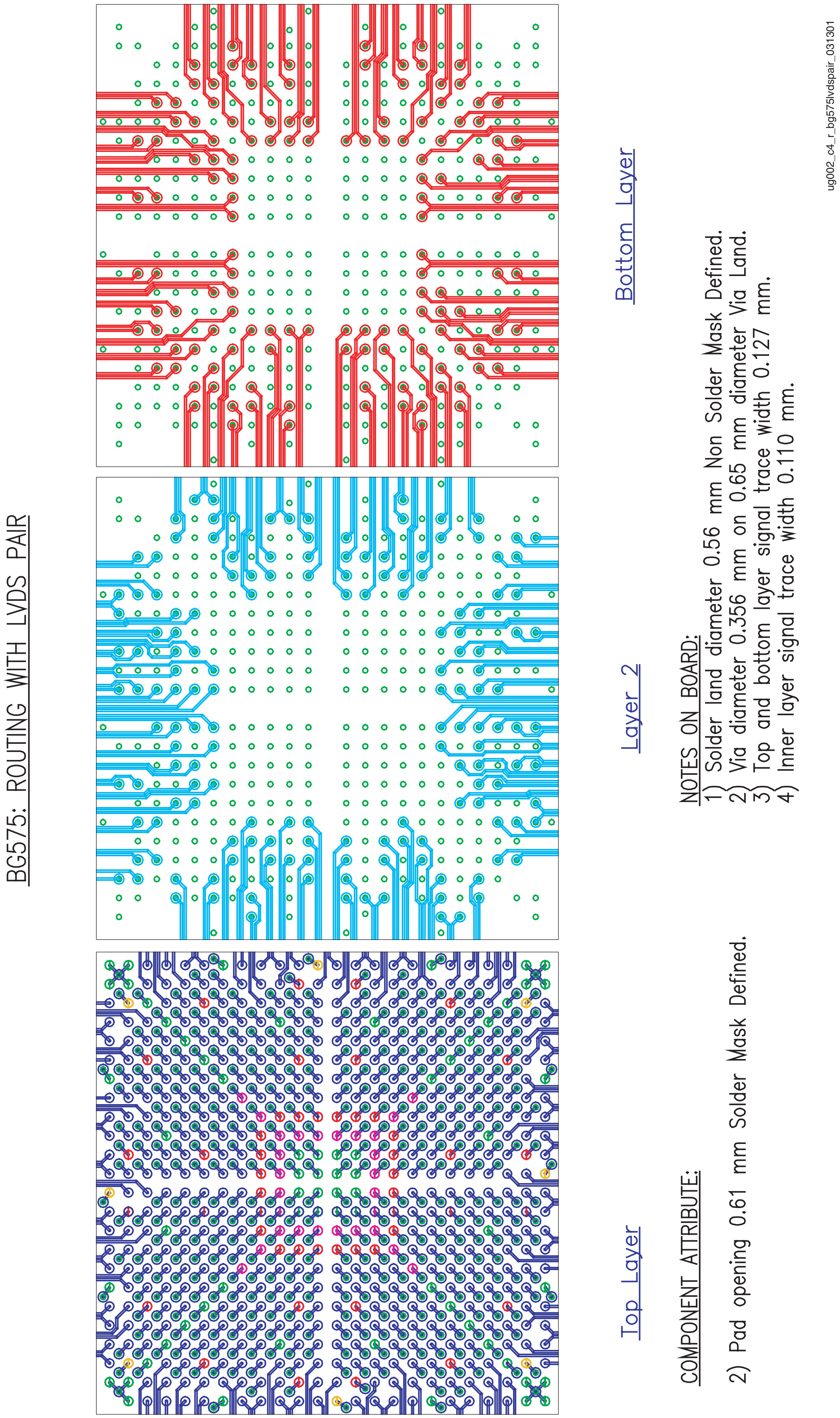
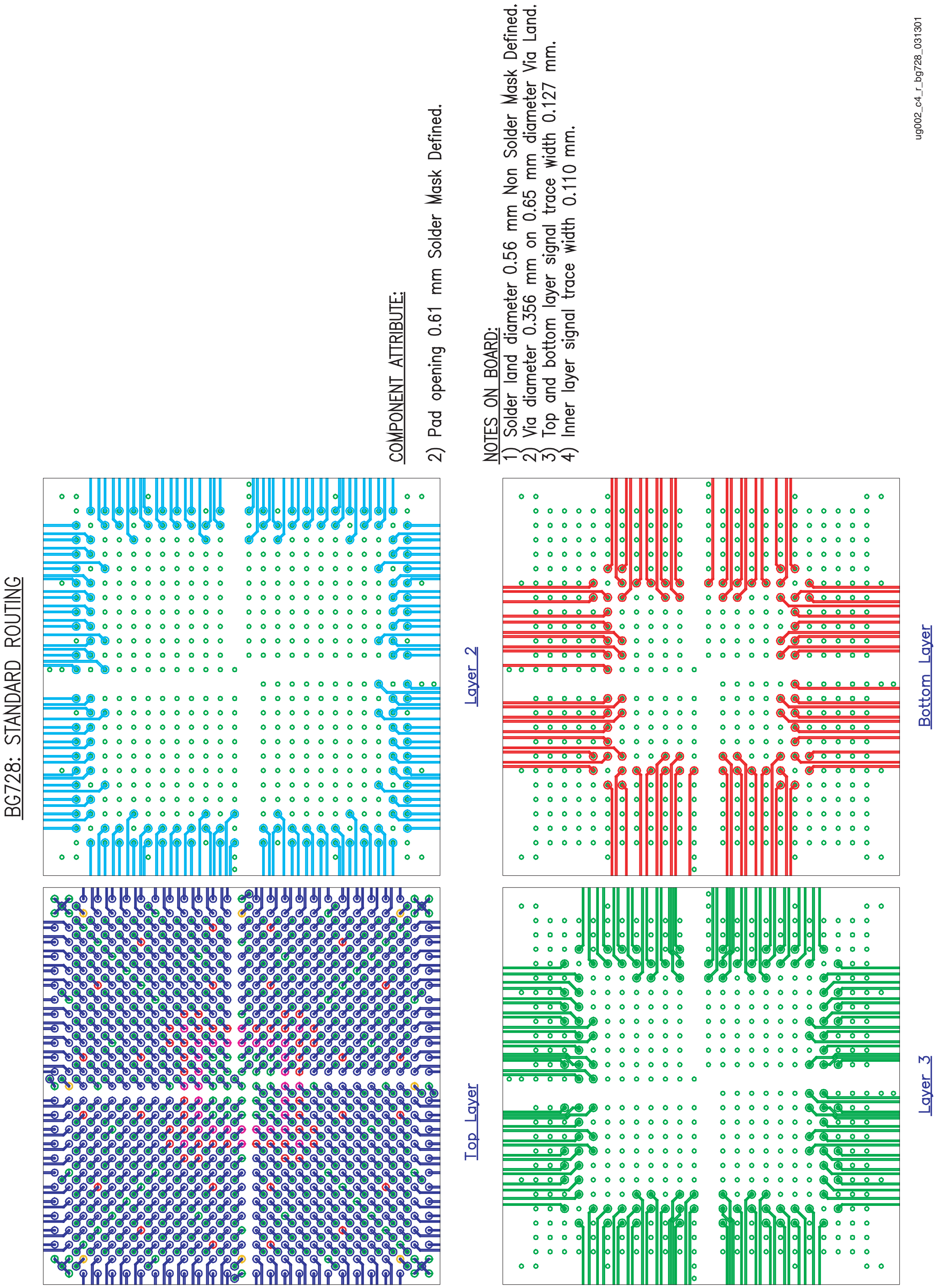


Figure 4-57: **BG575 Routing With LVDS Pairs**



COMPONENT ATTRIBUTE:

2) Pad opening 0.61 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

Figure 4-58: **BG728 Standard Routing**

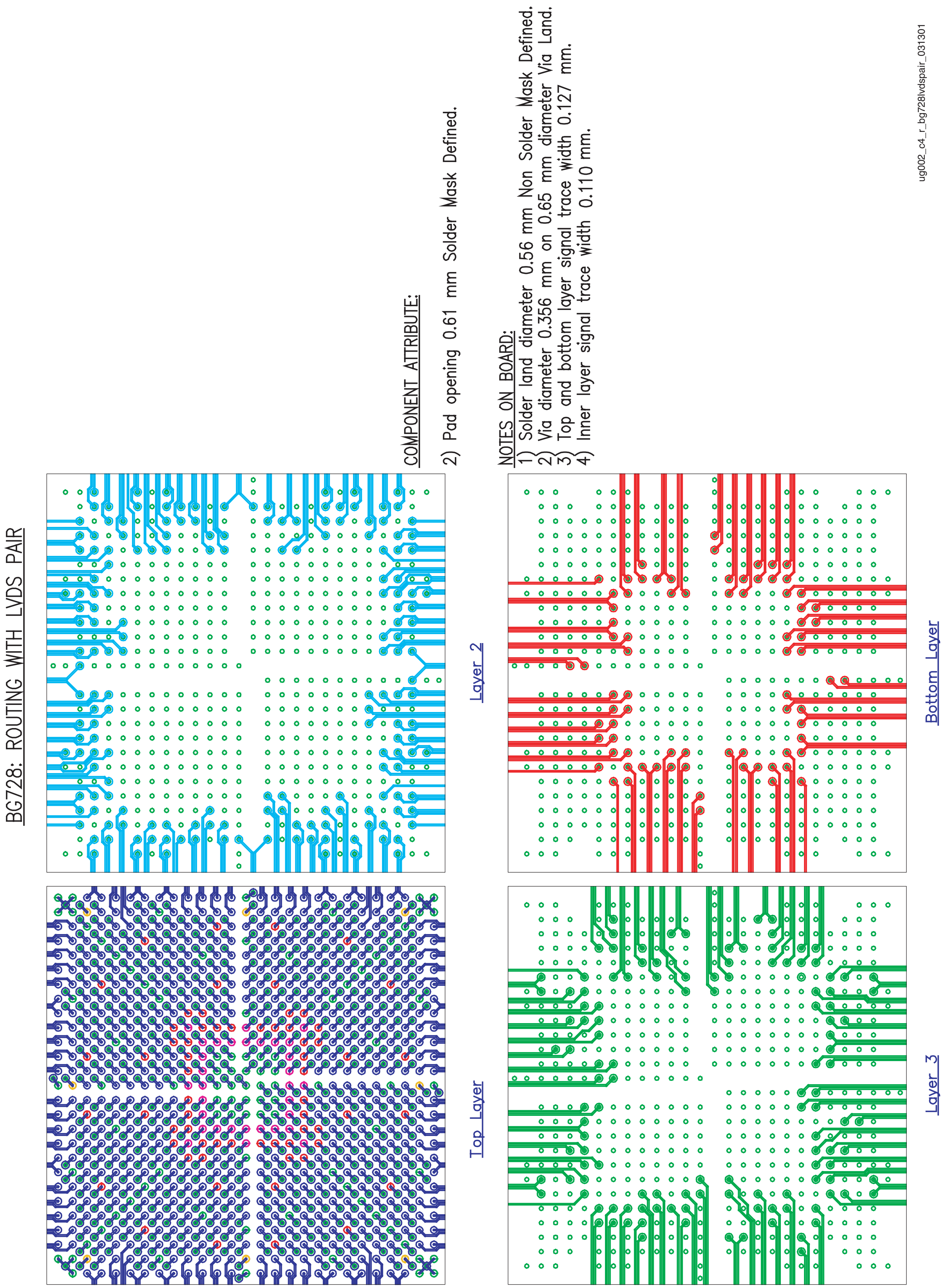


Figure 4-59: **BG728 Routing With LVDS Pairs**

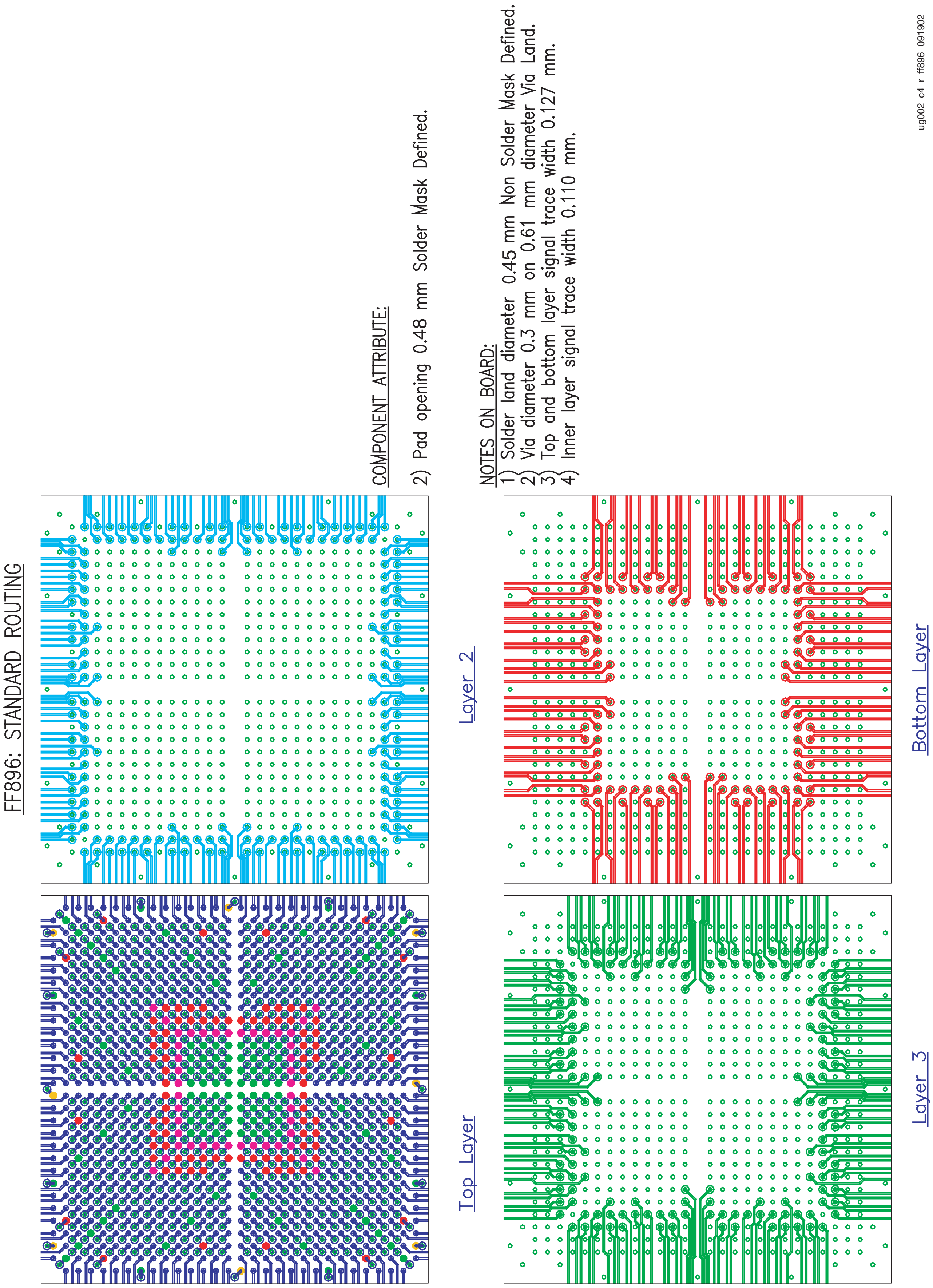
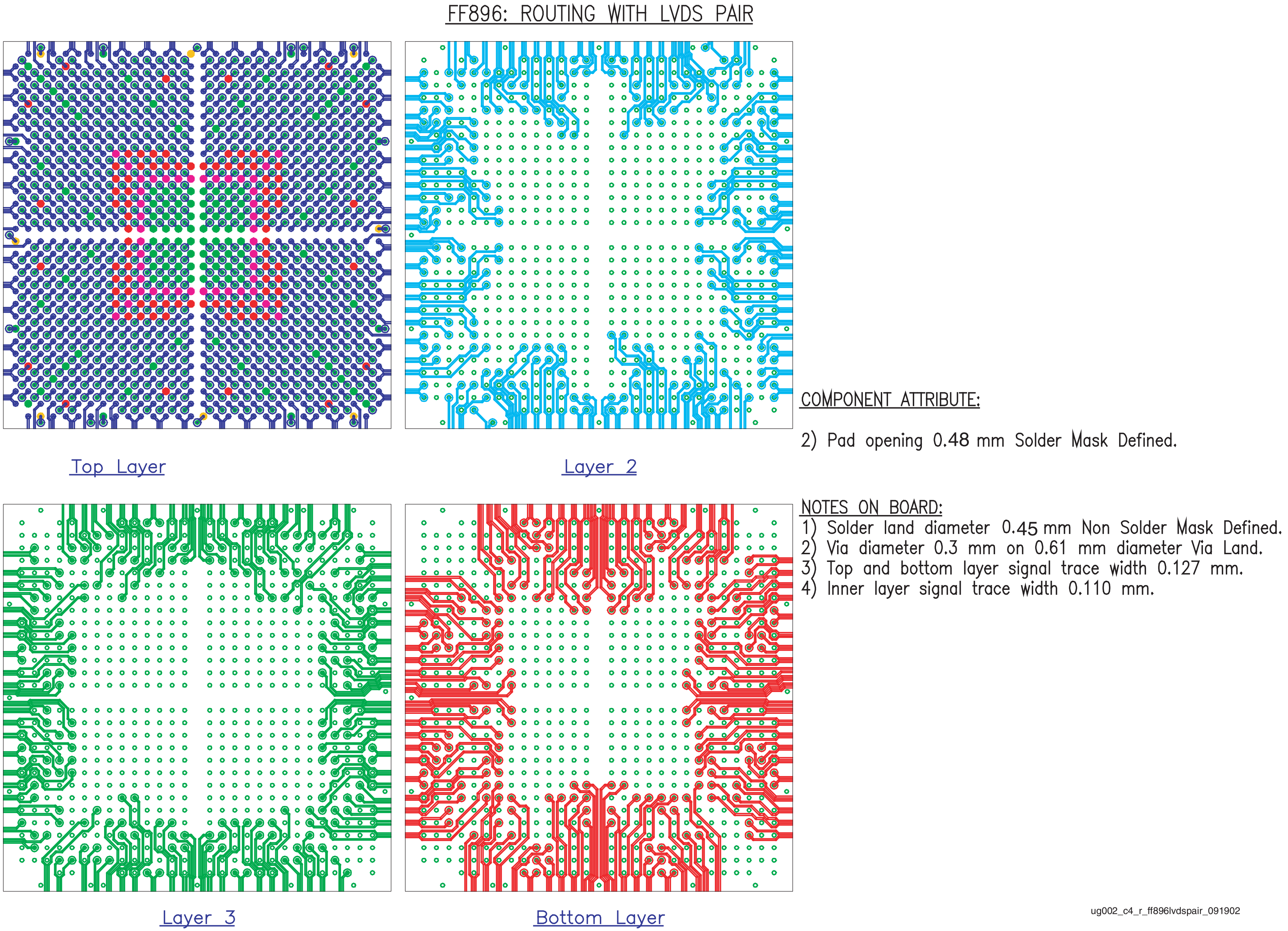


Figure 4-60: **FF896 Standard Routing**



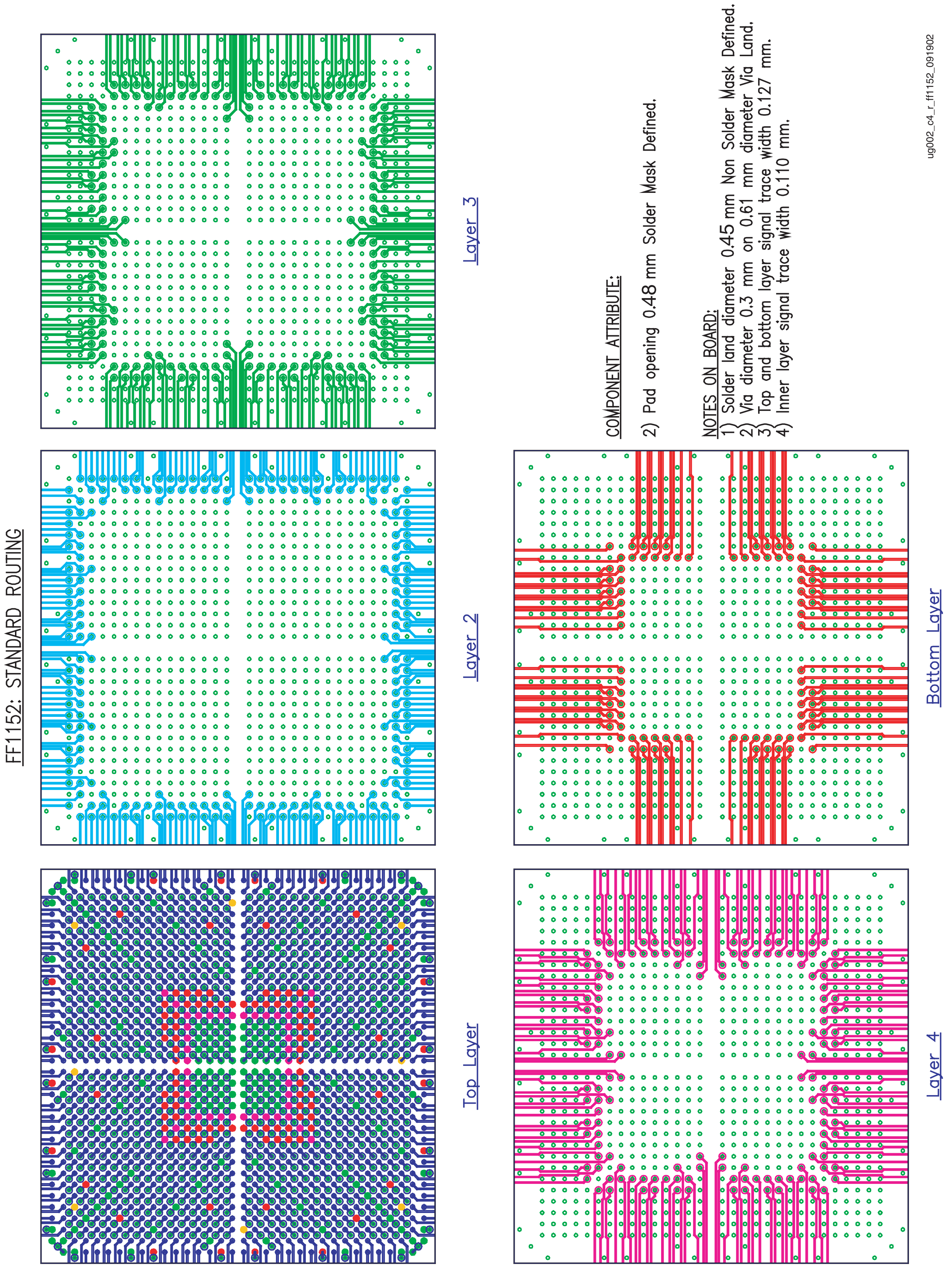
COMPONENT ATTRIBUTE:

2) Pad opening 0.48 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

Figure 4-61: **FF896 Routing With LVDS Pairs**



COMPONENT ATTRIBUTE:

2) Pad opening 0.48 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

Figure 4-62: **FF1152 Standard Routing**

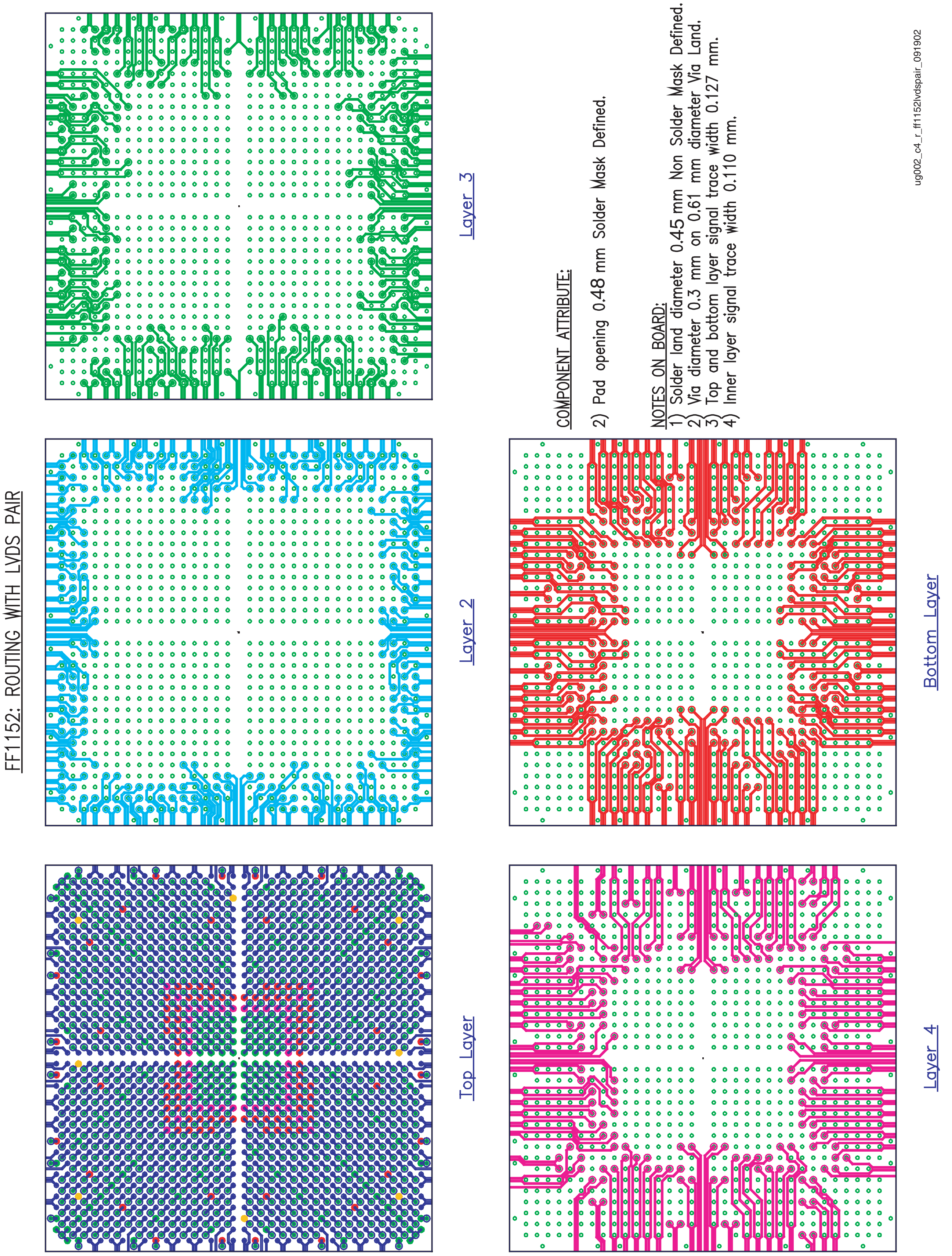


Figure 4-63: **FF1152 Routing With LVDS Pairs**

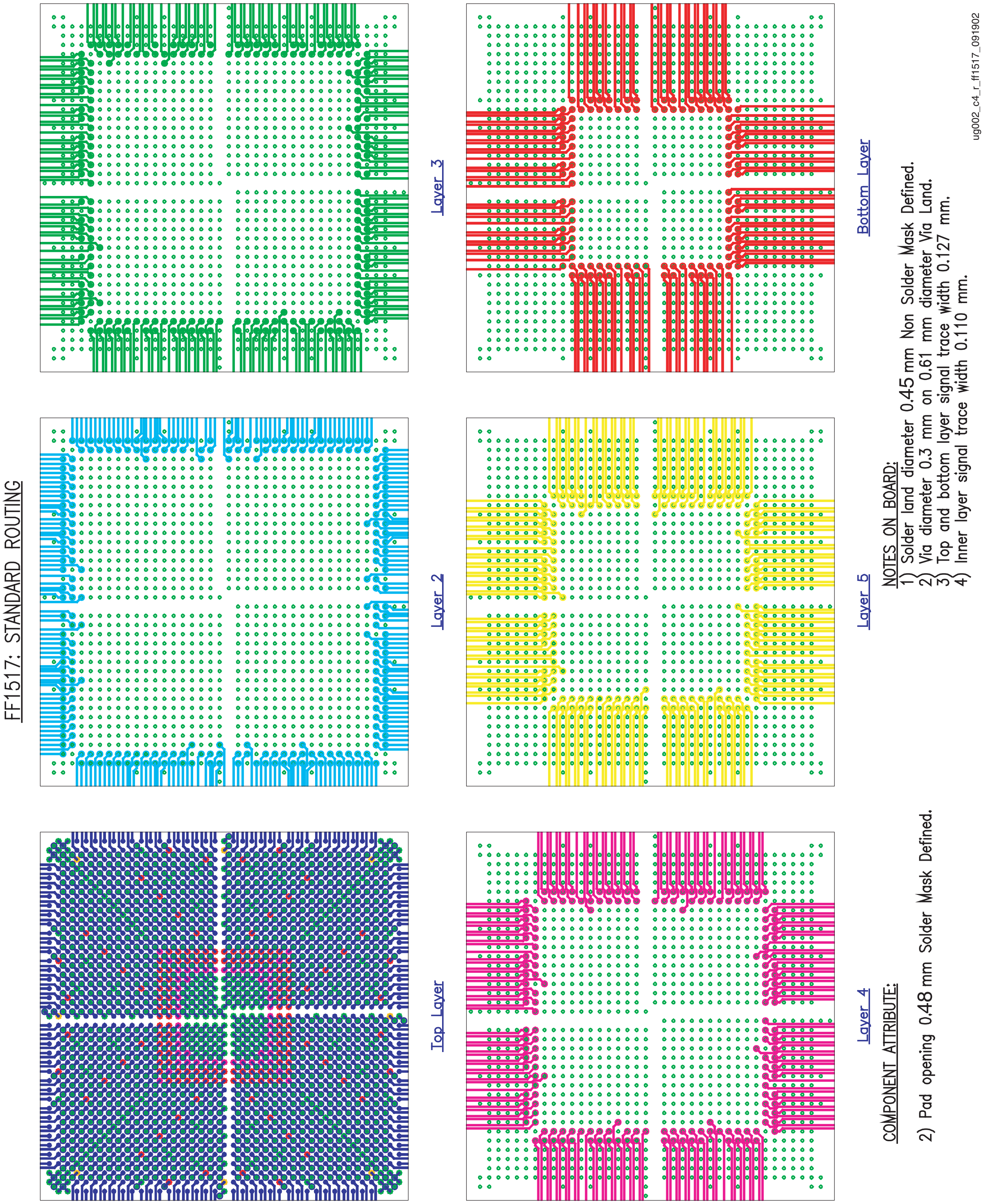
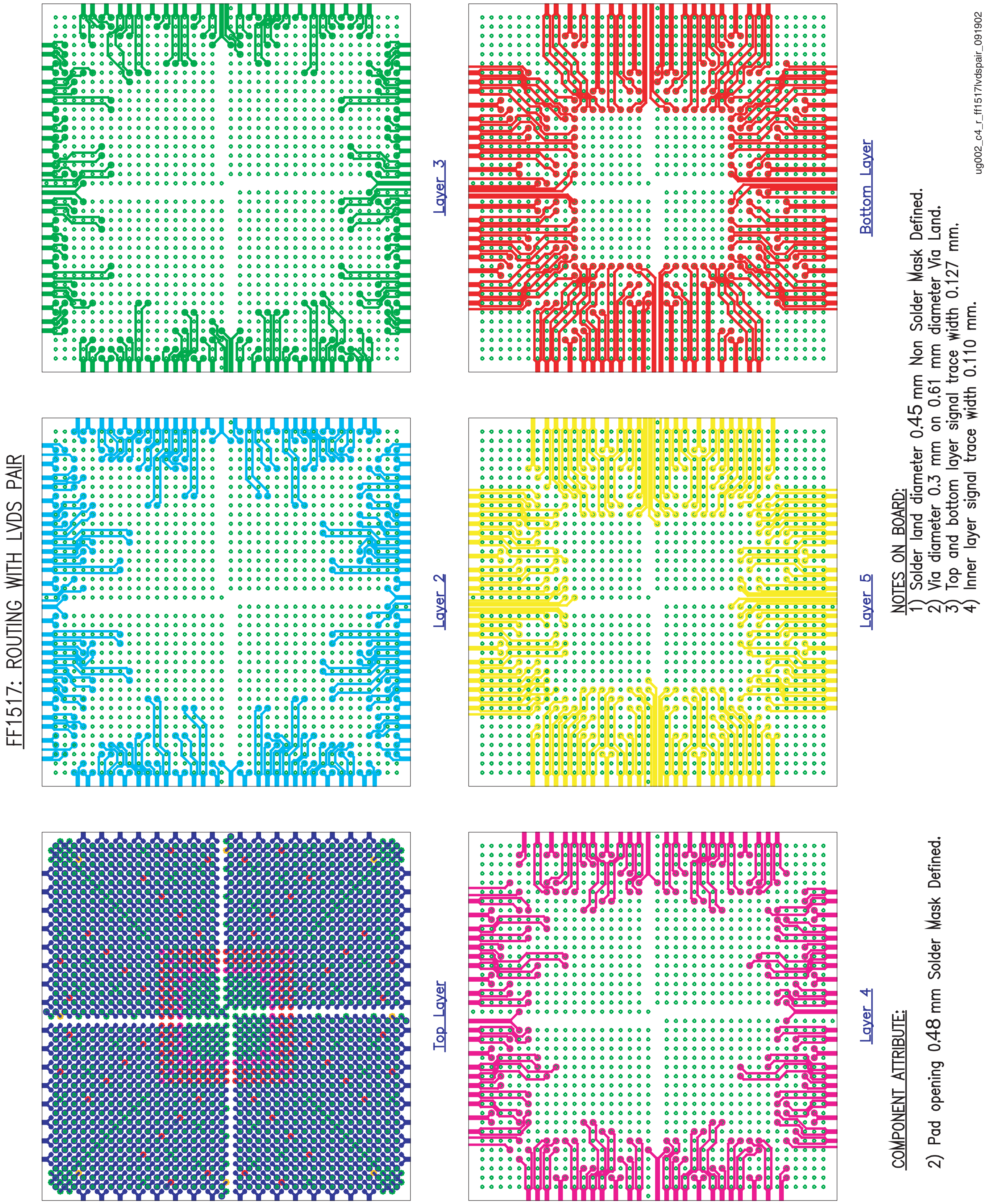


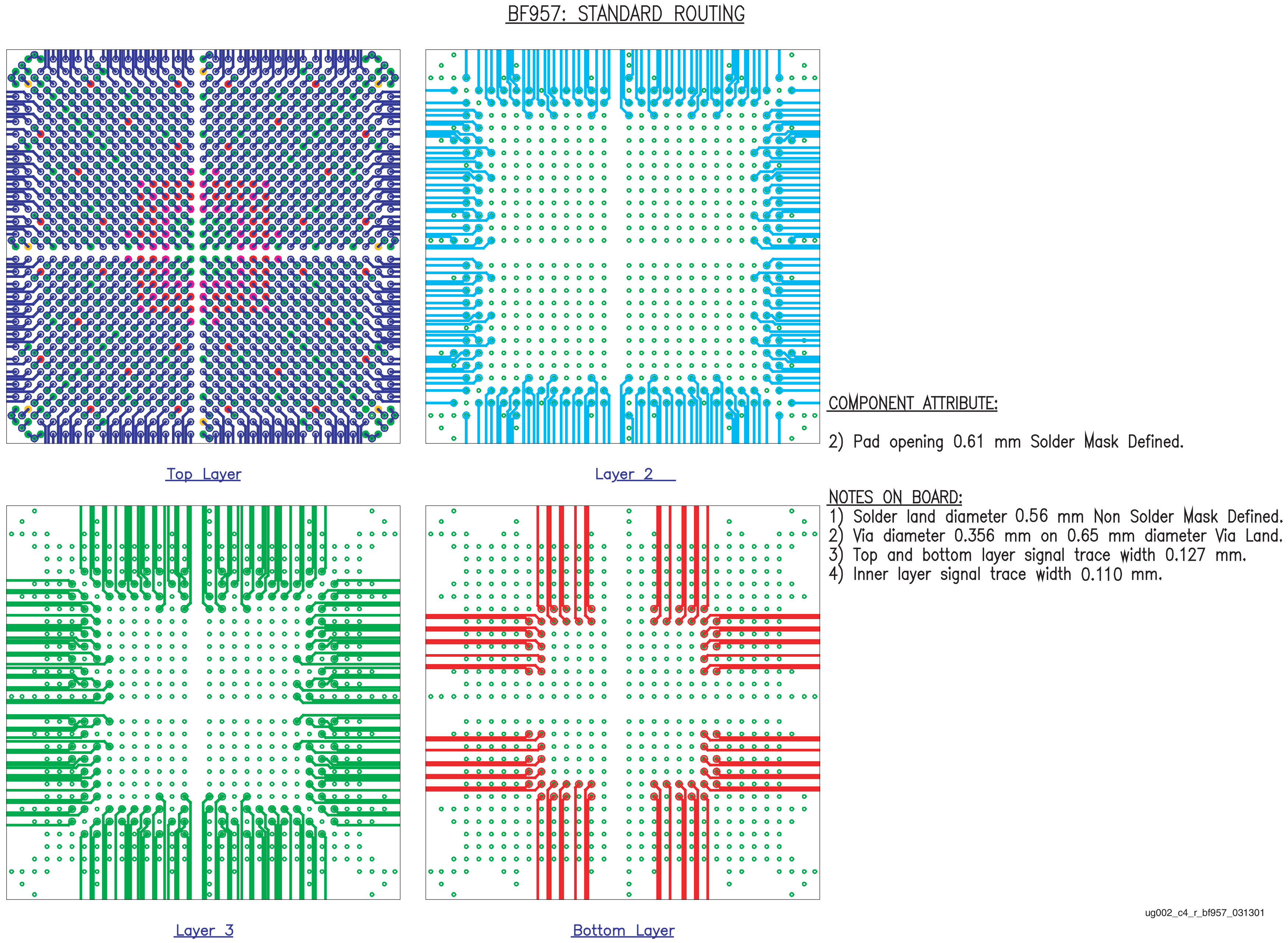
Figure 4-64: **FF1517 Standard Routing**



NOTES ON BOARD:
1) Solder land diameter 0.45 mm Non Solder Mask Defined.
2) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

COMPONENT ATTRIBUTE:
2) Pad opening 0.48 mm Solder Mask Defined.

Figure 4-65: **FF1517 Routing With LVDS Pairs**



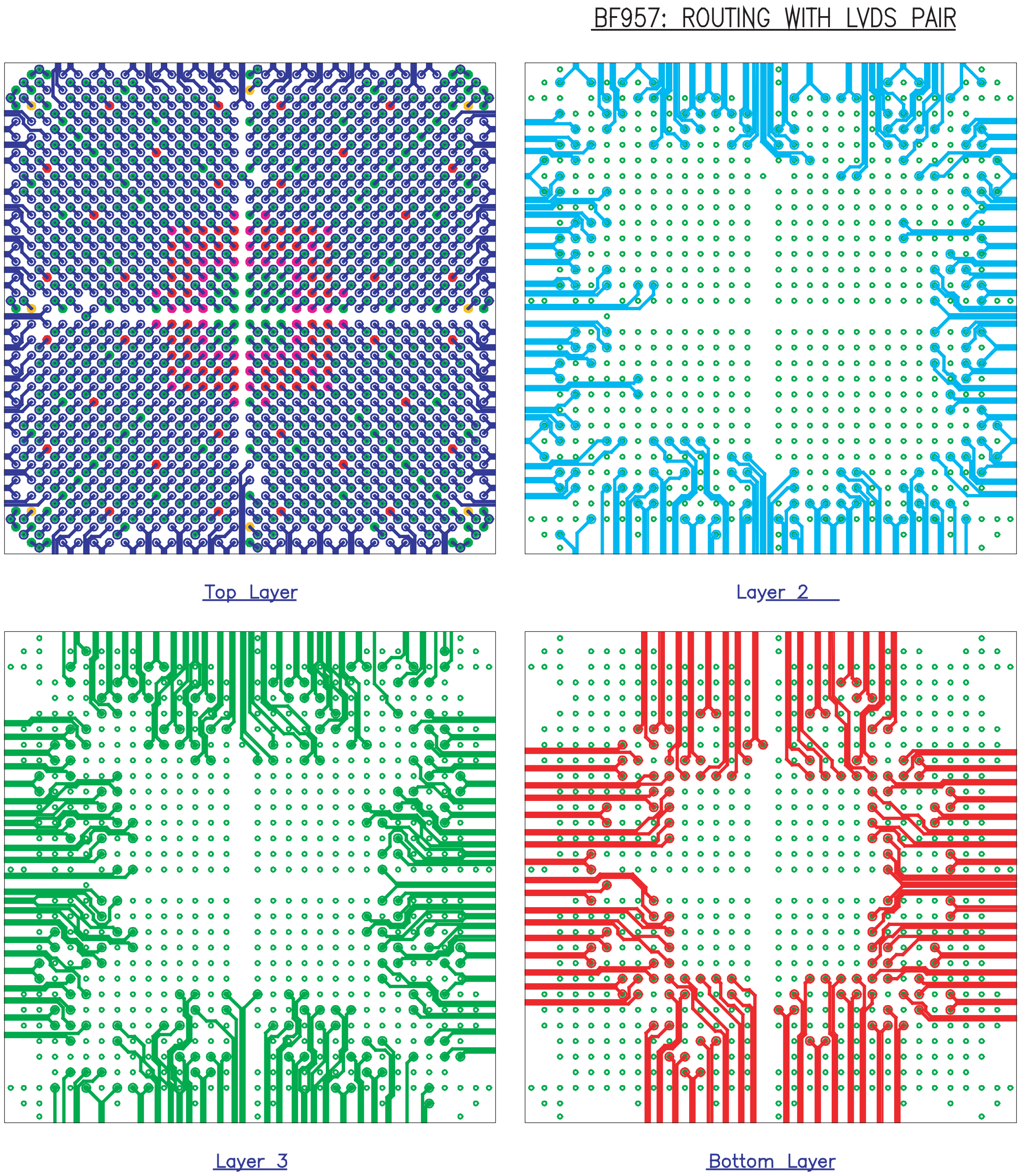
COMPONENT ATTRIBUTE:

2) Pad opening 0.61 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

Figure 4-66: **BF957 Standard Routing**



COMPONENT ATTRIBUTE:

2) Pad opening 0.61 mm Solder Mask Defined.

NOTES ON BOARD:

1) Solder land diameter 0.56 mm Non Solder Mask Defined.
2) Via diameter 0.356 mm on 0.65 mm diameter Via Land.
3) Top and bottom layer signal trace width 0.127 mm.
4) Inner layer signal trace width 0.110 mm.

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Figure 4-67: **BF957 Routing With LVDS Pairs**