CPM – Design & Implementation

Introduction

Subsystems:

- Control
- Readout
- Realtime

Mechanics

Manufacture & Test

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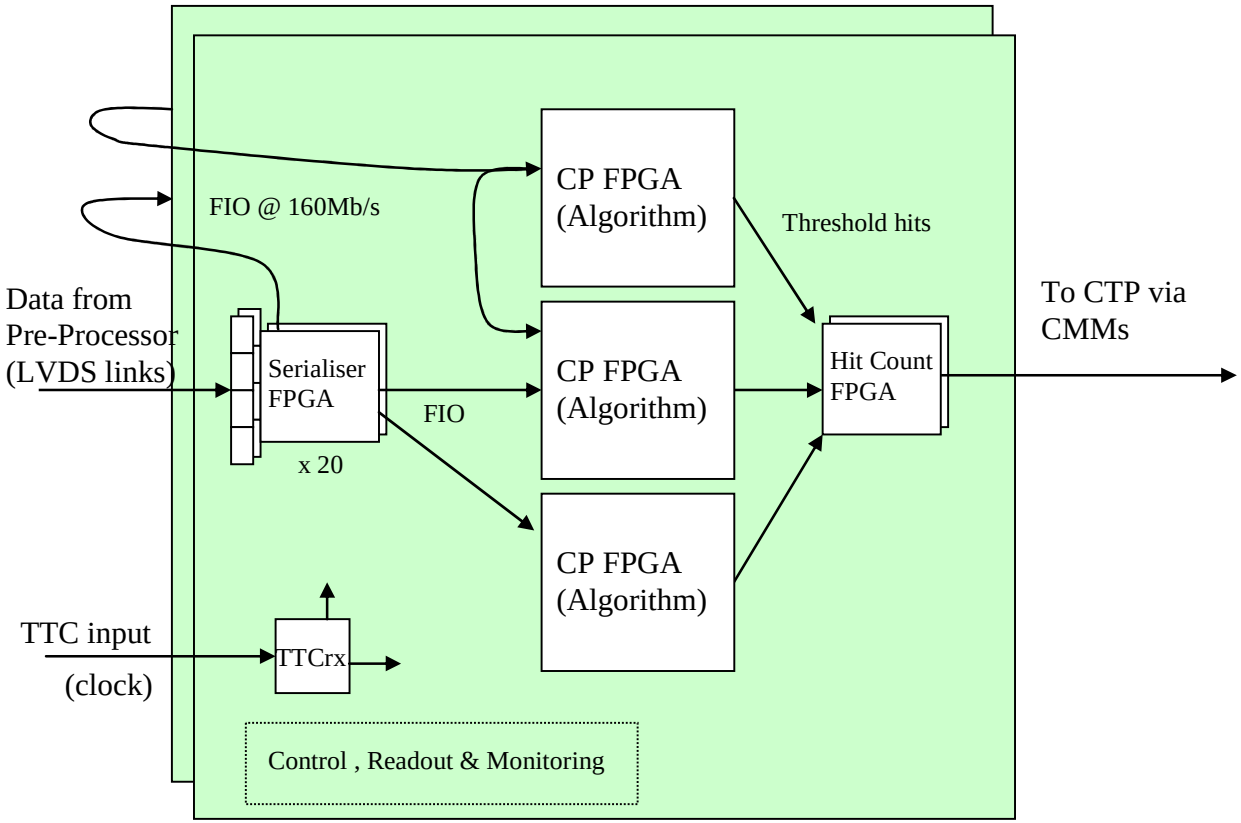
Introduction to CPM

A base for the large CP FPGAs, and the Serialiser FPGAs.

Much simplified diagram of CPM, showing real-time path



R. Staley

Revision history of CPM Design

V1.0 with rev /1 PCB designed to PDR (April 2002) 5 Modules
- Error in CP Chip design for capturing 160Mb/s data
- Poor routing of some FIO signals

V1.5 with rev /2 PCB (August 2003) 2 Modules
+ New layout, much better signal quality
+ Optical readout
- PLLs have excessive clock jitter

V1.9 with rev /3 PCB (March 2004) 2 Modules
+ Better PLLs
+ Equalise FIO transmission delays
+ Removable optics
- VME problem

Compatibility: FPGA Firmware -> successive versions of PCB.

A photograph of the latest version V1.9:

Control.

A subset of VME bus signals. This we call our “VME—“ specification.
A different backplane connector , but electrically equivalent.

VME interface is 3.3V powered – 5V tolerant and compatible with standard VME.

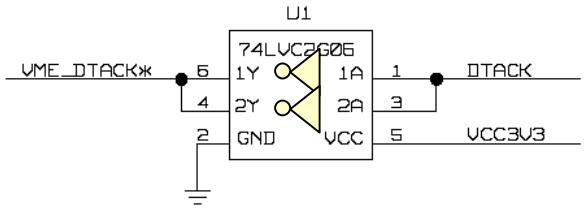
VME operation independent of other functions (such as TTC).

Internal signals are 3.3V LVTTL standard – compatible with 2.5V FPGA I/O and 5V TTL devices, such as FIFOs , FLASH memory, Glink Tx

The internal control bus is sub-divided to fan-out to the large number of FPGAs. This will isolate any problems, and aid fault diagnosis.

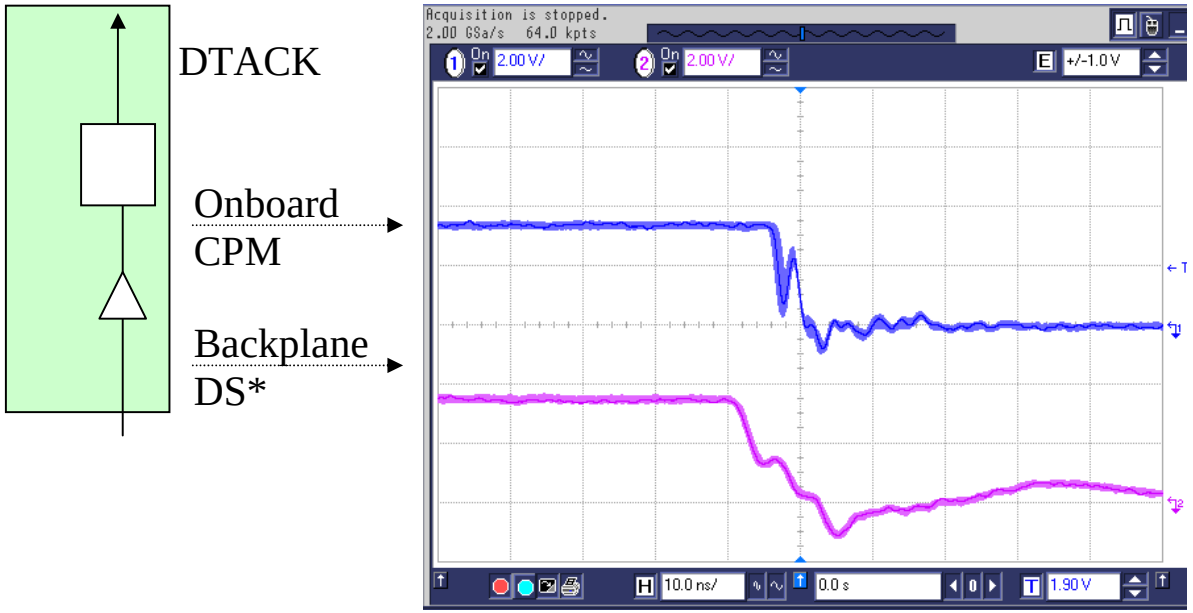
VME DTACK driver must sink 48mA. 3.3V Solution:

A dual 24mA open-drain driver is used, with both halves connected in parallel.



There is an issue with the VME address decoder on the CPM which has only just been understood:

A CPM sometimes will send a very early DTACK* when it or other modules are being addressed.
A poor quality backplane DS* signal is regenerated on the CPM with a 1 – 2ns glitch, causing the DTACK logic to malfunction.



The CPM may be contributing to the degradation of the DS* signal as the problem only appears when 3 or more processors are installed in a crate.
There is a 5cm stub to the DS* line.

This is not just a CPM problem. The design of the crate VME master (VMM) must be part of the solution by using suitable drivers adjacent to the backplane connector.

Further testing is needed. Dummy loads will be fitted to vacant slots so the DS* signal will see the equivalent of a fully loaded crate.

FPGA configuration

Configuration data is held on a FLASH memory, and loaded into the FPGAs using a CPLD based controller.

The FLASH memories are programmed via VME byte-serial.

This circuit has been reliable and stable since V1.0

Design pre-dates the Xilinx SystemACE configuration scheme.

As a precaution, the CPM may now hold 4 different configurations for the CP Chip.

DCS monitoring

A common CAN circuit using Fujitsu uC adopted within the L1 Processor crate.

CAN uC is 5V powered but using 5V CMOS logic levels.
(Translation was overlooked on V1.0. The Geographical Address was unavailable)

The front panel RS232 connector has been corrected to a plug on V1.9 CPM.

Readout.

Readout data transmitted out of the CPM using a Glink transmitter driving a FO transceiver.

The latest version of PCB now clocks the Glink from an onboard 40MHz XTAL oscillator, giving much less jitter induced errors than the previous synchronous scheme using a TTC derived clock.

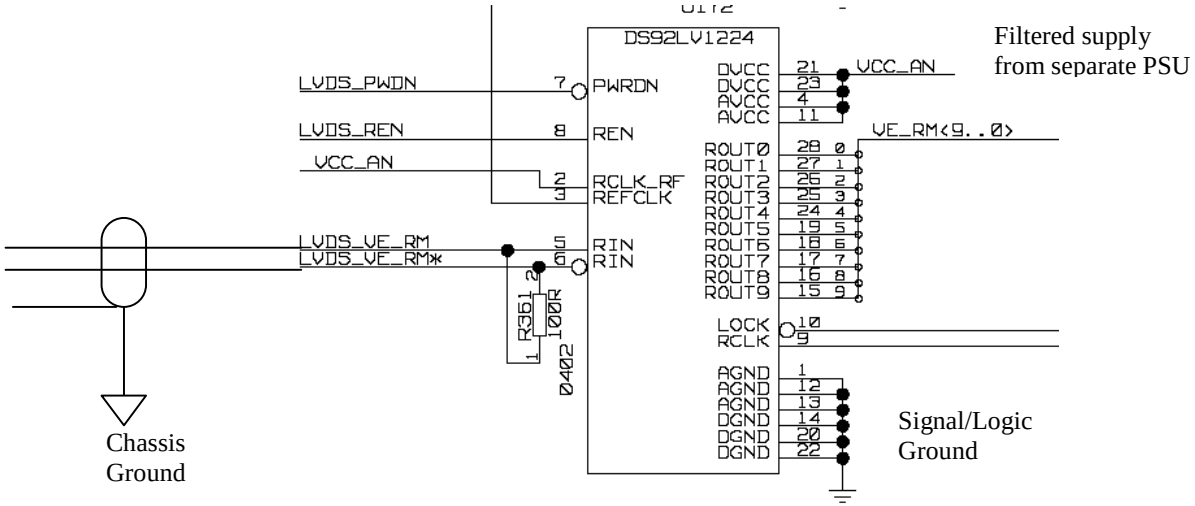
A FIFO within the ROC correctly retimes the data from the modules TTC derived 40.08MHz clock.

The latest PCB uses ‘swappable’ Fibre Optics in the form of SFP package. Reliability estimates give 3 failures during 10 year operation at 30degC.

Realtime data

Data arrives from Pre-Processor over 480Mbaud LVDS links.
These inputs are terminated differentially. (Split termination will introduce noise)

Incoming LVDS cable screens are connected to chassis ground at backplane only, and do not extend onto CPM.



Requirements of receivers (amplitude, jitter etc) -> Pre-Processor specification.

Serialisers fan-out at 160Mb/s.

Onboard signals are on point-to-point series terminated lines. (Simplest termination)

Signals going via backplane to adjacent modules are parallel terminated at destination. On the receiving CPM, the signal visits up to 3 CP chips.
(shown next slide)

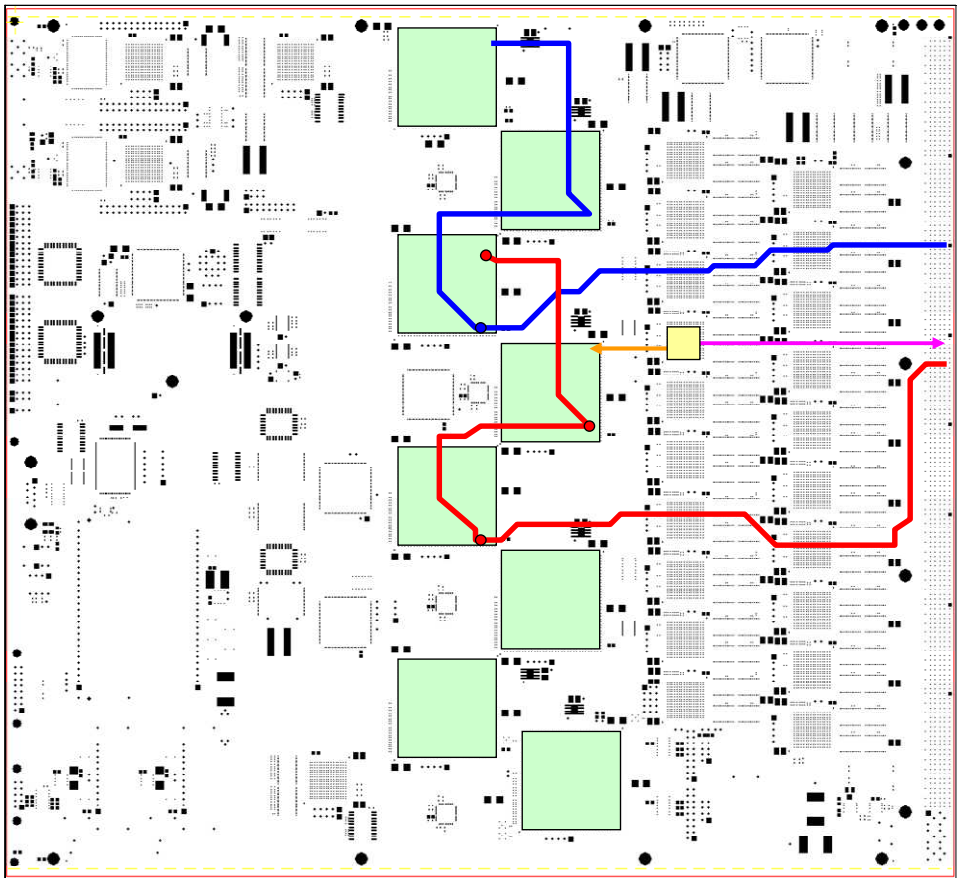
This scheme avoids using fan-out buffers in the area of PCB where the signal density is greatest.

Also, a direct connection between FPGAs allow certain signal levels/standards to be selected by firmware.

Number of FIO tracks:

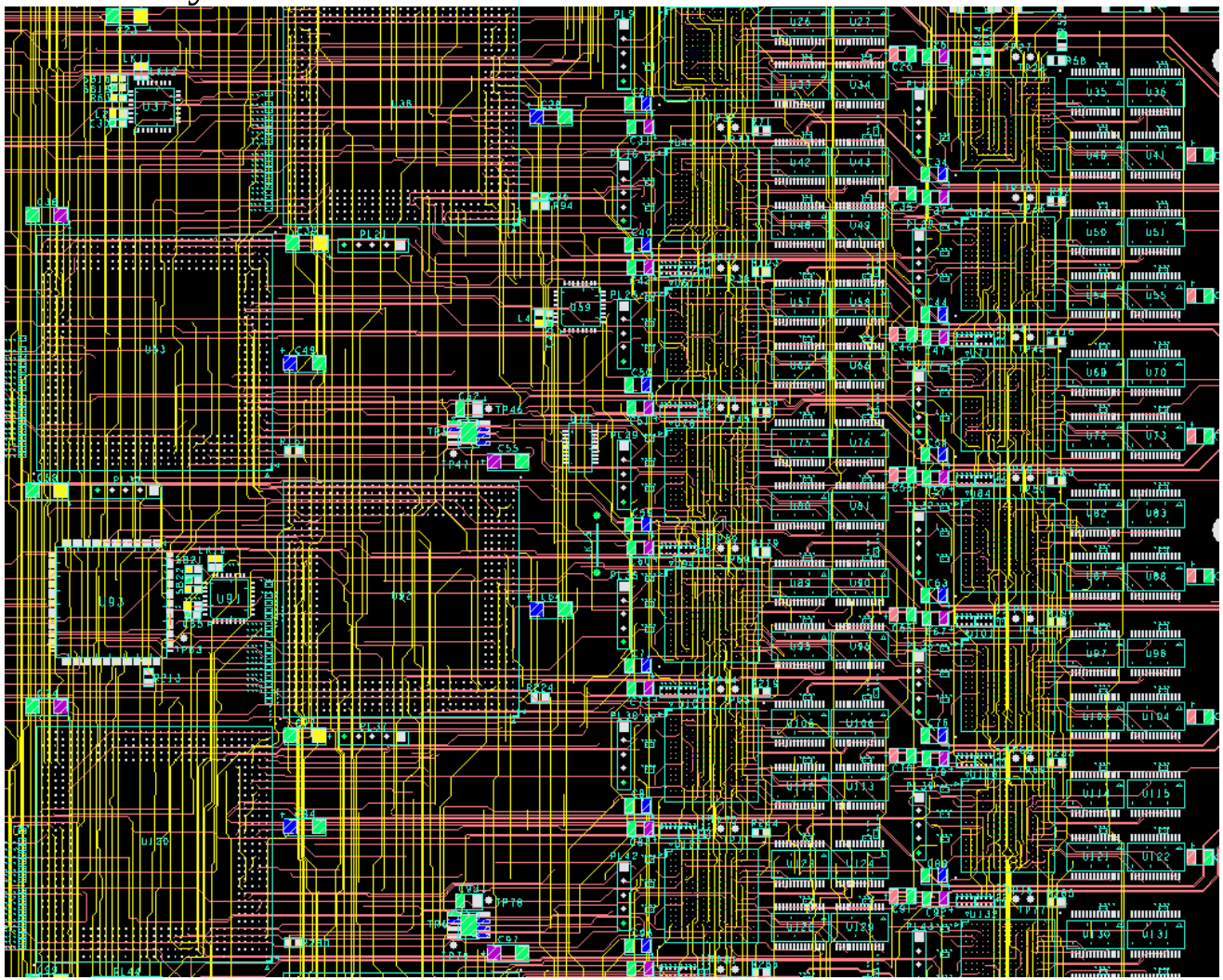
540 onboard.
160 outgoing.
160 incoming.

Typical routing of FIO signal paths:

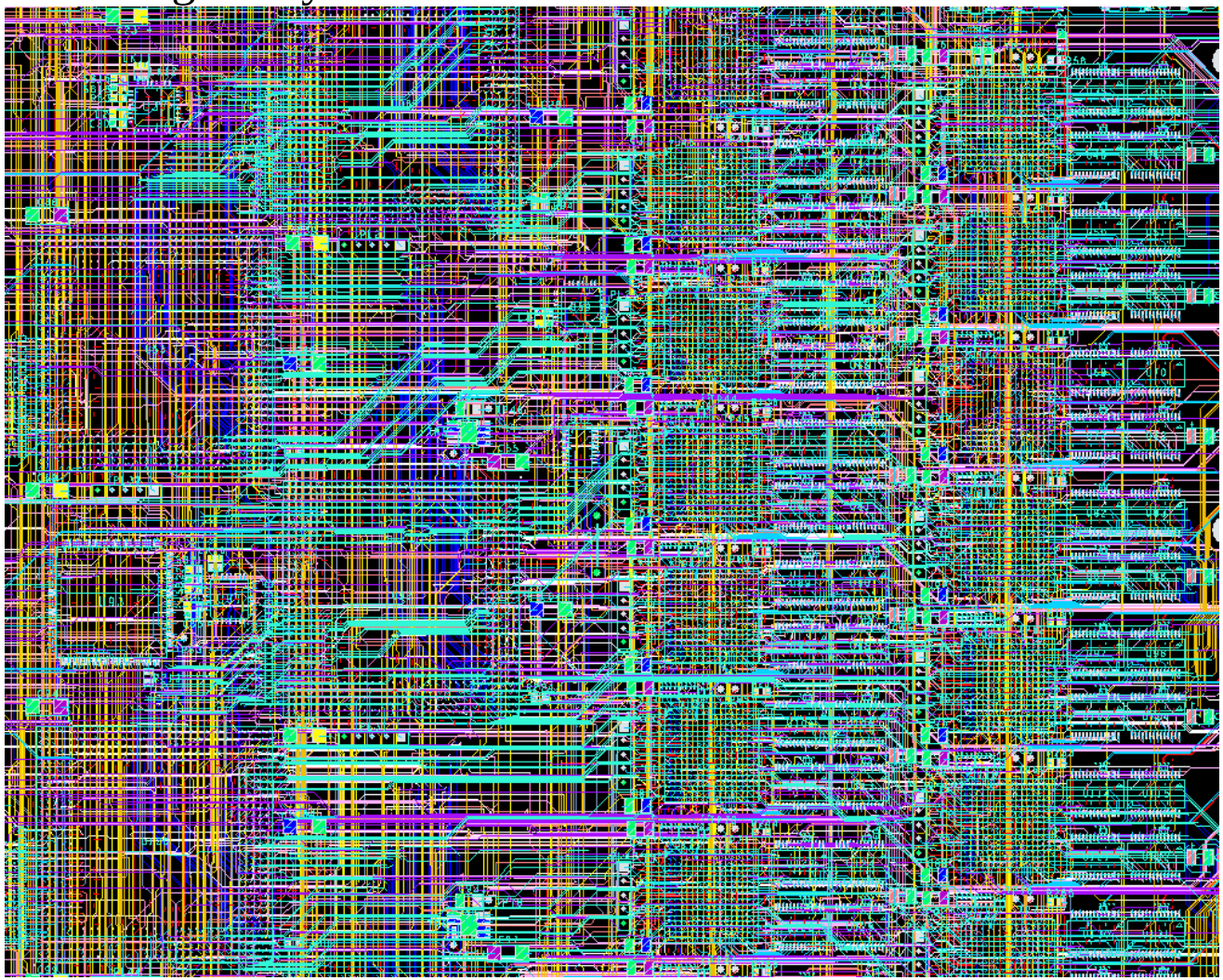


How dense are the tracks? ->

2 inner layers:



All 12 signal layers:



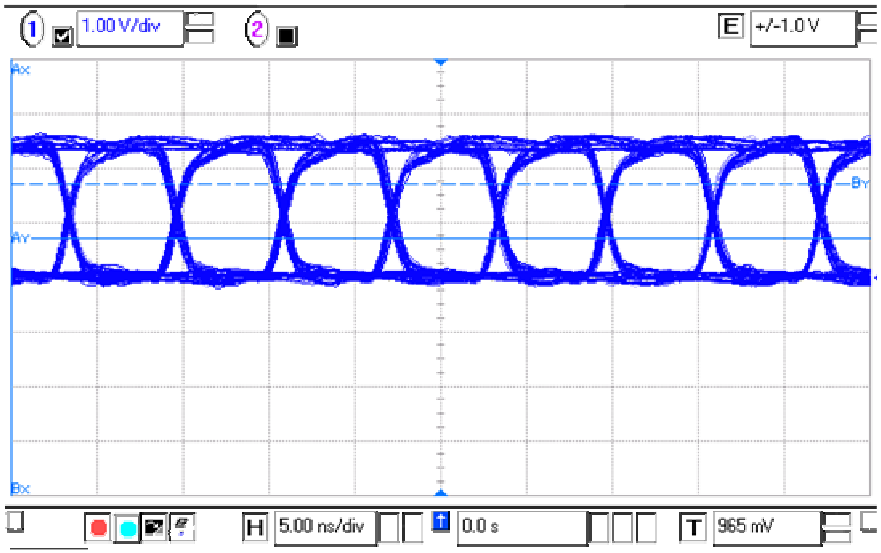
Originally , the CP chip was designed (at RAL) with an automatic circuit that would capture data of any phase, but design was found not to viable with the number of clock resources available to the chosen FPGA.

A re-timing scheme that could be implemented within the FPGA required careful control of the transmission paths.

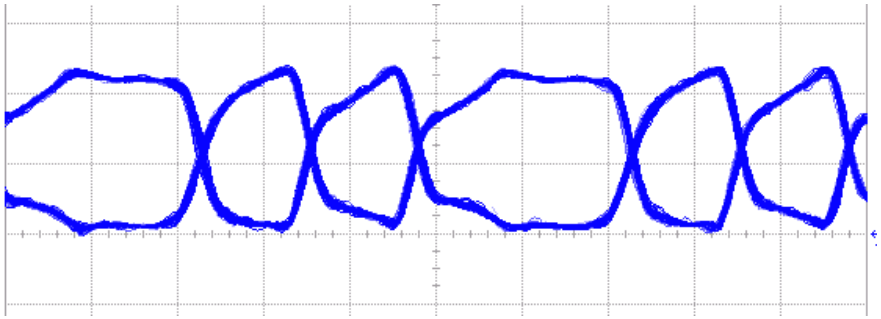
The original PCB /1 had been routed with no particular attention paid to the transmission delays of the FIO data. A re-layout was needed.

The new re-timing scheme also delayed the onboard signals by 3.1 ns within the Serialiser (using inverted bit-clock) so that all data arrives at a CP chip with similar timing. This reduced the clock resources needed by the CP chip to capture the FIO data, from 3 to 2 clock phases.

Signal Quality:



Onboard 160Mb/s FIO link



160Mb/s FIO from Backplane

Controlled impedance tracks are used where necessary, 55 ohms single-ended transmission , and 100 ohms differential. There are about 1000 signals that have to be regarded as transmission lines, with correct termination.

Incoming FIO signals are terminated to a fixed voltage (Vtt = 1.25V).
Vtt generator must be able to sink and source current.

On version 1.0 of CPM, Vtt was centrally generated , peak demand of +/- 3.2A
Stability problems of custom circuit prompted a re-think.

A commercial alternative appeared so for later versions of CPM, and Vtt generation is shared amongst a number of parts distributed close to the CP chips.

These devices also provide the Vref voltages to the CP chip for receiving SSTL2 signals.
Why SSTL2? Reduced switching noise. Large number of FIO signals at 20mA each could add up to 10A if switching together. SSTL2 = +/- 8 mA.

Threshold Hit Counting FPGAs.

Basically combinatorial adder circuits (+ retiming)

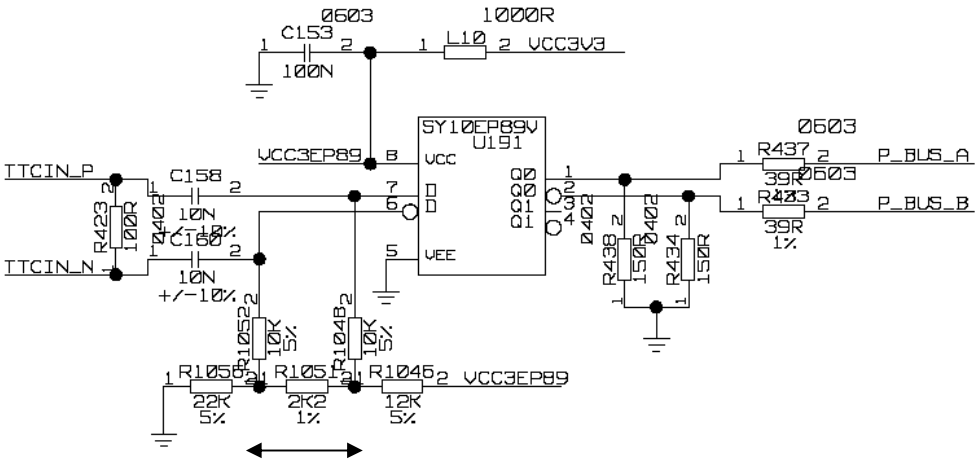
For the latest revision (V1.9) a VME interface was added to the Hit Counting FPGA, solely for diagnostic purposes, not needed for real-time running.

TTC

TTC signal from backplane is terminated, then capacitively coupled into a differential repeater that drives this signal across the module to the TTCdec.
The AC coupling is to allow this receiver to work with the present TCM signals that use 5V PECL drivers. LF cut-off frequency is 1.6 kHz.

Prototype TCM
5V PECL

Production TCM
3.3V LVPECL



TTC commands are decoded by a small FPGA (ALTERA EP1K10)
Used to start and stop the playback memory during testing.

This FPGA provides an I2C interface between VME and TTCrx.
Used to set the clock phases for timing scans.

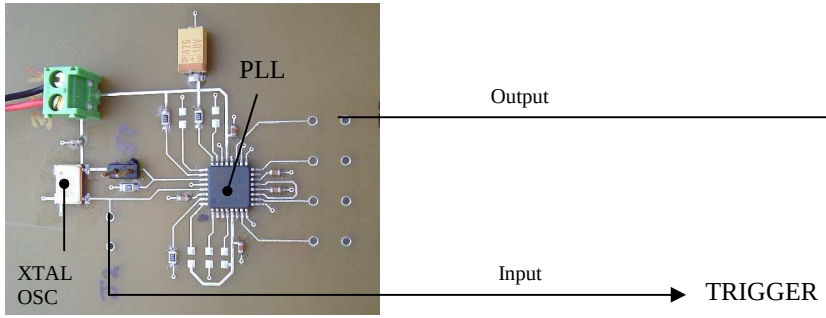
The I2C interface is very robust, used on V1.0 and later.

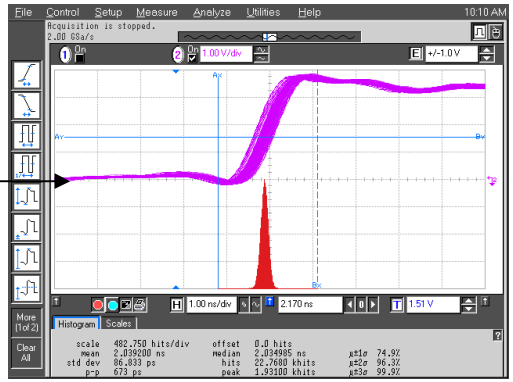
Clock Distribution.

Clocks from TTCrx are distributed using low skew buffers and low jitter PLLs.

Parallel Clocks are distributed with equal delays using ‘Serpentine’ routing to lengthen the shorter tracks. (V1.5 CPM & later)

High levels of ‘absolute’ jitter (> 600ps p-p) were found on the PLLs used on V1.5 CPM. A test PCB was made to evaluate a number of devices:





ABSOLUTE Jitter

637 ps p-p

Cycle-cycle jitter is the usual characteristic listed in datasheets.

The original IDT part was within its specification.

However, absolute jitter is more important to us - many PLLs connected in parallel timing 160Mbps data over backplane.

Part	Cycle to cycle specification ps p-p	Absolute Jitter measurement * ps p-p
IDT IDT5V9950	< 200	637
Cypress CY7B9950	< 100	145

V1.9

* = includes contribution from Crystal Oscillator and Oscilloscope Timebase.

Power supplies

A large number (> 1000) of de-coupling capacitors are allocated to each FPGA.

These are connected directly to power plans (and not device pads) to minimise the series inductance of the connections. Series inductance makes the capacitors ineffective at high frequencies.

Logic & FPGA supplies (3.3V , 2.5V & 1.8V) are internally generated from incoming 5V crate supply as only 3 high current pins available
.
Having switching converters reduces the current taken through the backplane pin.

Voltage and current from each of these 3 converters is monitored by CANuC.

LVDS receivers are powered from an external quiet 3.3V supply, separate from the 5V bus that supplies logic.

All converters are suitably de-coupled and filtered. The onboard voltage converters have current limiting , and fuses in series with their inputs, as does the internal 5V distribution to Glinks etc.

Resettable Poly-fuses are used where possible. When limiting current, a Poly-fuse may reach a temperature 125 deg C. A notice of this is present on PCB (although in very small letters.)

Supply currents and noise – To be re-measured and recorded.

Mechanical

Front panel Ejectors/injectors.

Existing ELMA parts do wear out and even break.

Evaluating All metal parts from TrippleEase. (Their ‘Unbreakable’ range)

Bracing bars.

To be fitted, mounting holes are available.

JTAG

For Manufacturing acceptance tests.

3 JTAG chains – 8 CP chips , 20 Serialisers, 4 other FPGAs and 5 CPLDs.
(Headers use Xilinx X-checker pinout)

Any device not responding to JTAG may be bypassed for diagnostics to continue.

Chains can be accessed through front panel for use in situ:
(Connector uses ALTERA Byteblaster(2) cable pinout)

To Reprogram CPLDs
Run Xilinx Chipscope analyser for diagnostics (missing from /1 PCB)

Not all nets checked through JTAG, ie LVDS receivers -> Serialiser, 960 nets

Manufacture and test.

PCB info:

18 layers

Each layer ½ oz copper - 3 thou tracks

14,000 vias

22,000 solder connections

2,000+ resistors & Capacitors

32 BGA packages

Manufacture and assembly arranged by RAL

1st CPM assembled OK.

2nd and 3rd CPMs had assembly problems with BGAs. (PCBs 11 months old.)

PCB manufacturers / PCB assemblers ‘in conflict’.

Tin vs Gold/Nickel finish…

Thanks to effort by people at RAL , we now use ‘1 stop shop’ companies who guarantee assembly to an agreed standard and meet any cost for re-work.

Company DDI selected - dialogue was very professional.

Examined design and produced a detailed report to improve yield.

Checked the thermal profile of the module to ensure correct soldering temperature for assembly.

X-ray of BGA assemblies.

Last 4 CPMs have been successfully delivered this way:

No BGAs needed re-work (unlike CPMs #2 & #3)

Total of 12 pins on some Quad Flat Packs were unsoldered.

A stray resistor under a package (twice)

On production run , computer vision used to check components.

End of presentation.

Any Questions?