| VME Address | Register name/function | Width | Default | R/W mode |
|---|---|---|---|---|
| Offset + 0 | Version | 12 | 0x041 | Read-only |
| Offset + 2 | Control register | 4 | 0x000 | Read/Write |
| Offset + 4 | Mask out η (eta) / FCAL handling | 5 | 0x000 | Read/Write |
| Offset + 6 | Status register | 8 | 0x03F | Read/Write |
| Offset + 8 | Threshold 0 | 12 | 0x3FF | Read/Write |
| Offset + 10 | Threshold 1 | 12 | 0x3FF | Read/Write |
| \| | \| | | \| | \| |
| Offset + 22 | Threshold 7 | 12 | 0x3FF | Read/Write |
| Offset + 24 | FCAL Threshold 0 | 12 | 0x3FF | Read/Write |
| Offset + 26 | FCAL Threshold 1 | 12 | 0x3FF | Read/Write |
| \| | \| | | \| | \| |
| Offset + 38 | FCAL Threshold 7 | 12 | 0x3FF | Read/Write |
| Offset + 40 | Event delay | 9 | 0x004 | Read/Write |
| Offset + 42 | Reserved | | | |
| Offset + 44 | Maximum orbit counter (from 0 to OrbitCounterMax) | 12 | 0xDEC | Read/Write |
| Offset + 46 | Orbit counter load, at BC_reset | 12 | 0x000 | Read/Write |
| Offset + 48 | DAV space (the gap between two DAVs is DAV_space+1) | 7 | 0x013 | Read/Write |
| Offset + 50 | Spy mode | 7 | 0x000 | Read/Write |
| Offset + 52 | Input spy-memory readout | 10 | | Read-only |
| Offset + 54 | Reset Input spy-memory address | 12 | | Read/Write |
| Offset + 56 | Output spy-memory readout | 10 | | Read-only |
| Offset + 58 | Reset Output spy-memory address | 12 | | Read/Write |
| Offset + 60 | ROC spy-memory readout | 4 | | Read-only |
| Offset + 62 | Reset ROC spy-memory address | 12 | | Read/Write |
| Offset + 64 | Events to read after spy trigger (ROC spy) | 8 | 0x080 | Read/Write |
| Offset + 66 | TTC instruction which trigger spy – Reg 0 | 8 | 0x000 | Read/Write |
| Offset + 68 | TTC instruction which trigger spy – Reg 1 | 8 | 0x000 | Read/Write |
| \| | \| | | \| | \| |
| Offset + 72 | TTC instruction which trigger spy – Reg 3 | 8 | 0x000 | Read/Write |
| Offset + 74 | Received TTC instruction 1 | 8 | 0x000 | Read/Write |
| Offset + 76 | Received TTC instruction 0 | 8 | 0x000 | Read/Write |
| Offset + 78 | Debug register 0 | 12 | 0x000 | Read/Write |
| Offset + 80 | Debug register 1 | 12 | 0x000 | Read/Write |
| Offset + 82 | Debug register 2 | 12 | 0x000 | Read/Write |
| Offset + 84 | Input mask (threshold value) | 12 | 0x000 | Read/Write |

| Bits | Function |
|---|---|

| Version | |
|---|---|
| 0 – 5 | Minor |
| 6 – 11 | Major |

| Control | |
|---|---|
| 0 | Reset FPGA |
| 1 | Start spying |
| 2 | Reset spy memory address |
| 3 | Reset L1A debug unit |

| Mask out η (eta) / FCAL handling | |
|---|---|
| 0 | Mask out column 0 |
| 1 | Mask out column 5 |
| 2 | Mask out column 6 |
| 3 | FCAL left |
| 4 | FCAL right |

| Status register | |
|---|---|
| 0 | DCM_1 locked |
| 1 | DCM_1 flag |
| 2 | DCM_2 locked |
| 3 | DCM_2 flag |
| 4 | G-Link locked |
| 5 | G-Link flag |
| 6 | Detected FCAL left |
| 7 | Detected FCAL right |

| Threshold / FCAL Threshold | |
|---|---|
| 0 – 9 | Threshold value |
| 10 – 11 | Cluster size |

| Spy mode | |
|---|---|
| 0 | Input spy mode |
| 1 | Enable Input spy |
| 2 | Output spy mode |
| 3 | Enable Output spy |
| 4 | ROC spy mode |
| 5 | Enable ROC spy |
| 6 | Trigger on L1A |

| |
|---|
| Controlling |
| Jet algorithm |
| ROC |
| Spy control |
| TTC for spying |
| TTC recording |
| Debug register |