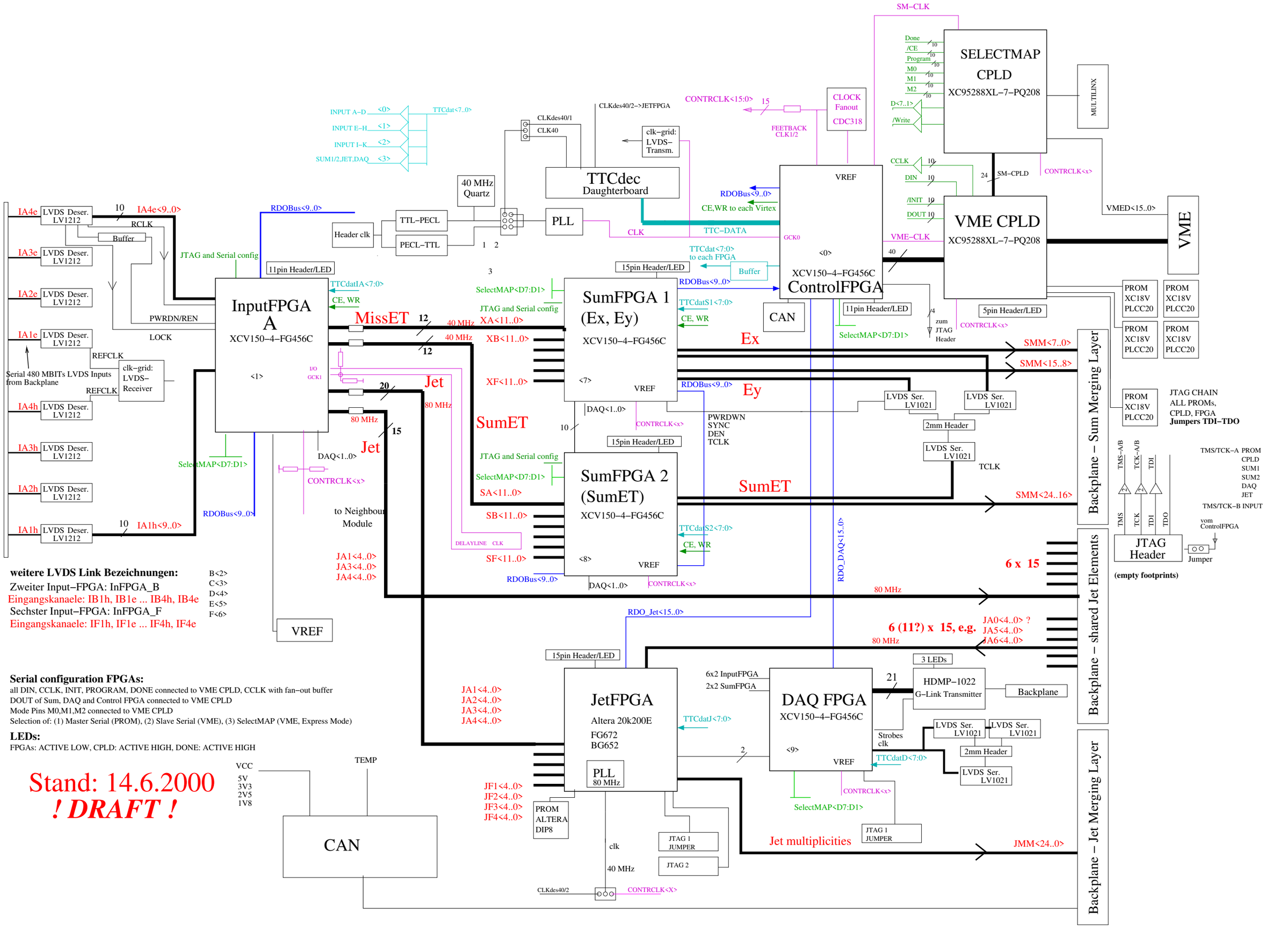
SM–CLK
SELECTMAP CPLD XC95288XL–7–PQ208
Done
/CE
Program
M0
M1
M2
D<7..1>
/Write
MULTILINX
CONTRCLK<15:0>
15
CLOCK Fanout CDC318
FEETBACK CLK1/2
INPUT A–D <0>
INPUT E–H <1>
INPUT I–K <2>
SUM1/2,JET,DAQ <3>
TTCdat<7..0>
CLKdes40/1
CLK40
CLKdes40/2–>JETFPGA
clk–grid: LVDS–Transm.
40 MHz Quartz
TTCdec Daughterboard
PLL
Header clk
TTL–PECL
PECL–TTL
CLK
TTC–DATA
RDOBus<9..0>
CE,WR to each Virtex
VREF
GCK0
<0>
XCV150–4–FG456C
ControlFPGA
CCLK
DIN
/INIT
DOUT
24
SM–CPLD
CONTRCLK<x>
VME CPLD XC95288XL–7–PQ208
VME–CLK
40
VMED<15..0>
VME
IA4e
LVDS Deser. LV1212
10
IA4e<9..0>
RCLK
Buffer
IA3e
IA2e
IA1e
IA4h
IA3h
IA2h
IA1h
IA1h<9..0>
PWRDN/REN
LOCK
REFCLK
Serial 480 MBITs LVDS Inputs from Backplane
clk–grid: LVDS–Receiver
JTAG and Serial config
11pin Header/LED
InputFPGA A
XCV150–4–FG456C
<1>
I/O GCK1
TTCdatIA<7:0>
CE, WR
MissET
12
40 MHz
XA<11..0>
XB<11..0>
XF<11..0>
Jet
20
80 MHz
15
SumET
DAQ<1..0>
CONTRCLK<x>
SelectMAP<D7:D1>
RDOBus<9..0>
to Neighbour Module
JA1<4..0>
JA3<4..0>
JA4<4..0>
VREF
15pin Header/LED
SumFPGA 1 (Ex, Ey)
XCV150–4–FG456C
<7>
VREF
SelectMAP<D7:D1>
JTAG and Serial config
TTCdatS1<7:0>
CE, WR
Ex
Ey
DAQ<1..0>
CONTRCLK<x>
15pin Header/LED
PWRDWN
SYNC
DEN
TCLK
SumFPGA 2 (SumET)
XCV150–4–FG456C
<8>
VREF
SA<11..0>
SB<11..0>
SF<11..0>
DELAYLINE CLK
TTCdatS2<7:0>
CE, WR
RDO_DAQ<15..0>
SMM<24..16>
6 x 15
80 MHz
RDO_Jet<15..0>
6 (11?) x 15, e.g.
JA0<4..0> ?
JA5<4..0>
JA6<4..0>
JA1<4..0>
JA2<4..0>
JA3<4..0>
JA4<4..0>
JetFPGA
Altera 20k200E
FG672
BG652
PLL
80 MHz
6x2 InputFPGA
2x2 SumFPGA
DAQ FPGA
XCV150–4–FG456C
<9>
VREF
TTCdatJ<7:0>
21
HDMP–1022
G–Link Transmitter
3 LEDs
Backplane
Strobes
clk
TTCdatD<7:0>
LVDS Ser. LV1021
2mm Header
JF1<4..0>
JF2<4..0>
JF3<4..0>
JF4<4..0>
PROM ALTERA DIP8
JTAG 1 JUMPER
JTAG 2
clk
40 MHz
CLKdes40/2
CONTRCLK<X>
Jet multiplicities
JMM<24..0>
Backplane – Sum Merging Layer
Backplane – shared Jet Elements
Backplane – Jet Merging Layer
zum JTAG Header
5pin Header/LED
PROM XC18V PLCC20
JTAG CHAIN
ALL PROMs,
CPLD, FPGA
Jumpers TDI–TDO
TMS–A/B
TCK–A/B
TDI
TMS
TCK
TDO
JTAG Header
Jumper
TMS/TCK–A PROM
CPLD
SUM1
SUM2
DAQ
JET
TMS/TCK–B INPUT
vom ControlFPGA
(empty footprints)
weitere LVDS Link Bezeichnungen:
Zweiter Input–FPGA: InFPGA_B
Eingangskanaele: IB1h, IB1e ... IB4h, IB4e
Sechster Input–FPGA: InFPGA_F
Eingangskanaele: IF1h, IF1e ... IF4h, IF4e
B<2>
C<3>
D<4>
E<5>
F<6>
Serial configuration FPGAs:
all DIN, CCLK, INIT, PROGRAM, DONE connected to VME CPLD, CCLK with fan–out buffer
DOUT of Sum, DAQ and Control FPGA connected to VME CPLD
Mode Pins M0,M1,M2 connected to VME CPLD
Selection of: (1) Master Serial (PROM), (2) Slave Serial (VME), (3) SelectMAP (VME, Express Mode)
LEDs:
FPGAs: ACTIVE LOW, CPLD: ACTIVE HIGH, DONE: ACTIVE HIGH
Stand: 14.6.2000
! DRAFT !
VCC
5V
3V3
2V5
1V8
TEMP
CAN