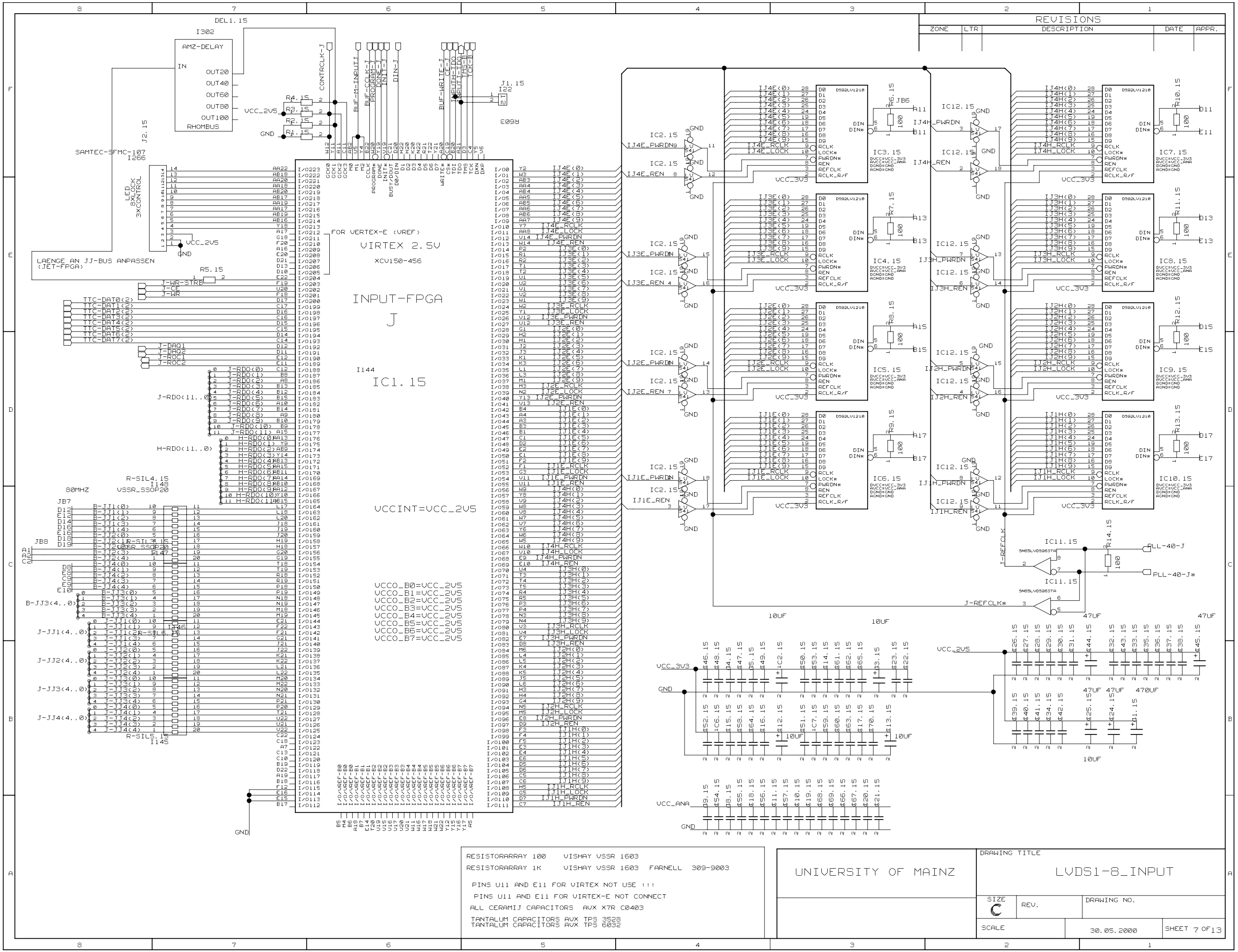
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPR.
AMZ-DELAY
RHOMBUS
SAMTEC-SFMC-107
LAENGE AN JJ-BUS ANPASSEN
(JET-FPGA)
FOR VERTEX-E (VREF)
VIRTEX 2.5V
XCV150-456
INPUT-FPGA
J
IC1.15
VCCINT=VCC_2V5
VCCO_B0=VCC_2V5
VCCO_B1=VCC_2V5
VCCO_B2=VCC_2V5
VCCO_B3=VCC_2V5
VCCO_B4=VCC_2V5
VCCO_B5=VCC_2V5
VCCO_B6=VCC_2V5
VCCO_B7=VCC_2V5
80MHZ
VCC_2V5
VCC_3V3
VCC_ANA
GND
PLL-40-J
PLL-40-J*
J-REFCLK*
RESISTORARRAY 100 VISHAY VSSR 1603
RESISTORARRAY 1K VISHAY VSSR 1603 FARNELL 309-9003
PINS U11 AND E11 FOR VIRTEX NOT USE !!!
PINS U11 AND E11 FOR VIRTEX-E NOT CONNECT
ALL CERAMIJ CAPACITORS AVX X7R C0403
TANTALUM CAPACITORS AVX TPS 3528
TANTALUM CAPACITORS AVX TPS 6032
UNIVERSITY OF MAINZ
DRAWING TITLE
LVDS1-8_INPUT
SIZE
C
REV.
DRAWING NO.
SCALE
30.05.2000
SHEET 7 OF 13