REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

DEL1.7
I298
AMZ-DELAY
IN
OUT20
OUT40
OUT60
OUT80
OUT100
RHOMBUS
CONTRCLK-A
M0-3-INPUTA
BUF-CCLK-A
PROGRAM-A
DONE-A
INIT-A
DIN-A
BUF-WRITE-A
CE-A
CONTR-TIO
INPUTS-TMS-B
TCK-B
R603
J1.7
I22
R4.7
R3.7
R2.7
R1.7
VCC_2V5
GND
J2.7
SAMTEC-SFMC-107
I265
LED
8XLOCK
3XCONTROL
LAENGE AN JA-BUS ANPASSEN
(JET-FPGA)
R5.7
A-WR-STRB
A-CE
A-WR
TTC-DAT0(0)
TTC-DAT1(0)
TTC-DAT2(0)
TTC-DAT3(0)
TTC-DAT4(0)
TTC-DAT5(0)
TTC-DAT6(0)
TTC-DAT7(0)
A-DAQ1
A-DAQ2
A-ROC1
A-ROC2
A-RDO(11..0)
VME-RDO(11..0)
R-SIL4.7
I145
VSSR_SSOP20
80MHZ
JB1
J-JA1(4..0)
J-JA2(4..0)
J-JA3(4..0)
J-JA4(4..0)
R-SIL5.7
I144
FOR VERTEX-E (VREF)
VIRTEX 2.5V
XCV150-456
INPUT-FPGA
A
IC1.7
VCCINT=VCC_2V5
VCCO_B0=VCC_2V5
VCCO_B1=VCC_2V5
VCCO_B2=VCC_2V5
VCCO_B3=VCC_2V5
VCCO_B4=VCC_2V5
VCCO_B5=VCC_2V5
VCCO_B6=VCC_2V5
VCCO_B7=VCC_2V5
GND

IC2.7 IA4E_PWRDN
IC2.7 IA4E_REN
IC2.7 IA3E_PWRDN
IC2.7 IA3E_REN
IC2.7 IA2E_PWRDN
IC2.7 IA2E_REN
IC2.7 IA1E_PWRDN
IC2.7 IA1E_REN
VCC_3V3
GND
DS92LV1210
DIN
DIN*
RCLK
LOCK*
PWRDN*
REN
REFCLK
RCLK_R/F
JB2
IC3.7
IC4.7
IC5.7
IC6.7
IC7.7
IC8.7
IC9.7
IC10.7
IC12.7 IA4H_PWRDN
IC12.7 IA4H_REN
IC12.7 IA3H_PWRDN
IC12.7 IA3H_REN
IC12.7 IA2H_PWRDN
IC12.7 IA2H_REN
IC12.7 IA1H_PWRDN
IC12.7 IA1H_REN
A-REFCLK
IC11.7
SN65LVDS9637A
PLL-40-A
PLL-40-A*
A-REFCLK*
10UF
47UF
VCC_2V5
VCC_ANA
RESISTORARRAY 100 VISHAY VSSR 1603
RESISTORARRAY 1K VISHAY VSSR 1603 FARNELL 309-9003
PINS U11 AND E11 FOR VIRTEX NOT USE !!!
PINS U11 AND E11 FOR VIRTEX-E NOT CONNECT
ALL CERAMIC CAPACITORS AVX X7R C0403
TANTALUM CAPACITORS AVX TPS 3528
TANTALUM CAPACITORS AVX TPS 6032

UNIVERSITY OF MAINZ

DRAWING TITLE: LVDS1-8_INPUT

SIZE	REV.	DRAWING NO.
C		
SCALE	30.05.2000	SHEET 7 OF 13