1.4.7 The Jet Feature Extractor Module [3p]

64 Potential algorithms, module description, essential design choices, board opera65
tional basics, output to L1Topo, etc

The jFEX processor performs the jet, large tau, missing-ET and total-ET trigger algorithms on 0.1 × 0.1 electromagnetic and hadronic jet elements provided by the Digital Processor System. The jFEX processor consists of a single shelf of AdvancedTCA modules (blades). Each module processes a phi-quadrant of calorimeter data, for one half of the detector in eta, comprising barrel, endcap, and forward calorimeters. A total of 8 modules is required for full coverage of all calorimeter data. Each module is supplied with an additional 100% of the data duplicated from neighbouring phi-quadrants. The data duplication is performed at the data source, the Digital Processor System. At eta=0 another stage of data duplication is required between modules covering the same quadrant, opposite eta. This duplication is achieved by a separate duplication stage at the level of the fibre patch panel.

Jets are identified on the jFEX modules as local maxima of energy deposits within a window sliding over the detector space in eta and phi, as outlined in section x. The chosen module layout and duplication factor allow for a maximum environment size of up to 1.7 in phi, i.e. environment data from up to 8 trigger towers on either side of any tower are accessible on each jFEX module. It should be noted that the environment actually available to the algorithms depends on the FPGA processors used on the modules (see below). The sharing of data between the individual FPGAs along eta is handled on module level.

The jFEX baseline design will operate at input rates of 6.4 Gb/s. With 8b/10b data encoding this provides for a payload of 128 bit per bunch tick per optical fibre link. This will allow for 8 trigger towers to be transmitted on a single fibre, organized as 4 x 2 towers in eta x phi. The optical fibres are routed through rear transition modules on 72-way MTP/MPO connectors. The signals are converted on 12-channel MicroPOD opto-electrical receivers. The electrical signals are routed on to the processor FPGAs.

De-serialization and real-time processing is performed on six large FPGAs. Even though a final choice will be made at a later stage only, the Xilinx devices XC7VX980T and XC7VX1140T have been identified as suitable candidates. They provide for sufficient input bandwidth to allow for processing a core area of up to 1.2 x 0.8 in eta x phi with an environment of 0.9 x 0.9 available to each trigger tower.