"Fibre bundles will be split and re-assembled similar to the L1Topo input scheme, so as to bring in fibres from a possibly larger number of L1Topo modules into the CTP optical input"

5.2.2 Real Time interface with L1Muon

At Phase-0 the muon input come from 16 octants. Such signal is sent by two lemo connectors (on MUCTPI) per octant, overclocked at 320 MHz. This corresponds to 256 bits in total to be transferred into two fibers at 6.4 Gb/s using 8/10 bit encoding. MUCTPI does not have optical output. Therefore a dedicated interface was designed [8]. The optical link to the L1Topo is 8 channels QSFP, replicated for two L1Topo modules. The muon input links will use the same data encoding of zero data as being defined for the calorimeter inputs (see 5.2.1).

5.2.3 Real Time interface with L1Calo

The calorimeter processors are connected via MPO/MTP 48-way fibre assemblies to 12 CMXs modules. At current, the L1Calo input consist of:

- 6 fibres from each of the 8 CMXs on the Cluster Processor (48 fibres)
- 8 fibres from 2 CMXs on the Jet Energy Processor (16 fibres)
- 2 fibres from 2 CMXs on Jet Energy Processor (for energies and zeroes, 4 fibres).

Data rates and formats are defined by the FPGAs used for serialization and deserialization. The production module will be equipped with high speed grade XC7VX690T equipped with 13Gb/s MGTs and 14Gb/s speed grade miniPOD recievers. This would guarantee operation at both 6.4 and 12.8 Gb/s.

5.2.4 Real Time optical interconnection with the CTP

From L1Topo two 12-way fibers are routed into the CTP from the processors FPGAs via Avago miniPODs transmitters. The optical signal from each Avago miniPOD is driven to the front panel via a short pigtail male MTP Molex connector. For data output to the CTP 6.4 Gb/s is used and the transmission protocol as in Sect.5.2.1.
Optical signals from L1Topo would come in through a dedicated Avago miniPOD receivers on the upgraded CTPCORE module.

caution: since we have 12 fibres per FPGA, we need another cross over box ~~to get~~ or patching to go into CTP. see above!

5.2.5 Real time electrical Interconnection with the CTP

32 differential LVDS signals are routed into the CTP from the processors FPGA via a SCSI female VHDCI type connector on the front panel. There are 22 signal pairs per processor FPGA reserved for the most latency critical paths to the CTP. Those are routed into the extension mezzanine on which the SCSI plug is mounted.
The maximum data rate on the electrical path will depend on the signal conditioning scheme chosen, and the cable length. The FPGAs themselves would allow for more than 1 Gb/s per signal pair. Signals from L1Topo would come in CTPCORE module through a dedicated LVDS connectors on the upgraded CTPCORE module. It provide three of those SCSI VHDCI type connectors, each can carry up to 32 differential pairs and a clock. The trigger input signals could run at 40 MHz (96 input signal to the CTP) or 80 MHz if needed (192 input signal to the CTP) where the DDR mode has a small latency penalty.

5.3 ROD functionality

There are two types of non-real-time optical links. Their data rates and encoding schemes need to be kept within the capabilities of the control FPGA (Kintex-7 / GTX transceiver, up to 10.3 Gb/s). Three emulated S-Links via miniPOD are envisaged for legacy DAQ and ROI links into L1Calo RODs Firmware has been devised at Stockholm University to generate compliant signals in Xilinx MGTs. The optical control link is assumed to be run at 1.25 Gb/s line rate and will therefore be compatible to Ethernet (SGMII). Additional miniPOD based connectivity is available for DAQ data, using an embedded ROD. The MiniPOD devices are used by the embedded ROD firmware and are compatible to the S-Link specifications. They offer 12 bi-directional fibre links and are accompanied by an electrical busy output lemo-00. The busy signal is active low and conditioned in the extension module (with an LCX245 device).

Outputs to the ROIB are duplicated on the control FPGA

5.4 Front panel

The front panel is carrying connectivity for both real-time output and non real-time control:

- Standard ATCA handle switches and LEDs (wired to IPMC).

- Compact Flash card slot for SystemACE.
- SD card slot.
- Ethernet port.
- 2 MTP connectors (from miniPODs, dedicated to CTP output).
- 2 MTP connectors (to miniPODs, for L1Muon input).
- 1 MTP connector (from miniPOD, for ROD and DAQ/ROI).
- 1 MTP connector (to miniPOD, for external optical input).
- 1 TTC optical AMP input.
- 1 electrical (SCSI VHDCI) connector (to CTP).
- 1 lemo-00 (Busy from embedded ROD).

5.5 Backplane connector layout

The backplane connector is made to standard ATCA layout in zones 1 and 2. Zone 3 is populated with four MTP/MPO connectors that connect onto a RTM with hermaphroditic blind-mate shrouds (MTP-CPI).

do we want to post that?

A Checklist for detailed design

(may well be ignored by reviews)

Detailed rules regarding signal integrity are to be followed so as to make sure the high desity/high speed module can be built successfully. In addition a few details on signal wiring for FPGA control pins are listed. ~~This list might be expanded for a detailed design review~~.

The rules with respect to power supply are:

- Use low-noise step-down converters on the module.
- ~~Use local POL linear regulators for MGT link supplies.~~ no!, all switched
- According to the device specifications the following supply voltages need to be applied to the FPGAs: Vccint=1.0, Vccaux=1.8V, Vccauxio=1.8V, Vccio(Virtex7)=1.8V, Vccio(Kintex7)=1.8V and 3.3V, Vccbram=1.0V, MGTVccaux=1.8V, MGTAVcc=1.0V, MGTAVtt=1.2V. checked?
- On all FPGA supply voltages observe the device specific ramp up requirement of 0.2μs to 50μs. checked?
- Run all supply voltages on power planes, facing a ground plane where possible, to provide sufficient distributed capacitance .
- Provide at least one local decoupling capacitor for each active component.
- For FPGAs, follow the manufacturers guidelines on staged decoupling capacitors (low ESR) in a range of nF to μF.
- Observe the capacitance limitations imposed by the voltage convertors.
- Minimise the number of different VCCO voltages per FPGA to avoid fragmentation of power planes.
- Avoid large numbers of vias perforating power and ground planes near critical components.

The rules with respect to general I/O connectivity are:

- Tie Vccaux and most bank supplies to 1.8V. A given FPGA is supplied by only one 1.8 V plane.

seems we proved that on prototype

- Use all processor FPGA banks for LVDS (1.8V) only.
- Use HP banks on the control FPGA for LVDS connections to the processor FPGAs and mezzanine modules.
- For the control FPGA only: wire a small number of banks for 3.3V single ended operation (HR banks).
- Neither reference voltages nor DCI termination are required on the processor FPGAs. Use respective dual-use pins for I/O purposes.
- For the control FPGA HR banks allow for DCI termination on single ended lines.

??

The rules with respect to single ended signalling are:

- Run FPGA configuration and FPGA JTAG clock lines on approximately 50Ω point-to-point source terminated lines.
- Observe the requirements on overshoot and undershoot limitation, in particular for System ACE and FPGA JTAG and configuration lines.
- Use slew rate limited or low current signals and/or series termination.

The rules with respect to differential signalling are:

- For discrete components, use internally sink-terminated devices throughout. Any non-terminated high-speed devices need to be documented in a separate list.
- Use LVDS on all general-purpose FPGA-FPGA links.
- Use LVDS on all GCK clock lines.
- Use DC coupling on all LVDS lines.
- Design all LVDS interconnect for 1Gb/s signalling rate.
- Use CML signalling on all MGT lines, for both data and clocks.
- Design all MGT data links for 10Gb/s signalling rate.
- Generally use AC coupling on all MGT differential inputs and outputs, for both data and clocks.

- ~~SFP devices might be internally decoupled,~~ MicroPod transmitters might have a sufficient common mode range to allow for direct connection.
- Use CML on all common clock trees; rather than using AC coupling, observe the signalling voltage and input compatibility rules as outlined by the device manufacturers.
- Use AC coupling or suitable receivers when crossing voltage or signal standard domains, except on LVDS.
- Use small package coupling capacitors to reduce parasitics on signal lines (0201 capacitors) or larger capacitors (0402 capacitors) and cut the grounding plane under this components.
- Use widely spread buses (S/H>5, possibly make a separation of 700 μm among pairs) to reduce cross talk.
- consider Rotating the model of 22 degree with reference to the PCB panel during PCB manufacture. This would evoid intra-pair differential skew. ?
- Use micro vias on the high speed links.
- Use bias networks on AC coupled inputs where required.
- Route all differential signals on properly terminated, 100Ω controlled-impedance lines.
- Have all micro strip lines face a ground plane.
- Have all strip lines face two ground planes or one ground plane and one non-segmented power plane.
- Avoid sharply bending signal tracks.
- Minimise cross talk by running buses as widely spread as possible.
- Avoid in-pair skew, in particular for MGT links and clocks.
- Not make use of device built-in programmable signal inversion for latency reasons. ?!

well, we do not do that, but its not a requirement!

I did not check the remaining pages!

- Avoid impedance discontinuities and stubs, in particular on MGT links and clocks.

The rules with respect to processor FPGA pre-configuration and configuration control pins are:

- Wire configuration lines for optional JTAG or slave serial configuration.
- Allow mode lines M0, M2 to be jumpered to either Vcc or GND. Prewire to Vcc.
- Connect M1 to the CPLD (GND=JTAG mode, Vcc=slave serial).
- Connect PROGRAM, INIT and DONE lines to the CPLD.
- Pullup DONE 330Ω, INIT 4k7 PROGRAM 4k7.
- Connect Vccbatt to GND.
- Wire DIN, DOUT and CCLK (series terminated) configuration lines to the CPLD.

The rules with respect to system monitor pins are:

- Connect DXN, DXP to I2C based monitoring circuits.
- Decouple analog power and GND according to UG370 with ferrite beads and wire the system monitor for internal reference (both Vref pins to analog GND).
- Do not use analog sense lines Vn and Vp and connect to analog GND.

B Power Supply

C Clock tree

D Control busses