Technical Specification

ATLAS Level-1 Calorimeter Trigger Upgrade

Topology Processor (L1Topo)

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Who else ?

Draft

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1 Introduction

73

This document describes the specifications for the upgrade of the Level-1 topology processor
module (L1Topo) of the ATLAS Level-1 Calorimeter Trigger Processor (L1Calo) [1.1] . An
L1Topo processor has initially been introduced into the ATLAS trigger for Phase-0 during
Run-2 to improve trigger performance by correlating trigger objects (electromagnetic
clusters, jets, muons) and global quantities.

The new L1Topo will be installed in L1Calo during the long shutdown LS2, as part of the
Phase-1 upgrade, and it will operate during Run 3. It is built to be forward compatible and
may remain in the system after the Phase-2 upgrade in LS3, being operated in Run-4 as
L1Topo or L0Topo, dependent on the eventual trigger architecture in Phase-2.

The ATLAS Phase-1 Level-1 Trigger system comprises eFEX [1.4] , jFEX [1.5] , and gFEX
[1.6] subsystems as calorimeter data sources for L1Topo. They are providing trigger object
data, "TOBs", to L1Topo via optical fibre bundles. Another source of trigger objects is the
ATLAS muon trigger subsystem.

L1Topo is a set of dual width ATCA [1.8] modules, operated in a single ATCA "shelf"
(crate), compliant with ATLAS and L1Calo standards. Real-time data are received via optical
fibres exclusively. L1Topo runs a large number of concurrent and independent algorithms on
the input data, to derive a number of trigger bits, typically one result bit and one overflow bit
per algorithm. The result bits are forwarded to the Central Trigger Processor, which
correlates these bits with further trigger and machine data to generate Level-1 Trigger and
associated data words, to be transmitted back to the detector. Outputs to CTP are available
via electrical and optical data paths.

95 The non-real-time data paths of L1Topo are basically identical to the L1Calo modules built
96 for Phase-1: data are sent into the readout and the 2nd level Trigger via L1Calo RODs over
97 the backplane of the ATCA shelf. Control and global timing are accomplished via the
98 backplane as well. To that end, L1Calo communicates with two hub/ROD modules located in
99 dedicated slots of the L1Topo shelf.

100 The Phase-1 Level-1 trigger system and the role of L1Topo within the Level1Calo system is
101 described elsewhere in detail. Material on current Phase-0 L1Topo construction and
102 performance is available as well. References are given in the appendix.

103

2 Functionality

105 Figure 1 shows a block diagram of L1Topo. The various aspects of L1Topo functionality are
106 described in detail below. Implementation details are given in section 3.
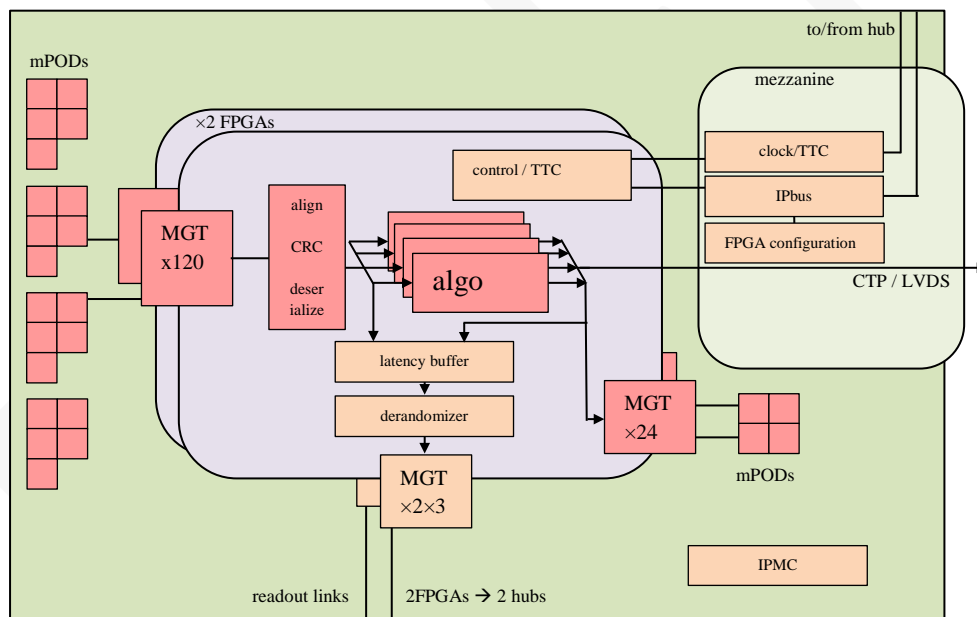
107
108 **Figure 1.   A block diagram of the L1Topo module.**

2.1   Real-Time Data Path

110 ATCA Backplane zone 3 of L1Topo is used for real-time data transmission. The input data
111 enter L1Topo optically through the backplane. The fibres are fed via four blind-mate
112 backplane connectors that carry 72 ?? fibres each. The optical signals are converted to
113 electrical signals in 12-fibre receivers. For reason of design density miniPOD [1.11] receivers
114 are used. The electrical high speed signals are routed into two FPGAs, where they are de-
115 serialized in MGT receivers; the parallel data are presented to the FPGA fabric. The two
116 FPGAs operate on their input data independently and in parallel. High bandwidth, low

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117 latency parallel data paths allow for real-time communication between the two processors.
118 The signal results are transmitted towards the CTP on both optical fibres and electrical
119 cables. The electrical signals are routed via an extension mezzanine module.

2.1.1   Input Data

121 L1Topo will receive the topological output data of the sliding window processors from
122 L1Calo and data from the L1Muon system. The data format transmitted into L1Topo
123 comprises TOB data (Trigger Object data) for jets, clusters and muons. The data will consist
124 of a description of the position of an object (jet, e/m cluster, tau and muons) along with some
125 qualifying information, like the energy sum within the object.

2.1.2   Input Data Rates

127 So as be compatible to the conflicting bitrate requirements of gFEX and eFEX, the module
128 will be built so as to support input data rates of either 11.2 or 12.8 Gb/s on a given input
129 channel. Since MGT input channels are organized in quads, with all four channels sharing
130 clock generation, it is assumed that a given quad will be operated on one of the two bitrates
131 only. Also, for the relatively small number of channels that are used for high speed output,
132 the input bitrate might need to be chosen for compatibility with the output rate. That might
133 create constraints for physical location of certain object types on the FPGA / on the fibre
134 bundles.

2.1.3   Algorithms

136 Due to the large amount of logic resources in the chosen FPGAs, a significant number of
137 algorithms is expected to be run on the real-time data in parallel. Most of the algorithms will
138 be identical or very similar to the ones already introduced for Run-2. In addition, plenty of
139 new and more complex algorithms can be added.

2.1.4   Data Sharing

141 Topology data are processed in two FPGAs. There is no data duplication implemented at
142 PCB level. The two processors can communicate via a parallel bus to get access to data that
143 cannot be received directly via the multi-gigabit links. Though according to the device data
144 sheets higher data rates should be possible, a maximum bit rate of 640 Gb/s per differential
145 pair is anticipated for the inter-FPGA link, which is a convenient multiple of the bunch clock
146 frequency. That will limit parallel connectivity to 60-80 Gb/s of aggregate bandwidth (see
147 section 3).

2.1.5   Output

149 The real-time output data of L1Topo to the CTP consist of individual bits indicating whether
150 a specific algorithm passed or not plus an overflow bit. The resulting trigger data are
151 expected to exhibit a rather small volume. They will be transmitted to CTP optically or
152 electrically. A single fibre-optical ribbon connection per module that carries 48 fibres,
153 running through the front panel of the module is provided for this purpose. A mezzanine

154 board will be required to interface L1Topo to the CTPCORE module electrically via 32
155 LVDS signals at low latency.

2.2 Error Handling

157 Input data are protected by several error detection schemes. The MGT hardware blocks can
158 detect link errors and code errors. Additional protection is achieved by cyclic redundancy
159 check characters included in the real-time data. Errors of all types will be monitored and the
160 error counter will be incremented for any bunch clock cycle where there is at least one error
161 in any input channel. Detailed information of the specific error will be stored in expert
162 registers. Detection of an error will enforce zeroing the real-time data for the affected events.

2.3 Latency

164 A breakdown of the estimated latency of the real-time path of the L1Topo is given in the
165 ATLAS TDAQ System Phase-1 Upgrade Technical Design Report [1.1] .

2.4 Readout Data Path

167 Upon receipt of an L1Accept all L1Topo real-time output data will be captured and sent to
168 the DAQ. Input data capture can be made dependent on possible occurrence of reception
169 errors, or be fixed, software programmable. The number of slices worth of data per bunch
170 tick is programmable up to 3 ????. Data are pipelined and de-randomized on the processors
171 and then serialized onto the backplane links to the ROD/hub modules. Region-of-Interest data
172 (RoI) are captured separately and made available to the higher level triggers via the RoI
173 builder.

174 A detailed description of the readout scheme is given at xxxx.

175

2.5 TTC and Clock

177 Timing signals are received in the L1Topo shelf via the Hub-ROD module. There, the clock
178 is recovered and commands are decoded, before being re-encoded using a local protocol. This
179 use of a local protocol allows the TTC interface of the shelf to be upgraded to future timing
180 distribution schemes without any modification of the L1Topo modules.

181 The L1Topo module receives the clock and TTC commands from the Hub-ROD via the
182 ATCA backplane. It receives the clock on one signal pair and the commands on a second (see
183 section 3.11 for details).

2.6 Module Control and Configuration

An IPBus interface is provided for high-level, functional control of L1Topo. This allows, for example, algorithmic parameters to be set, modes of operation to be controlled and spy memories to be read.

IPBus is a protocol that runs over Ethernet to provide register-level access to hardware. Here, it is run over a 1000BASE-T Ethernet port, which occupies one channel of the ATCA Base Interface. On L1Topo there is a local IPBus interface in every FPGA. These interfaces contain those registers that pertain to that device. A control FPGA, residing on a mezzanine, implements the interface between the topology processors and the shelf backplane, routing IPBus packets to and from the other devices as required. The control FPGA also contains those registers which control or describe the state of the module as a whole. For those devices such as MiniPODs, which have an I^2C control interface, an IPBus-I2C bridge is provided.

The processor FPGAs are configured upon power-up from flash based storage. The configuration data are clocked into the FPGAs via a parallel bus. Controller and flash memory are located on the mezzanine. For debug purposes the processors can be configured and accessed (Ibert, Chipscope ILA) via their JTAG interface.

2.7 Commissioning and Diagnostic Facilities

To aid in module and system commissioning, and help diagnose errors, the L1Topo can be placed in Playback Mode (via an IPBus command). In this mode, real-time input data to L1Topo are ignored and, instead, data are supplied from internal scrolling memories. These data are fed into the real-time path at the input to the algorithm logic, where they replace the input data from the FEXes and muons.

Optionally, the real-time output of L1Topo can also be supplied by a scrolling memory. It should be noted that, in this mode, L1Topo will process data from one set of memories, but the real-time output will be supplied by a second set of memories. Depending on the content of these memories, this may result in a discrepancy between the real-time and readout data transmitted from L1Topo.

In Playback Mode the use of the input scrolling memories is mandatory, the use of the output scrolling memories is optional, and it is not possible to enable Playback Mode for some channels but not others. Playback Mode is selected, and the scrolling memories loaded, via the IPbus interface. The scrolling memories are 256 (????) words in depth.

In addition to the above facility, numerous flags describing the status of L1Topo can be read via the IPbus control. Access points are also provided for signal monitoring, boundary scanning and the use of proprietary FPGA tools such as ChipScope and IBERT.

2.8 Environmental Monitoring

L1Topo monitors the voltage and current of all critical power rails on the board. It also monitors the temperatures of all the FPGAs, of the MiniPOD receivers and transmitters, and of other areas of dense logic. Where possible, this is done using sensors embedded in the relevant devices themselves. Where this is not possible, discrete sensors are used.

223 A small set of voltage and temperature data are collected by the L1Topo IPMC, via an I^2C
224 bus and are made available to ATLAS DCS via the shelf manager. Supplementary
225 environment data are available to the control FPGA. These data can be accessed via IPbus.

226 FPGAs are protected against over temperature by internal monitoring and shutdown. This
227 provides the lowest possible reaction time. Also, if any board temperature exceeds a
228 programmable threshold set for a specific device monitored via IPMB, the IPMC powers
229 down the board payload (that is, everything not on the management power supply). The
230 thresholds at which this function is activated should be set above the levels at which the DCS
231 will power down the module. Thus, this staged mechanism should activate only if the DCS
232 fails. This might happen, for example, if there is a sudden, rapid rise in temperature to which
233 the DCS cannot respond in time.

2.9 ATCA form factor

235 L1Topo is an ATCA module, conforming to the PICMG® 3.0 Revision 3.0 specifications.
236 The modules are dual width, they occupy two adjacent slots of an ATCA shelf each.

3 Implementation details

3.1 Modular Design

239 L1Topo consists of an ATCA sized main board, equipped with mezzanines. The mainboard
240 mainly carries the real-time processing circuitry: Two processor FPGAs, connected up with
241 12 MiniPOD devices ($10 \times$ RX, $2 \times$ TX) each. The FPGA/MiniPOD circuitry is two exact
242 copies placed on the same PCB.

243 Module control via IPbus, and breakout of the electrical links to the CTP are implemented on
244 the "Extension Mezzanine". FPGA configuration memories are also located on the
245 mezzanine, along with the TTC/clock reception and conditioning (jitter reduction). The
246 mezzanine runs along the lower part of the front panel to allow for front panel connectivity
247 and controls.

248 Further front panel connectivity and indicators are located on a separate, small front panel
249 mezzanine in the upper part of the module.

250 Environmental monitoring and low level control is implemented on an IPMC controller
251 module (LAPP IPMC).

252 Primary power supply is via standard PIM and converter bricks. Secondary power supplies
253 are located on mezzanines.

3.2 Input Data Reception

255 L1Topo receives data from the L1Calo processors and the Muons via optical fibres. The
256 bitrate is specified to 11.2 and 12.8Gb/s data rate, so as to be compliant with all data sources.

257 The data are required to be 8b/10b coded data streams. Each fibre carries a net data volume of
258 224 (or 256 respectively) bits of data per bunch tick.

259 The input fibres to L1Topo are organised into 4 ribbons of 72 fibres each. They are routed to
260 L1Topo via the rear of the ATCA shelf, where a rear transition module provides mechanical
261 support. Optical connections between the fibres and L1Topo are made by four 72-way Multi-
262 fibre Push-On/Pull-Off (MPO) connectors, mounted in Zone 3 of the ATCA backplane.
263 These connectors allow L1Topo to be inserted into, and extracted from, the shelf without the
264 need to handle individual ribbon connections.

265 On the L1Topo side of the MPO connectors, 20 optical ribbons (each comprising 12 fibres)
266 carry the signals to 20 MiniPOD receivers. These perform optical to electrical conversion.
267 They are mounted on board, around the Processor FPGAs, to minimise the length of the
268 multi-Gb/s PCB tracks required to transmit their output.

269 ## 3.3   Processor FPGA

270 There are two Processor FPGAs on each L1Topo module. The functionality they implement
271 can be grouped into real-time, readout and slow-control functions. Both FPGAs on an
272 L1Topo module have the same wiring. Differences in functionality between Processor
273 FPGAs on the same and different modules are due to different algorithms being run and are
274 implemented via different firmware versions only.

275 Every Processor FPGA performs the following real-time functions:

276 •   It receives, from MiniPOD optical receivers, up to 118 inputs of serial data at
277   11.2 or 12.8 Gb/s per MGT link.

278 •   It detects any data integrity issues with help of the MGT built-in error checks and with
279   help of CRC checksums embedded in the user data.
280   —   Any errors are registered and counted, error counts can be read and reset via module
281   control.
282   —   Any erroneous real-time data are zeroed.

283 •   It allows for fine grain data alignment to word (bunch tick) boundaries.

284 •   It allows for coarse grain data alignment in terms of full bunch ticks, up to 32 ticks.

285 •   It runs topological algorithms on the conditioned real-time input data.

286 •   It is able to share real-time data with the other on-board FPGA via parallel links

287 •   It forwards the trigger results (typically a trigger bit with accompanying overflow bit) to
288   the CTP.

289 •   The CTP is fed with trigger results bits directly from each FPGA
290   —   Electrically (LVDS) via the extension mezzanine
291   —   Optically via MiniPOD

292 On the readout path, each Processor FPGA performs the following functions.

293 •   The Processor FPGA records the input data and the output generated on the real-time path
294   in scrolling memories, for a programmable duration of up to 3(?) μs.

295   • On receipt of an L1A, it writes data from the scrolling memories to the FIFOs, for a
296   programmable time frame. This is only done for those data enabled for readout by the
297   control parameters.

298   • The Processor FPGA transmits data from the readout FIFOs to the ROD module, via a 9.6
299   GB/s MGT backplane link.

300 For module control and monitoring, each Processor FPGA contains a local IPBus interface,
301 which provides access to registers and RAM space within the FPGAs.

302 The Processor FPGA footprint on L1Topo is compatible to several FPGA types from the
303 Xilix UltraScale(+) families. XCVU190 and VU9P are envisaged for L1Topo. They are all
304 2577 ball devices.

305 Of the 120 high speed links available in the XCVU190 or VU9P, two(?) are reserved for
306 control purposes (TTC data and module control).

307 Regarding general-purpose I/O, of the total of 448 pins available, five ?? banks of 22 pairs
308 each (???) are used for inter-FPGA data sharing. The pair count includes one pair of
309 forwarded clock per bank. Each one-to-one bank interconnect is meant to be operated in one
310 direction only. Receive and transmit lanes are not to be mixed within one bank. Inter-bank
311 pin swapping is not allowed during PCB routing work.

3.4   Clocking

313 There are two types of clock sources on L1Topo: on-board crystal clocks and the LHC TTC
314 clock, received from the ATCA backplane. These clock sources are fed via the clocking
315 circuitry to the two processor FPGAs. The 40.079MHz TTC "clean" clock has potentially too
316 much jitter to drive multi-Gb/s links directly. A PLL chip is therefore used to clean up the
317 jitter on this clock. From the input of 40.079 MHz the PLL chip can generate clocks of
318 frequency $n \times 40.079$ MHz within a certain range. This flexibility allows the multi-Gb/s links
319 on the L1Topo to be driven at a range of different rates. The Si5345 has been tested and
320 verified on the jFEX prototype and will be used on L1Topo. The clock (re)generation
321 circuitry is located on the extension mezzanine, the individual clock trees for MGT reference
322 clocks and global clocks are actively fanned out on the main board.

323 The 5? MGT reference clock trees are operated at CML signal level, they are AC coupled
324 into the FPGAs. The main clock tree supplies the real-time inputs running at 11.2/12.8Gb/s.
325 There are additional trees for real-time output (6.4/12.8Gb/s) and for backplane output
326 towards the RODs (9.6Gb/s).

3.5   High-Speed signals on the PCB

328 L1Topo is a very high-speed and very high-density ATCA module, which has many optical
329 fibre links and some electrical backplane links running at a speed of up to 12.8Gb/s. In
330 addition, the tight ATLAS L1Calo latency margin requires a large number of parallel links
331 running at up to 1Gb/s between FPGAs for data sharing on L1Topo.

332 Signal integrity is a challenge for the L1Topo design. It benefits, however from the detailed
333 PCB simulations that have been done for the jFEX prototype, from which the phase-1
334 L1Topo is being derived.

3.6 FPGA configuration

336 The L1Topo mainboard houses two big Processor FPGAs. The configuration of these FPGAs
337 is controlled from the extension mezzanine. To this end all signal lines required for either
338 master SPI mode or slave SelectMAP are routed to the mezzanine.

339 The baseline configuration option is SPI mode. Though dual SPI mode (ie. Byte wide
340 configuration) is supported by this scheme, the mezzanine currently under construction will
341 use a single SPI flash memory chip per processor FPGA. The flash devices can be written
342 either via JTAG or via IPbus. The latter operation will require specific firmware and software
343 to be written.

344 The configuration scheme will allow for both the current production firmware and a "golden"
345 recovery image to be stored on the SPI flash devices. Whether that feature will actually be
346 used is as yet undecided, since the processor FPGAs can always be configured through the
347 mezzanine-based control FPGA, even with an erased or corrupted flash ship connected up to
348 the processors. Direct JTAG configuration of the processor FPGAs is an additional option for
349 debug purposes.

350

3.7 The Extension Mezzanine

352 The extension mezzanine module provides many of the (non-realtime) services described
353 above. It carries mainly module control, clock/control, and configuration circuitry. It also
354 provides initialization circuitry for the FPGAs and acts as an interface to environmental
355 monitoring devices. The only real-time signals running via the mezzanine are the electrical
356 outputs to the CTP.

357 The "intelligent" module controller is an FPGA from the XILINX Artix-7 family. This
358 Control FPGA handles incoming IPbus requests and forwards the data and control packets to
359 the processors on the mainboard via MGT (GTP) links. MGT links are also used to replicate
360 incoming TTC data into the four processors (see below).

361 The IPbus communicates with its control PC(s) via an Ethernet Phy chip. The chip type
362 chosen is VSC8221. It is an electrical Ethernet (1000BASE-T) to SGMII device. The SGMII
363 link is connected to an MGT link of the control FPGA. The 1000BASE-T port is linked to the
364 hub/ROD module-1 via the backplane. This link is AC-coupled with series capacitors.
365 Magnetics (transformers) are not required due to the choice of Phy chip, which is specifically
366 designed (voltage mode drivers, internal biasing) to support magnetics-free links.

367 The backplane clock arriving from the hub modules is transmitted at the LHC bunch crossing
368 frequency of 40.079 MHz and meant to be of high quality, low jitter. However, locally on the
369 mezzanine this clock is run through a jitter cleaner / clock synthesizer chip (Si5345) where it
370 is refreshed and multiplied to higher ratios of the bunch clock. The jitter cleaner delivers four

371 multiples of the base frequency: x1 multiplication, just jitter cleaned for purpose of global
372 clock into the FPGA fabric, a multiple suitable for 11.2/12.8 Gb/s real-time input reference, a
373 multiple for the backplane readout links and a separate multiple for the real-time outputs.

374 Can a single clock support 11.2/12.8? Can all output clocks be generated on the same jitter
375 cleaner for all frequencies required? What do we do about crystal clocks? TTC data recovery
376 from crystal or LHC multiple? Option switch on first iteration of mezzanine? The secondary
377 IPbus is operated off an LHC clock on current Topo, which creates possible issues. Do we
378 believe the jitter cleaner generates a clean clock even at LHC clock switches?

379 The mainboard processors are fed from the jitter cleaner outputs via clock fan-out chips. The
380 global (FPGA fabric) clocks are of LVDS level, the MGT reference clocks of CML. Separate
381 crystal clocks are provided for local use on IPbus/Ethernet and optionally for TTC data (?)
382 inputs.

383 The TTC data links are received from the backplane, one AC-coupled MGT link from each
384 hub/ROD module. The data are routed into the control FPGA, where they are interpreted and
385 forwarded to the processor FPGAs, again on AC-coupled MGT links. The TTC data links are
386 synchronous to the LHC bunch clock and therefore require an LHC clock multiple for re-
387 transmission to the processors on the mainboard.

388 While the processor FPGAs are accessible through their JTAG ports at any time, the
389 configuration bit stream required at any power-up is meant to be provided by local storage.
390 Default storage device is one large (quad) SPI flash memory per FPGA. The device chosen
391 for the first version of the mezzanine is... (MT25QU01GBBB8ESF-0SIT seems to be the
392 only one currently available!!! Avnet only !!! order now). Different configuration schemes
393 can be made available with further versions of the mezzanine card, should the updates of the
394 flash devices, required for any persistent processor firmware updates, be considered
395 inconveniently slow. The update process can be triggered and controlled from either the
396 control FPGA or via JTAG. The control FPGA itself will in any case be configured from a
397 small SPI flash chip, which due to smaller capacity and rare updates, is assumed to be a
398 rather painless operation. For the control FPGA in-situ (live) updates are possible due to the
399 use of a Xilinx-provided fall-back / golden image scheme.

400 Environmental data (voltages, currents, temperatures) are collected on the mainboard by I2C
401 based sensors, and routed to the mezzanine via the bidirectional I2C buses. Parameters in the
402 respective devices are set in the same way. Data are originating from dedicated monitoring
403 chips, or from monitor/control interfaces available in core functionality devices, e.g.
404 MiniPODs. They are routed into the control FPGA with an optional breakout onto headers.
405 The control FPGA allows for access to these data via IPbus. The status/control data
406 exchanged that way are complementary to the IPMC data. The handling of serialized slow
407 control data on FPGAs and the description of the required state machines in VHDL and the
408 maintenance of such circuitry is not particularly efficient in terms of engineering effort. For
409 this reason an updated mezzanine with a complimentary, small microcontroller for
410 housekeeping functionality is envisaged. Alternatively an embedded processor might be used
411 on the FPGA.

412 The real-time signals forwarded to the CTP via the mezzanine are plain route-through only.
413 They are run via the mezzanine so as to allow for re-grouping signals from the two processor
414 FPGAs into a single cable port, should that be required. This scheme is taken over from the
415 Phase-0 Topology processor. At current the signal distribution is symmetric, same bandwidth

416 from each of the processors. That's the baseline for the Phase-1 modules as well, unless
417 specific requirements are presented. Do we assume this route-through via mezzanine is what
418 we want again, or would we rather opt for a separate mini mezzanine / Y-cable construction?

419

3.8 The IPM Controller

421 For the purposes of monitoring and controlling the power, cooling and interconnections of a
422 module, the ATCA specification defines a low-level hardware management service based on
423 the Intelligent Platform Management Interface standard (IPMI). The Intelligent Platform
424 Management (IPM) Controller is that portion of a module (in this case, L1Topo) that
425 provides the local interface to the shelf manager via the IPMI bus. It is responsible for the
426 following functions:

427 • interfacing to the shelf manager via dual, redundant Intelligent Platform Management
428   Buses (IPMBs), it receives messages on all enabled IPMBs;

429 • negotiating the L1Topo power budget with the shelf manager and powering the payload
430   hardware only once this is completed (see section 3.9);

431 • managing the operational state of L1Topo, handling activations and deactivations, hot-
432   swap events and failure modes;

433 • implementing electronic keying, enabling only those backplane interconnects that are
434   compatible with other modules in shelf, as directed by the shelf manager;

435 • providing to the Shelf Manager hardware information, such as the module serial number
436   and the capabilities of each port on backplane;

437 • collecting, via an I^2C bus, data on voltages and temperatures from sensors on L1Topo,
438   and optionally exchanging these data, with the control FPGA;

439 • driving the ATCA-defined LEDs.

440 L1Topo uses the IPMC mezzanine produced by LAPP as the IPM Controller [1.12] . The
441 form factor of this mezzanine is DDR3 VLP Mini-DIMM.

3.9 Power Management

443 With regard to power, the hardware on the L1Topo is split into two domains: Management
444 hardware and Payload hardware. The Management hardware comprises the IPM Controller
445 plus the primary DC-DC converters and any non-volatile storage that this requires. By
446 default, on power up, only the Management hardware of L1Topo is powered (drawing no
447 more than 10 W), until the IPM Controller has negotiated power-up rights for the Payload
448 hardware with the shelf manager. This is in accordance with the ATCA specification.
449 However, via a hardware switch it is also possible to place L1Topo in a mode where the
450 Payload logic is powered without waiting for any negotiation with the shelf controller. This
451 feature, which is in violation of the ATCA specification, is provided for diagnostic and
452 commissioning purposes.

453 On power-up of the Payload hardware, the sequence and timing with which the multiple
454 power rails are turned on can be controlled by the IPM Controller. Alternatively, by setting
455 hardware switches, these rails can be brought up in a default sequence defined by resistor-
456 capacitor networks on the module. That's probably wrong for both jFEX and L1Topo. We are
457 using a CPLD. Anything else?

458 Excluding the optional exception noted above, the L1Topo conforms to the full ATCA
459 PICMG® specification (issue 3.0, revision 3.0), with regard to power and power
460 management. This includes implementing hot swap functionality, although this is not
461 expected to be used in the trigger system.

462 Power is supplied to L1Topo on dual, redundant -48V DC feeds. A standard power input
463 module (eg. PIM400) and a step down convertor, both "quarter brick" sized, are employed
464 for power conditioning and conversion down to 12V. This 12V supply is stepped down
465 further, by multiple (secondary) switch-mode regulators, to supply the multiplicity of
466 voltages required by the payload hardware.

467 For the power supplies to the FPGA multi-Gigabit transceivers, the PCB design guidelines
468 and noise requirements specified in the UltraScale Series FPGAs GTH Transceiver User
469 Guide (UG576) and GTY Transceiver User Guide (UG578) will be observed. The secondary
470 convertors are located on mezzanine modules.

471 ## 3.10 Front-panel Inputs and Outputs

472 The following signals are, or can be, sent or received via the L1Topo front panel.

473 • Electrical differential (LVDS) signals are sent to the CTP via an SCSI VHDCI style
474 connector, located on the mezzanine.

475 • Fibre-optical output to CTP via MPO/MTP connectors. A total of 48 fibres can be sent
476 out of the front panel, largest fraction assumed to be spares for possible use at Phase-2.

477 • Auxiliary clock. This input allows L1Topo to be driven by an external 40 MHz clock, in
478 the absence of a suitable clock on the backplane. The optimum physical form factor for
479 the signal is to be identified.

480 • Do we want a clock output ? what else ?

481

482 The following bi-directional control interfaces are available on the front panel. See section
483 3.13 for the use of these interfaces.

484 • JTAG Boundary Scan. The optimum physical form factor for this interface is to be
485 identified.

486 • 1G Ethernet socket (optional, not to be used in production environment).

3.11 Rear-panel Inputs and Outputs

3.11.1   ATCA Zone 1

This interface is configured according to the ATCA standard. The connections include

- dual, redundant -48V power supplies,
- hardware address,
- IPMB ports A and B (to the Hub module),
- shelf ground,
- logic ground.

Figure 2 shows the backplane connections between the L1Topo and the Hub module, which are located in Zones 1 and 2 of the ATCA backplane. See the ATCA specification for further details.

3.11.2   ATCA Zone 2

3.11.2.1   Base Interface

The Base Interface comprises eight differential pairs. Four of these are connected to hub slot one and are used for module control (IPbus), the other four are connected to hub slot two and are used to interface to the IPMC.

3.11.2.2   Fabric Interface

The Fabric Interface comprises 16 differential signal pairs, eight of which are connected to hub slot one, and eight of which are connected to hub slot two. Those signal pairs connected to hub slot one are used as follows:

- One signal pair is used to receive the TTC "clean" clock of 40.079 MHz.

- One signal pair is used to receive decoded TTC commands, plus near real-time signals such as ROD busy. This lane is connected into a multi-Gigabit receiver on the extension mezzanine. The exact protocol is defined by the hub module developers and is implemented in firmware. The link speed does not exceed 10 Gb/s.

- Six signal pairs are used to transmit readout data via MGT links. The protocol is defined by the ROD module developers. The link speed does not exceed 10 Gb/s. Two out of these six signal pairs are used as receivers in standard ATCA backplanes. They are operated in inverse direction on all L1Calo modules to increase the possible readout bandwidth. These two links are considered spares on L1Topo

The same connectivity is available into hub slot 2.
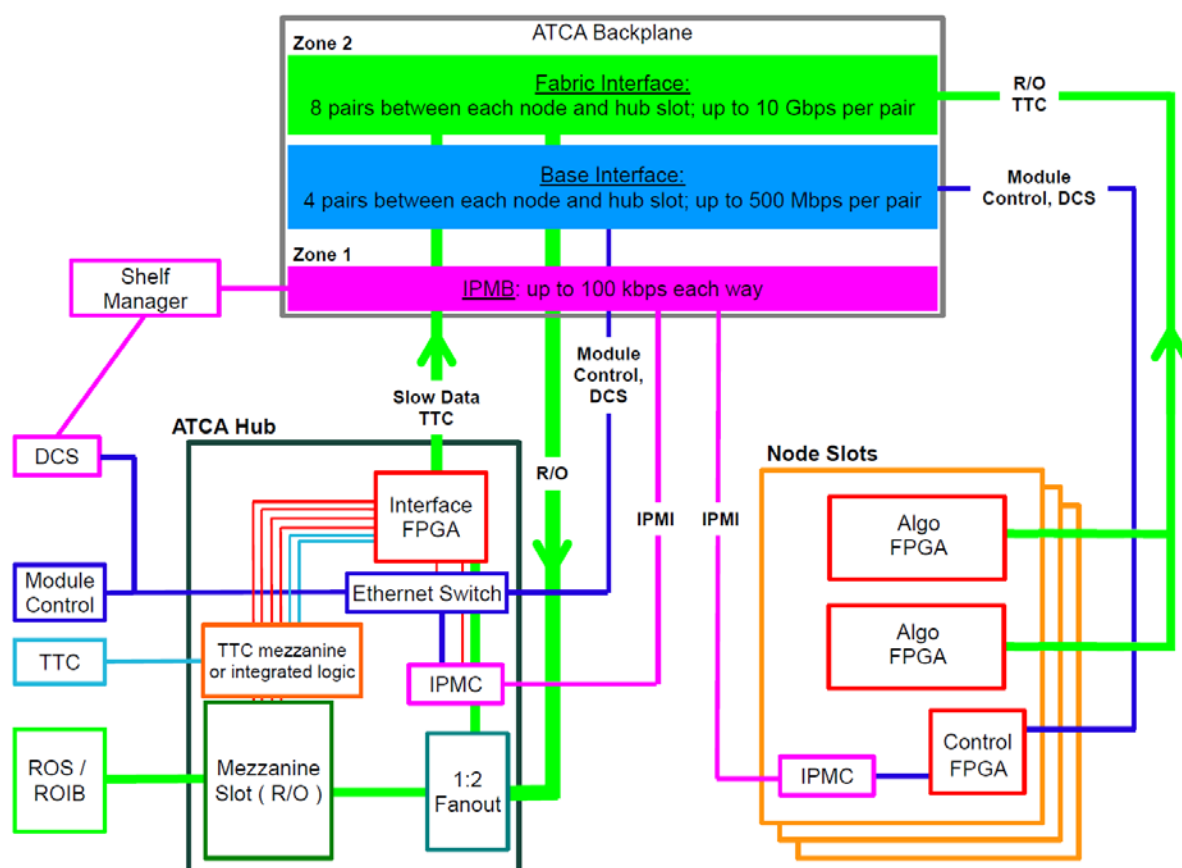
518
519 **Figure 2.   The ATCA backplane connections between the L1Topo and the Hub**
520   **module.**

521

3.11.3   ATCA Zone 3

523 ATCA zone 3 houses four 72-way optical MPO connectors. That allows for up to 288 fibres,
524 carrying data from the feature extractors and muons to L1Topo (see section 3.1). These
525 fibres are supported in the L1Topo shelf by a (passive, mechanical) rear transition module
526 (RTM). On the L1Topo side of the connectors, fibre ribbons carry the calorimeter data to
527 MiniPOD receivers, mounted in board. The optical connections are made on the insertion of
528 the L1Topo into the shelf, and broken on its extraction. Dependent on the requirements, real-
529 time output can possibly be run on otherwise dark fibres (spares). However, it is anticipated
530 that real-time optical output connection is rather made via the front panel.

3.12 LEDs

532 All LEDs defined in the ATCA specifications are located on the L1Topo front panel. In
533 addition, further status LEDs are provided on either the front panel or the top side. These
534 indicate functions like power, Done signals, L1A receipt und further LEDs for diagnostic
535 purposes for all FPGAs.

3.13 Instrument Access Points

3.13.1 Set-Up and Control Points

The following interfaces are provided for the set-up, control and monitoring of the L1Topo. They are intended for commissioning and diagnostic use only. During normal operation it should not be necessary to access the L1Topo via these interfaces.

- The JTAG Boundary Scan port: via this port a boundary scan test can be conducted, all FPGAs on the L1Topo can be configured, the configuration memory of the Configurator can be loaded and the FPGA diagnostic/evaluation tool ChipScope can be run, including for IBERT tests. This port is on the front panel.

- The 1G Ethernet port (optional): this port provides an auxiliary control interface to the L1Topo, over which IPBus can be run, should there be a problem with, or in the absence of, an IPBus connection over the shelf backplane. It is on the front panel and located on the extension mezzanine.

3.13.2 Signal Test Points

Due to the sensitive nature of multi-Gb/s signals, no test points are provided on PCB tracks intended to carry multi-Gb/s data. If such signals need to be examined, this must be done via firmware. Test points are placed on a selection of those data and control tracks that are not operating at multi-Gb/s.

For each FPGA, spare, general-purpose IO pins are routed to headers. Furthermore, spare multi-Gb/s transmitters and receivers are routed to SMA sockets. With appropriate firmware these connections allow internal signals, or copies of data received, to be fed to an oscilloscope, for example, or driven from external hardware.

The exact number of test connections, and those signals on which a test point can be placed most usefully, are to be determined in the final stage of module layout.

3.13.3 Ground Points

At least six ground points are provided, in exposed areas on the top side of the module, to allow oscilloscope probes to be grounded.
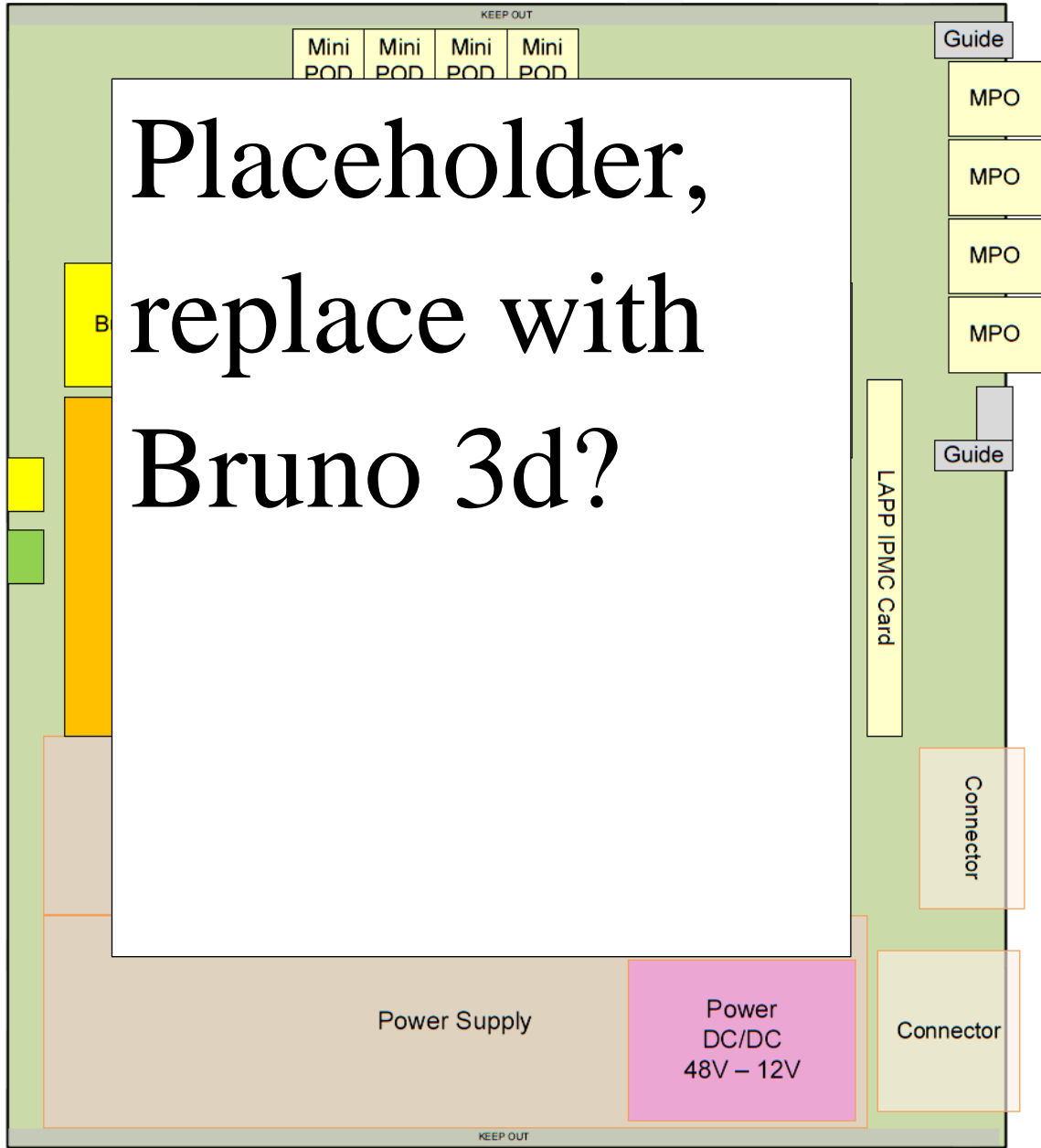
3.14 Floor plan

Figure 3 shows a preliminary floor plan of the L1Topo module. This will be used as a guide for the layout process; the exact location of components may change.

The routing of c. 300 signals at multi-Gb/s presents a significant challenge for the design of the L1Topo PCB. In order to minimise track lengths and routing complexity for these signals, the Avago MiniPOD receivers are placed around the Processor FPGAs. However, this creates an additional constraint on the layout: the need to accommodate routing paths for the fibre-optic ribbons carrying the data to these receivers. To connect the MPO connectors to the

571 receivers the ribbons need to twist, curve and bypass large heat sinks on the FPGAs. It can be
572 seen in Figure 3 that large components have been excluded from some areas of the floor plan,
573 to allow space for the routing of the fibre-optic ribbons.

574 In addition to those components shown in Figure 3, glue logic is placed on the underside of
575 the module.

576

577 **Figure 3.   A floor plan of the L1Topo, showing a preliminary placement guide.**

4 Front-Panel Layout—update!

Figure 4.   Preliminary front panel layout (not to scale).

Figure 4 shows a preliminary template for the front panel layout of the L1Topo. Shown are the JTAG port for boundary scanning and FPGA access, an auxiliary Ethernet control port, status LEDs and the ATCA extraction/insertion handles. These components are not drawn to scale.

5 Related Documents

[1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-018, http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf

[1.2] L1Calo Phase-I Hub Specification

[1.3] L1Calo Phase-I ROD specification *(https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/Hub-ROD_spec_v0_9.pdf)*

[1.4] L1Calo Phase-I eFEX Specification *(https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/eFEX_spec_v0.2.pdf)*

[1.5] L1Calo Phase-I jFEX Specification *()*

[1.6] L1Calo Phase-I gFEX Specification *()*

[1.7] L1Calo Phase-I Optical Plant Specification

[1.8] ATCA Short Form Specification, http://www.picmg.org/pdf/picmg_3_0_shortform.pdf disappeared, now only http://www.powerbridge.de/download/know_how/ATCA_Short_spec.pdf

[1.9] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*, http://www.picmg.com/

[1.10] L1Calo High-Speed Demonstrator report *(https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/HSD_report_v1.02.pdf)*

[1.11] Foxconn 14Gb/s MiniPOD devices *http://www.fit-foxconn.com/Product/ProductDetail?topClassID=&&PN=AFBR-824VXYZ*

609 [1.12] Development of an ATCA IPMI controller mezzanine board to be used in the ATCA
610   developments for the ATLAS Liquid Argon upgrade,
611   http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf

612 6 Glossary

ATCA	Advanced Telecommunications Computing Architecture (industry standard).
BC	Bunch Crossing: the period of bunch crossings in the LHC and of the clock provided to ATLAS by the TTC, 24.95 ns.
DAQ	Data Acquisition.
DCS	Detector Control System: the ATLAS system that monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.
ECAL	The electromagnetic calorimeters of ATLAS, considered as a single system.
eFEX	Electromagnetic Feature Extractor.
FEX	Feature Extractor, referring to either an eFEX, gFEX or jFEX module or subsystem.
FIFO	A first-in, first-out memory buffer.
FPGA	Field-Programmable Gate Array.
HCAL	The hadronic calorimeters of ATLAS, considered as a single system.
IPBus	An IP-based protocol implementing register-level access over Ethernet for module control and monitoring.
IPMB	Intelligent Platform Management Bus: a standard protocol used in ATCA shelves to implement the lowest-level hardware management bus.
IPM Controller	Intelligent Platform Management Controller: in ATCA systems, that portion of a module (or other intelligent component of the system) that interfaces to the IPMB.
IPMI	Intelligent Platform Management Interface: a specification and mechanism for providing inventory management, monitoring, logging, and control for elements of a computer system. A component of, but not exclusive to, the ATCA standard.
jFEX	Jet Feature Extractor.
JTAG	A technique, defined by IEEE 1149.1, for transferring data to/from a device using a serial line that connects all relevant registers sequentially. JTAG stands for Joint Technology Assessment Group.
L0A	In Run 4, the Level-0 trigger accept signal.
L0Calo	In Run 4, the ATLAS Level-0 Calorimeter Trigger.

L1A	The Level-1 trigger accept signal.
L1Calo	The ATLAS Level-1 Calorimeter Trigger.
LHC	Large Hadron Collider.
MGT	As defined by Xilinx, this acronym stands for Multi-Gigabit Transceiver. However, it should be noted that it denotes a multi-gigabit transmitter–receiver pair.
MiniPOD	An embedded, 12-channel optical transmitter or receiver.
MicroPOD	An embedded, 12-channel optical transmitter or receiver, smaller compared to the MiniPOD.
MPO	Multi-fibre Push-On/Pull-Off: a connector for mating two optical fibres.
PMA	Physical Media Attachment: a sub-layer of the physical layer of a network protocol.
ROD	Readout Driver.
RoI	Region of Interest: a geographical region of the experiment, limited in η and ϕ, identified by the Level-1 trigger (during Run 3) as containing candidates for Level-2 trigger objects requiring further information. In Run 4, RoIs are used in the same between the Level-0 and Level-1 triggers.
Shelf	A crate of ATCA modules.
SMA	Sub-Miniature version A: a small, coaxial RF connector.
Supercell	LAr calorimeter region formed by combining E_T from a number of cells adjacent in η and ϕ.
TOB	Trigger Object.
TTC	The LHC Timing, Trigger and Control system.
XTOB	Extended Trigger Object. A data packet passed to the readout path, contained more information than can be accommodated on the real-time path.

613 # 7 Document History

Version	Comments
0.7	Internal circulation without mezzanine section

8 Summary : Interfaces

Some important details of interfaces to external systems as described above are summarized in this section.

8.1 Internal Interfaces

Do we want that section for eg. Mezzanine connectors ?

8.2 External Interfaces

8.2.1 Electrical TTC interface (backplane input)

A clean clock of 40.079MHz is received as a differential electrical signal via the ATCA backplane. The signal is AC-coupled on the extension mezzanine and routed into an "any-in" differential receiver or a jitter cleaner????

The clock is accompanied by a TTC data signal, differential, AC coupled on the mezzanine, electrically compatible to Xilinx MGT. The data rate is assumed to be 3.2Gb/s, 8b/10b encoded. Format being defined by the hub designers.

Data paths supported from both hub slots 1 and 2.

8.2.2 Electrical DAQ interface (backplane output)

Readout data are sent to the DAQ via ATCA backplane on 6 links, LHC bunch clock synchronous(?) AC coupled on L1Topo, Xilinx MGT compatible, below 10Gb/s. Data paths are supported into both hub slots 1 and 2. The data formats are being defined by the hub/ROD community. Readout paths supported from both FPGAs to both hub slots, ie. a total of 4 times 2+1spare link.

8.2.3 IPbus interface (backplane I/O)

Module control links are standard Gigabit Ethernet via the backplane from/to hub slot 1. The phy chip is located on the extension mezzanine. The envisaged phy chip (VSC8221) allows for magnetics-free, capacitive coupling, which will be the baseline.

8.2.4 DCS interfaces (backplane I/O)

The IPMC module is linked to the outside world via an I2C (IPMB) bus in ATCA Zone1, and a standard Ethernet link to hub slot 2 via the base interface.

8.2.5   Electrical CTP interface (front panel output)

The Central Trigger Processor is interfaced electrically via a VHDCI SCSI style connector. Pinout is unchanged with respect to the Phase-0 L1Topo module. Signals level is LVDS. All signal pairs can be driven from the two processor FPGAs. The allocation of pairs to individual FPGAs is implemented on the extension mezzanine. The interface is assumed to be data lines only, though parity and clock signals could be generated in FPGAs if required. The signal level is LVDS.

8.2.6   Optical CTP interface (front panel output)

The Central Trigger Processor is interfaced fibre-optically via an MTP/MPO connector on the front panel. Up to 48 total fibres can be driven from the two processor FPGAs through MiniPODs. The maximum bitrate is 14Gb/s, the interface is assumed to run at 6.4/12.8 Gb/s synchronous to the LHC clock. Data encoding is 8b/10b.

8.2.7   Optical FEX/Muon interface (rear input)

The calorimeter FEXes (e/j/g-FEX) and the muon trigger are fibre-optically interfaced via the backplane, on 72-way MTP/MPO connectors. The mechanical interface to the RTM is Molex MTP-CPI. Four of these shrouds are available in ATCA Zone3. The signals are routed through MiniPODs (up to 14 Gb/s) and received into FPGAs via GTH/GTY links. Encoding is 8b/10b. Data rate is specified for mixed operation 11.2/12.8Gb/s. Signal rates are not to be mixed in same quad.

9 Appendix : Data formats

The formats of the data received and generated by L1Topo are about to be finalised. Details are found in separate documents. This section gives a coarse overview only.

9.1   Real-Time Input Data

Real-time input from FEXes and Muon Trigger is 8b/10b-encoded at 11.2 or 12.8 Gb/s. This yields a line capacity of 224 or 256 bits total per bunch crossing. The raw data are accompanied by a CRC check sum and by comma characters, required for line synchronization. Comma characters are sent upon link start-up and in otherwise empty data fields, replacing 0x00 data bytes. Comma characters are injected in fixed and unique positions within a full-BC data word only. For purpose of overall alignment and monitoring bunch count information is embedded into the data stream as well.

9.2   Real-Time Output Data

The Real-time output of L1Topo into the CTP is composed of trigger information, accompanied by overflow information, one overflow bit per trigger bit (?). On the electrical interface this information is sent without any further formatting, as an 80Mb/s stream. On the optical interface the raw data will be protected by a CRC check sum and aligned with help of

---

676 embedded comma characters, plus overall alignment with embedded bunch count
677 information.

9.3   Backplane data formats

679 Readout streams into DAQ and RoI systems are routed through the two hub/ROD modules in
680 the shelf. The formats on the data links are defined by the ROD community. It should be
681 noted that it will not be possible to run all DAQ or RoI output in a channel bonded scheme,
682 since it is actually two separate streams from distinct sources, the two processor FPGAs.

683 The TTC data running on the backplane from the hub modules to the L1Topo modules are re-
684 coded on the hub. The exact protocol is being defined by the hub designer community.