Technical Specification

ATLAS Level-1 Calorimeter Trigger Upgrade

Topology Processor (L1Topo)

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Draft

Version: 0.0

13 February 2017

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1 Related Documents

[1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-018, http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf

[1.2] L1Calo Phase-I Hub Specification

[1.3] L1Calo Phase-I ROD specification (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/Hub-ROD_spec_v0_9.pdf*)

[1.4] L1Calo Phase-I eFEX Specification (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/eFEX_spec_v0.2.pdf*)

[1.5] L1Calo Phase-I jFEX Specification *()*

[1.6] L1Calo Phase-I gFEX Specification *()*

[1.7] L1Calo Phase-I Optical Plant Specification

[1.8] ATCA Short Form Specification, http://www.picmg.org/pdf/picmg_3_0_shortform.pdf

[1.9] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*, http://www.picmg.com/

[1.10] L1Calo High-Speed Demonstrator report (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/HSD_report_v1.02.pdf*)

[1.11] Development of an ATCA IPMI controller mezzanine board to be used in the ATCA developments for the ATLAS Liquid Argon upgrade, http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf

2 Conventions

The following conventions are used in this document.

A programmable parameter is defined as one that can be altered by slow control, for example, between runs, not on an event by event basis. Changing such a parameter does not require a re-configuration of any firmware.

Where multiple options are given for a link speed, for example, the readout links of the jFEX are specified as running up to 10 Gb/s, this indicates that the link speed has not yet been fully defined. Once it is defined, that link will use a single speed. All links on the L1Topo will run at a fixed speed in the final system. but not all same speed!?

In accordance with the ATCA convention, a crate of electronics here is referred to as a shelf.

Where the term L1Topo is used here, without qualification, it refers to the L1Topo module. The L1Topo subsystem is always referred to explicitly by that term.

3 Introduction

This document describes the specifications for the upgrade of the Level-1 topology processor module (L1Topo) of the ATLAS Level-1 Calorimeter Trigger Processor (L1Calo) [1.1] . A L1Topo processor has initially been introduced into the ATLAS trigger for Phase-0 during Run-2 to improve trigger performance by correlating trigger objects (electromagnetic clusters, jets, muons) and global quantities.

The new L1Topo will be installed in L1Calo during the long shutdown LS2, as part of the Phase-1 upgrade, and it will operate during Run 3. It is built to be forward compatible and may remain in the system after the Phase-2 upgrade in LS3, being operated in Run-4 as L1Topo or L0Topo, dependent on the eventual trigger architecture in Phase-2.

The ATLAS Phase-1 Level-1 Trigger system comprises eFEX, jFEX, and gFEX subsystems as calorimeter data sources for L1Topo. They are providing trigger object data, "TOBs", to L1Topo via optical fibre bundles. Another source of trigger objects is the ATLAS muon trigger subsystem.

L1Topo is a set of ATCA modules, operated in a single ATCA shelf, compliant with ATLAS and L1Calo standards. Real-time data are received via optical fibres exclusively. L1Topo runs a large number of concurrent and independent algorithms on the input data, to derive a number of trigger bits, typically one result bit and one overflow bit per algorithm. The result bits are forwarded to the Central Trigger Processor, which correlates these bits with further trigger and machine data to generate Level-1 Trigger and associated data words, to be transmitted back to the detector. Outputs to CTP are available via electrical and optical data paths.

The non-real-time data paths of L1Topo are basically identical to the L1Calo modules built for Phase-1: data are sent into the readout and the 2^{nd} level Trigger via L1Calo RODs over the backplane of the ATCA shelf. Control and global timing are accomplished via the backplane as well. To that end L1Calo communicates with two hub/ROD modules located in dedicated slots of the L1Topo shelf.

The Phase-1 Level-1 trigger system and the role of L1Topo within the Level1Calo system is described elsewhere in detail. Material on current Phase-0 L1Topo construction and performance is available as well.

4 Functionality

Figure 1 shows a block diagram of the L1Topo. The various aspects of L1Topo functionality are described in detail below. Implementation details are given in section 5.

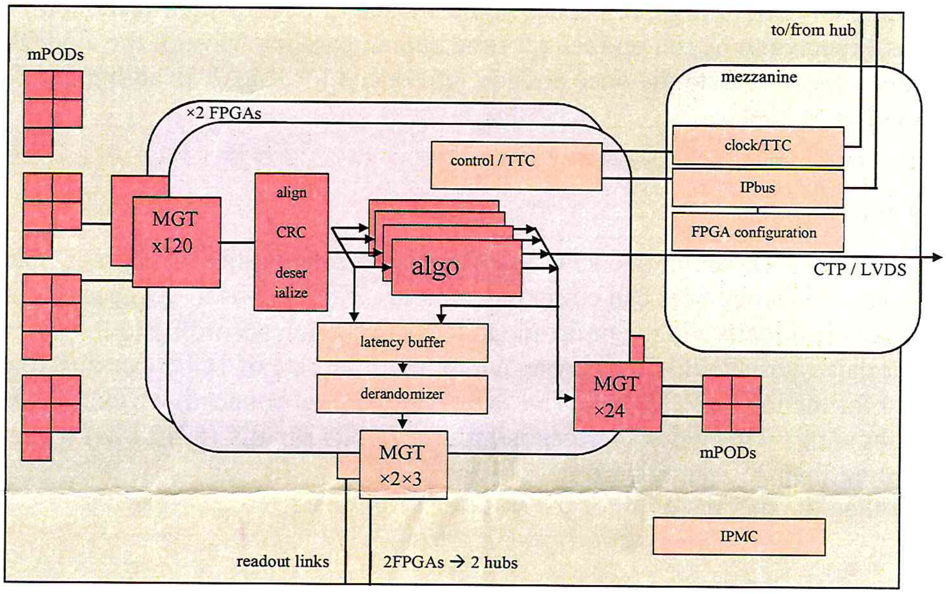

Figure 1. A block diagram of the L1Topo module.

4.1 Real-Time Data Path

ATCA Backplane zone 3 of L1Topo is used for real-time data transmission. The input data enter L1Topo optically through the backplane. The fibres are fed via four blind-mate backplane connectors that carry 48 fibres each. The optical signals are converted to electrical signals in 12-fibre receivers. For reason of design density miniPOD receivers are used. The electrical highspeed signals are routed into two FPGAs, where they are de-serialized in MGT receivers; the parallel data are presented to the FPGA fabric. The two FPGAs operate on their input data independently and in parallel. High bandwidth, low latency parallel data paths allow for real-time communication between the two processors. The signal results are transmitted towards the CTP on both optical fibres and electrical cables. The electrical signals are routed via an extension mezzanine module.

x or 72 ?!
total 240

4.1.1 Input Data

L1Topo will receive the topological output data of the sliding window processors from L1Calo and data from the L1Muon system. The data format transmitted into L1Topo comprises of TOB data (Trigger Object data) for jets, clusters and muons. The data will consist of a description of the position of an object (jet, e/m cluster, tau and muons) along with some qualifying information, like the energy sum within the object.

4.1.2 Algorithms

Due to the large amount of logic resources in the chosen FPGAs, a significant number of algorithms is expected to be run on the real-time data in parallel. Most of the algorithms will be identical or very similar to the once already introduced for Run-2. In addition, a few new algorithms will be added.

4.1.3 Data Sharing

Topology data are processed in two FPGAs. There is no data duplication implemented at PCB level. The two processors can communicate via a parallel bus to get access to data that cannot be received directly via the multi-gigabit links. Though according to the device data sheets higher data rates should be possible, a maximum bit rate of 1Gb/s per differential pair is anticipated for the inter-FPGA link. That will limit parallel connectivity to 238 Gb/s of aggregate bandwidth. This would correspond to 24238 bits per BX (5712 bits) which allow for sharing more than 250 generic trigger objects (TOBs).
This is more than the outputs of all of the sort trees combined.

4.1.4 Output

The real-time output data of the L1Topo to the CTP consist of individual bits indicating whether a specific algorithm passed or not plus an overflow bit. The resulting trigger data are expected to exhibit a rather small volume. They will be transmitted to CTP optically or electrically. A single fibreoptical ribbon connection per processor FPGA, running through the front panel of the module is provided for this purpose. A mezzanine board will be required to interface L1Topo to the CTPCORE module electrically via 32 LVDS signals at low latency.

4.2 Error Handling

The data received by the L1Topo from the Calorimeters are accompanied by a CRC code. This is checked in the Processor FPGAs, immediately after the data are converted from serial, multi-Gb/s streams into parallel data. If an error is detected, the following actions are performed:

- All data to which a detected error pertains are suppressed (i.e. set to zero) on the real-time path. They are passed to the readout path as received.
- The Error Check Result for the current clock cycle is formed from the 'OR' of all error checks for the current bunch crossing.

- The Input Error Count is incremented for any clock cycle where there is at least one error in any input channel.
- A bit is set in the Input Error Latch for any channel that has seen an error. These bits remains set until cleared by an IPBus command.
- The global Input Error bit is formed from the 'OR' of all bits in the Input Error Latch.

The Error Check Result, Input Error Count, Input Error Latch and Input Error bit can all be read via IPBus. A single IPBus command is provided to clear all of these registers. The Error Check Result and Input Error Count are included in the readout data for the current bunch crossing. The L1Topo does not generate any other external error signal, so data monitoring or regular hardware scanning must detect an error condition.

4.3 Latency

A breakdown of the estimated latency of the real-time path of the L1Topo is given in the ATLAS TDAQ System Phase-1 Upgrade Technical Design Report [1.1] .

4.4 Readout Data Path

On receipt of an L1A signal, the L1Topo provides data to a number of systems: in Run 3, it provides RoI data to Level-2; in Run 4, it provides RoI data to L1Track and L1Calo (the L1Topo being part of L0Calo in Run 4); in both Run 3 and Run 4, it provides data to the DAQ system. Collectively, these data are referred to here as readout data.

The L1Topo outputs a single stream of readout data, which contains the superset of the data required by all of the downstream systems. In Run 3, these data are transmitted across the crate backplane to a ROD. In Run 4, there are two RODs per crate and the L1Topo transmits identical readout data to both RODs. It is the RODs that are responsible for formatting the data as required by the downstream systems, and handling the multiple interfaces.

For each event that is accepted by the Level-1 trigger, the L1Topo can send three types of data to the readout path: final TOBs, expanded TOBs (XTOBs) and input data. The final TOBs are copies of those transmitted to L1Topo. In normal running mode these are the only data read out. The XTOBs are words that contain more information about trigger candidates than can be transmitted on the real-time data path. They are extracted from the real-time path before the merging process and therefore, as merging may reduce the number of TOBs, the number of XTOBs may be larger than the number of TOBs. To minimise the amount of readout data generated, XTOBs are not normally read out. However, this functionality can be enabled via the slow control interface. This cannot be done dynamically for individual events.

The input data comprise all data received from the calorimeters. They are copied from the real-time path after serial-to-parallel conversion and after the CRC word has been checked. There are a number of programmable parameters, set via slow control, that determine which input data are read out. These are as follows.

- The Input Readout mode: by default, only input data from fibres that have generated an error are read out. However, the readout of data received without error can also be enabled.

- The Input Channel Mask: the read out of individual channels of input data, from individual FPGAs, can be disabled. A channel here means the data received at an FPGA from one fibre. In total, a Processor FPGA on the L1Topo receives up to 104 channels of input data. However, many of these data are redundant copies, created because of the need to fan out data between the FPGAs. The Input Channel Mask provides a way of stripping redundant channels from the L1Topo readout. It also allows data from permanently broken links to be excluded from the readout process.
- The Input Readout Veto: this veto is asserted for a programmable period (0-256 ticks) after the read out of any Input Data. It provides a means of pre-scaling the amount of Input data read out, preventing it from overwhelming the readout path.

The mechanism for capturing readout data is illustrated in Figure 2. For every bunch crossing all input data, intermediate and final TOB data are copied from the real-time path and written to scrolling, dual-port memories. They are read from these memories after a programmable period, of up to 3 μs. At this point they are selected for readout if they meet both of the following criteria: an L1A pertaining to them is received, and they are enabled for readout by the control parameters described above. Otherwise, they are discarded.

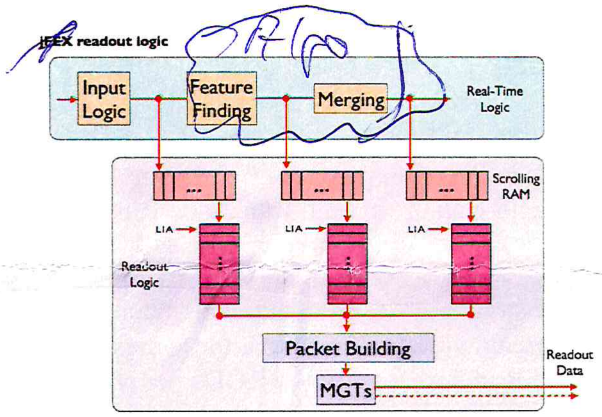

Figure 2. A functional representation of the L1Topo readout logic.

For each L1A, data from a time frame, programmable via control parameters, can be read out. The selection of data for read out is a synchronous process with a fixed latency, and it is the period for which data are held in the scrolling memories that determines the start point of this time frame. The correct value must be determined when commissioning L1Calo (it should correspond to the period from when the data are copied into the scrolling memories, to when an L1A pertaining to those data is received at the L1Topo, plus or minus any desired offset in the time frame). The L1Topo hardware allows the read out of overlapping time frames. At low rates (including everything before Run 4) the L1Topo does not expect to read out overlapping time frames, still the firmware will be able to provide this if required. At high rates, the read out of overlapping time frames will be more likely, but the frame length and trigger rate will need to be controlled carefully to prevent buffer overflow.

It is possible that for a BC there will be no TOB data (or XTOB data when enabled) to be captured. In such cases a control word is inserted into the readout path to indicate this. This word, which is used for flow-control, is internal to the L1Topo; it is not passed to the ROD.