

algo

MGT  
x120

align   
 CRC  
  
deserialize

latency buffer

derandomizer

MGT  
×2×3

MGT  
×24

×2 FPGAs

mezzanine

CTP / LVDS

mPODs

mPODs

control / TTC

clock/TTC

IPbus

readout links 2FPGAs 🡪 2 hubs

FPGA configuration

IPMC

to/from hub