ATLAS Level-1Trigger

L1Topo Module

- V1.0 (Prototype) -

Project Specification

Version 0.22

Date: 23/05/2012 16:57:15

Bruno, Eduard, Uli, Weina

Universität Mainz

Table of Contents

1 Introduction

This document describes the specification for the prototype of the Level-1 topology processor module (L1Topo). The specification covers the processor main board as well as the mezzanine modules. Section 1 of this document gives an overview of the module. Section 2 describes the functional requirements. Section 3 details the implementation.

1.1 Related projects

L1Topo is a major processor module within the future Cluster, Jet and Muon Processor scheme of the ATLAS level-1 trigger. L1Topo will from 2013/14 be located between the CMX and the CTP in the L1Calo architecture. The muon trigger will supply a small amount of signals into L1Topo in an initial phase. Additional connectivity will be available in upgrade phase 1.

TTC	http://www.cern.ch/TTC/intro.html
L1Calo modules	http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html
TTCDec	http://hepwww.rl.ac.uk/Atlas-L1/Modules/Components.html
CTP	http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/ctpttc/L1CTP.html
CMX	http://ermoline.web.cern.ch/ermoline/CMX
Muon Trigger	http://

1.2 L1Topo processor board

The Topological Processor will be a single processor crate equipped with one or several processor modules. The processor modules will be identical copies, with firmware adapted to the specific topologies to operate on.

L1Topo will receive the topological output data of the sliding window processors. The details of the data formats are not yet finally defined. However, the information transmitted into L1Topo will be basically comprised of the ROI data that are currently transmitted to the 2nd level trigger. The data will consist of a description of the position of an object (jet, e/m cluster, and tau) along with some qualifying information, basically the energy sum within the object. Preliminary data formats have been devised. Data are going to be transmitted on optical fibres. After conversion to electrical representation, data are received and processed in FPGAs equipped with on-chip Multi-Gigabit Transceivers (MGT). Results are sent to the Central Trigger processor (CTP). The L1Topo module will be designed in AdvancedTCA (ATCA) form factor.

1.2.1 Real-time data path

ATCA Backplane zone 3 of L1Topo is used for real-time data transmission. The input data enter L1Topo optically through the backplane. The fibres are fed via four to five blind-mate backplane connectors that can carry up to 72 fibres each. In the baseline design 48-way connectors will be used. The optical signals are converted to electrical signals in 12-fibre receivers. For reason of design density miniPOD receivers will be used. The electrical high-speed signals are routed into two FPGAs, where they are de-serialised in MGT receivers; the parallel data are presented to the FPGA fabric. The two FPGAs operate on their input data independently and in parallel. High bandwidth, low latency parallel data paths allow for real-time communication between the two processors. The final results are transmitted towards the CTP on optical fibres. Some limited bandwidth of low latency, electrical connectivity can be made available via a mezzanine module.

The operation of the real-time data path requires low-jitter clocks throughout the system. For synchronous operation, data transmitters will have to be operated with clean multiples of the LHC bunch clock. Receiver reference clocks may as well be derived from local crystal oscillators, though tight limits on the frequency range will have to be observed. The L1Topo module will be designed for 40.08 MHz operation of the real-time data path only.

Figure 1 shows a conceptual drawing of L1Topo. The real-time processor FPGAs are labelled A and B. They are surrounded by the optical receivers. Non-real-time module control functionality is implemented FPGA C. More detailed diagrams are shown in section 3.

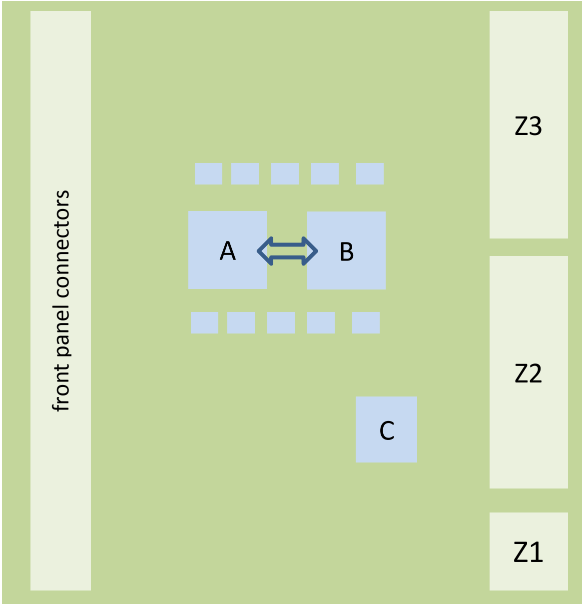

Figure 1: L1Topo module

1.2.1.1 Data reception

The optical data arrive on the main board on 12-fibre ribbons. Since the backplane connectors support multiples of 12 fibres, the optical signals will be routed via "octopus" cable sets, splitting 24, 36, 48, or 72 fibres into groups of 12. It should be noted that un-armed, bare fibre bundles are very flexible and can easily be routed to their destination, even in high-density designs. However, they need to be protected from mechanical stress. The opto-electrical conversion will be performed in Avago miniPOD 12-channel devices. The opto receivers exhibit programmable pre-emphasis so as to allow for improvement on signal integrity for given track length.

After just a few centimetres of electrical trace length, the multi-gigabit signals are de-serialised in the processor FPGAs. They allow for programmable signal equalization on their inputs. The exact data formats are as yet undefined, though standard 8b/10b encoding is envisaged for purpose of run length limitation and DC balance. The processors are supplied with required bias and termination voltages, as well as a suitable reference clock.

1.2.1.2 Data processing

Topology data are processed in two FPGAs. There is no data duplication implemented at PCB level. Therefore two different schemes can be employed. The two processors can communicate via their fabric interface to get access to data that cannot be received directly via the multi-gigabit links. Though according to the device data sheets higher data rates should be possible, a maximum bit rate of 1Gb/s per differential pair is anticipated for the inter-FPGA link. That will limit parallel connectivity to about 190 Gb/s of aggregate bandwidth. Since this data path adds approximately one bunch tick of latency, it might be more attractive to fan out data electrically or optically at the source, should both processors need to be supplied with the same data.

Due to the large amount of logic resources in the chosen FPGAs, a significant number of algorithms is expected to be run on the real-time data in parallel. The resulting trigger data are expected to exhibit a rather small volume. They will be transmitted to the CTP optically.

A single fibre-optical ribbon connection per processor FPGA, running through the front panel of the module is provided for this purpose. An adapter board will be required to interface L1Topo to the CTP via a small number of electrical LVDS signals at low latency. In case of serious latency issues such a direct interconnect can be useful if a direct electrical connection into the CTP core FPGA can be made.

1.2.2 Clock distribution

Both the FPGA fabric and the multi-Gigabit transceivers (MGT) need to be supplied with clock signals of appropriate signal levels and signal quality. The fabric clocks run at the LHC bunch clock frequency of 40.08MHz at LVDS levels. The MGT clocks are CML level signals, AC-coupled into the MGT clock pads of the FPGAs. The jitter of the MGT clocks has to be tightly controlled. Clock generation and jitter clean-up are performed on the L1Topo main board. The clock distribution trees are located close to the processor FPGAs. The clock fan-out chips chosen are devices with multiple signal level input compatibility, and output levels suitable for their respective use, either LVDS or CML.

There are two independent clock trees for the fabric clocks into all FPGAs. There are two MGT clock trees into all FPGAs. This allows for both crystal based and LHC wide clocks to be distributed on the module. The control FPGA receives additional local clocks since it handles DAQ, ROI, and control links as well.

The current L1Calo modules receive their LHC bunch clock and associated data through the TTCDec module, based on a TTCRx chip. Future LHC bunch clock distribution might differ from this scheme. L1Topo will have to operate with the existent clock distribution scheme initially. At a later stage it will probably be driven in a different way. For backward compatibility a TTCDec module will be mounted on L1Topo. It will be wired to the control FPGA. Alternative optical LHC clock paths will be possible via a mezzanine module. The spare optical inputs of DAQ and ROI SFP modules (see below) are available to route LHC clock and data into L1Topo.

For reason of signal integrity on the multi-Gibgabit real-time path any clock used for data transmission will have to be conditioned for low jitter. A PLL-based jitter cleaner device will be employed in the MGT reference clock path. .

1.2.3 Configuration, monitoring, and control

While the L1Topo prototype is meant to be very close to future production modules, there is still some uncertainty about FPGA configuration and module control on future Level-1 trigger modules.

1.2.3.1 Pre-configuration access

L1Topo is a purely FPGA-based ATCA module. There are no dedicated communications processors available on the module. Therefore there is only a single control path predefined that could possibly allow for access to a module with un-configured FPGA devices. This is the I2C port (IPMB) available on all ATCA modules in zone 1 (see below). Also CAN (see below) could be an option for pre-configuration access. Due to the very limited bitrates on these two networks, neither of them is considered suitable for initial access in case of failure of configuration circuitry. FPGA configuration with up to the order of 100Mb of configuration would be impossible to achieve through a service network of just hundreds of kilobits per second bandwidth.

For this reason L1Topo will be equipped with an FTDI USB microcontroller which supports 480Mb/s USB high-speed mode. The microcontroller is interfaced to the FPGAs via JTAG protocol. The microcontroller design is fully compatible to commercial Xilinx evaluation platforms. Therefore the crucial operation of FPGA configuration is available from both Linux and Windows without the need for any software to be written. Either production firmware or service code can be loaded to the FPGAs, as required. Debug with the Xilinx Chipscope tool set will be supported out of the box. JTAG user access to the FPGAs will be possible with a sustained rate of several Megabits per second. However, some application software would need to be written for this purpose.

On the L1Topo prototype the USB sub-system will be built on a tiny mezzanine module, though it is envisaged to make this pre-configuration and debug access port available as an integral part of future L1 ATCA production modules.

1.2.3.2 FPGA configuration

The baseline (legacy) FPGA configuration scheme on L1Topo is via a CompactFlash card and the Xilinx System ACE chip. This configuration scheme has been successfully employed on several L1Calo modules so far, including the JEM. On the JEM the required software and firmware has been devised to allow for in-situ update of the CompactFlash images. The required board-level connectivity will be available on L1Topo, to write the flash cards through some network connection to the FPGAs, once they are configured. The inevitable bootstrap problem is solved through the USB based pre-configuration access scheme described above.

A local SPI memory will allow for an alternative configuration method for the control FPGA. This FPGA does not contain any algorithmic firmware and is therefore not expected to be updated particularly often. The processor FPGAs will be configured off a parallel flash memory, which in turn is sequenced by the control FPGA. In-situ configuration update will be possible via IP access to the control FPGA.

1.2.3.3 Environmental monitoring

Board level temperature and voltage monitoring will be a requirement on future L1 modules. The current L1Calo modules are monitored via CAN bus. The default ATCA monitoring and control path is via I2C links in zone 1. For L1Topo both monitoring paths are envisaged. The backplane I2C link (IPMB) is run via an IPMB compatible driver into the control CPLD. ??? This CPLD is basically used for a further stage of routing only. The I2C controller can be located either in the control FPGA or inside a microcontroller located on a mezzanine module. It will be possible to mount a CAN microcontroller on a future version of the control mezzanine. The required connectivity is available on the mezzanine socket. Initially an FPGA based state machine will handle the I2C connection. On L1Topo only configured FPGAs can be monitored for die temperature and internal supply voltage. This is achieved by the use of their built-in system monitor. These measurements might be complemented by board-level monitoring points, if required ?????.

1.2.3.4 Module control

On standard ATCA modules, IP connectivity is mandatory for module control. This is generally provided by two 10/100/1000 Ethernet ports on the backplane in zone 2 (redundant base interface). This is a requirement for an ATCA compliant backplane, but not for an ATCA compliant module. The module is free to ignore the Ethernet ports and provide IP connectivity by any suitable means. On a future L1Topo ATCA crate one would probably avoid wiring two slots exclusively to the two base interface ports. On L1Topo a few differential signal pairs towards the bottom of the module are reserved for module access via Ethernet, PCIe, or other connectivity. The respective lines are wired to the control mezzanine, where the required connectivity can be made to a local microcontroller, an SGMII Phy device, or straight into an MGT link on the control FPGA. A dedicated SFP based control link into the control FPGA will transport module control signals initially. It will be connected into an optical VME bus extender, so as to allow controlling L1Topo from a VME crate CPU within the current L1 online software empire.

1.2.3.5 DAQ and ROI

Since L1Topo would be used in the existent pre-phase-1 environment initially, a scheme for transmitting event data into the ATLAS data acquisition and 2nd level trigger was made compatible to the existent L1Calo modules. It is assumed that DAQ/ROI wise L1Topo would live in the L1Calo ecosystem and compatibility to L1Calo RODs is mandatory. A single optical channel into each the DAQ and ROI RODs is provided. The optical interface is made via SFP sockets.

2 Functional requirements

This section describes the functional requirements only. Specific rules need to be followed with respect to PCB design, component placement and decoupling. These requirements are detailed in section 3. For requirements on interfaces with other system components, see section 5.

2.1 Signal paths

L1Topo is designed for high speed differential signal transmission, both on external and internal interfaces. Two differential signalling standards are employed: LVDS and CML. For requirements regarding signal integrity see sect. 3.3.

2.2 Real-time data reception

Real-time data are received optically from the back of the ATCA shelf; they are converted to electrical representation, transmitted to the processors and de-serialised in on-chip MGT circuits.

The requirements with respect to data reception and conditioning are:

- Provide five MPO/MTP compatible blind-mate fibre-optical backplane connectors in ATCA zone 3
- Route bare fibre bundles to 12-channel opto receivers
- Supply opto-electrical components with appropriately conditioned supply voltages
- Connect single ended CMOS level control lines to the control FPGA
- Provide suitable coupling capacitors for multi-Gigabit links
- Run the signal paths into the processors

2.3 Real-time data processing

The L1Topo processing resources are partitioned into two processors. This is a consequence of limitations on MGT link count and processing resources on currently available FPGAs. The requirements on processing resources depend on the physics algorithms and are not currently known.

The requirements with respect to the processors are:

- Provide an aggregate input bandwidth of 160 GB/s (payload) into the processors
    - 160 channels of up to 10 Gb/s line rate
- Process the real-time data in a 2-stage (maximum) processing scheme (data might need to cross chip boundary between the two processors)
- Allow for footprint compatible medium- and high-end FPGAs for scalability of processing resources
- Minimise latency on chip-to-chip data transmission
- Maximise bandwidth between the two processors
    - Send bulk output data to CTP on MGT links, so as to maximise low-latency inter-processor communication bandwidth
    - Use higher latency channels for non-RTDP links where possible
- Provide an aggregate bandwidth of up to 24 GB/s (payload) on MGT outputs towards the CTP
    - 24 channels of up to 10Gb/s line rate
    - Additional 48-channel low latency electrical (LVDS) port

2.4 Clock distribution

Both the FPGA fabric and the MGT links need to be supplied with suitable clock signals. Due to the synchronous, pipelined processing scheme most of the FPGA-internal clocks need to be derived from the LHC bunch clock or a device emulating it. Due to requirements on MGT reference clock frequency accuracy, a mixed 40.00/40.08 MHz operation is impossible. Therefore a requirement for 40.08 MHz operation has to be introduced.

The requirements with respect to the clock distribution on the main board are:

- Provide the FPGAs with clocks of multiples of either a 40.08MHz crystal clock, or the LHC bunch clock
- Receive a TTC signal from backplane zone 2
- Receive an optical TTC signal from the front panel
- Recover TTC clock and data on a TTCdec mezzanine module
- Allow for clock conditioning hardware in the clock path
- Provide a common MGT crystal clock to all FPGAs.
- Provide a common MGT TTC-based clock to all FPGAs
- Connect the MGT clocks to the processor FPGAs such that the central quad of 3 quads is supplied. This rule must be followed such that the requirements are met, whether a smaller or larger device is mounted.
- Provide two fabric clocks to all FPGAs (40.08 crystal, bunch clock)
- Provide a separate crystal based MGT clock to the control FPGA for use on the control link
- Provide a separate crystal based MGT clock to the control FPGA for use on the DAQ and ROI link outputs (40.00 MHz or multiple)
- Provide a separate crystal based 40.08 MHz (or multiple) MGT receive reference clock to the control FPGA on the receive section of the DAQ and ROI links, for use on future LHC bunch clock recovery circuitry (TTCDec replacement), and thus:
- Allow for the input portion of the DAQ and ROI transceivers to be used for optical reception of LHC clock and data

2.5 Configuration and JTAG

JTAG is used for board level connectivity tests, pre-configuration access, and module configuration. During initial board tests and later hardware failure analysis, JTAG access will be required to connect an automatic boundary scan system, generally when the module is on a bench, not in an ATCA shelf. Also the initial configuration of non-volatile CPLDs will be performed at that stage.

The requirements with respect to boundary scan and CPLD configuration are:

- Allow for the connection of a boundary scan system to all scannable components of L1Topo: FPGAs, CPLDs, System ACE, and mezzanine modules via standard JTAG headers, following the standard rules on pull-up, series termination, and level translation between supply voltage domains.
- Allow for CPLD (re)configuration, following the boundary scan tests, and occasionally on the completed system.
- There is currently no requirement known regarding integration of devices sourcing or sinking MGT signals externally, into the boundary scan scheme

Pre-configuration access and device configuration of the FPGAs is required at any time. USB access and the System ACE / CompactFlash configuration scheme are employed.

The requirements with respect to USB access and FPGA configuration are:

- Employ the standard System ACE configuration scheme to configure the FPGAs upon power-up
- Connect the System ACE external JTAG port into an USB-to-JTAG converter according to Xilinx KC705 configuration scheme
- Connect the USB processor to a front panel mini USB socket
- Alternatively connect the USB (data lines only) via the control mezzanine module to the zone2 backplane connector
- Allow for static control of the FPGA configuration port settings and read-back of the status via the control CPLD.

2.6 Module control

On ATCA modules serial protocols are used to achieve board level configuration and control. Typically Ethernet would be used to control module operation. On L1Topo any serial protocol compatible to Xilinx MGT devices can be used to communicate to the control FPGA, once it has been configured. Examples are SGMII / Ethernet, PCI-Express, or any application specific protocol. All board level control goes via the control FPGA.

The requirements with respect to general board control are:

- Provide an optical bidirectional channel from the front panel to a control FPGA MGT (control link)
- Provide four-lane access from zone 2 to the mezzanine, compatible to 10/100/1000 Ethernet, so as to allow for a Ethernet Phy to be mounted on the mezzanine module
- Provide two-lane access from the mezzanine on to the control FPGA (one MGT, bidirectional)
- Provide bi-directional connectivity between processors and control FPGA
- Provide unidirectional transmission from each processor to the control FPGA via four MGT lanes for additional monitoring bandwidth
- Provide an interconnect between control FPGA and control CPLD
- Provide a control bus to all opto-electrical transceivers (I2C and static control)

The CPLD is in charge of mainly static controls and low speed I2C fanout.
The requirements with respect to the CPLD are:

- Communicate to the general board control system via a bus to the control FPGA.
- Communicate to the IPMB port via I2C protocol
- Communicate to the System ACE sub-system so as to control FPGA configuration and allow for in-situ update of the CompactFlash card
- Control the static FPGA configuration control lines

2.7 DAQ and ROI

A single fibre for each DAQ and ROI transmission will be provided on L1Topo.
The requirements with respect to DAQ and ROI interface are:

- Provide an optical ROI output channel to the front panel
- Provide an optical DAQ output channel to the front panel
- Use standard SFP modules
- Connect them to MGTs on the control FPGA
- Provide a separate 40 MHz (or multiple) clock to the MGT quads driving DAQ and ROI fibres

2.8 Mezzanine board

The mezzanine module provides some connectivity and real estate for electrical real-time signalling and general control purposes. The requirements with respect to auxiliary controls on the mezzanine board are:

- Breakout and signal conditioning for electrical trigger signals
- Receive a CAN signal from backplane zone 2
- Receive a 4-pair Ethernet signal from backplane zone 2
- Connect the clock mezzanine to the control FPGA via a single MGT for purpose of module control
- Connect the clock mezzanine to the control FPGA via a LVDS level bus
- Connect the clock mezzanine to the control FPGA via a CMOS bus for purpose of static and slow controls

3 Implementation

This section describes the detailed implementation of the module and it specifies a set of design rules needed to comply with general signal integrity rules, as well as component specific requirements.

L1Topo is built in ATCA form factor. The main board is built as a ~20 layer PCB. The PCB is approximately 2mm thick and should fit ATCA standard rails. If required, the board edges would be milled down to the required thickness. A detailed block diagram of the real-time data path is shown in Figure 2.

Figure 2 – L1Topo real-time data path

3.1 Scalable design

L1Topo can be assembled with a choice of footprint compatible devices. Initially XC7VX485T will be mounted due to component availability. The most powerful device XC7VX690T will be mounted on later copies of the module. L1Topo needs to be designed such that all vital signals are run on signal pins available on the smaller device. The mezzanine module socket will to provide some spare connectivity to make sure that L1Topo functionality can be upgraded at a later stage by replacing the relatively inexpensive mezzanine module only.

3.2 Clock

The clock circuitry comprises various crystal clocks and a TTCdec clock mezzanine module for clock generation, a jitter cleaner for signal conditioning, and several stages of electrical fan-out. Various Micrel device types are used to drive and fan out clocks of LVDS and CML type at low distortion. All Micrel devices are sink terminated on-chip. A detailed block diagram of the clock path is shown in Figure 4.

Figure 3 – L1Topo clock distribution

3.3 Control

A detailed block diagram of control paths is shown in Figure 4.

Figure 4 – L1Topo control paths

3.3.1 Module control

L1Topo module control is initially done via a serially extended VME bus, as outlined above. This choice was made since such an operation will not require any access-mode specific online software to be written. The module is seen from a VME crate CPU as if it were a local VME module.

As soon as the required software environment is available, this access mode will be converted to standard Ethernet access. The required hardware components are available on L1Topo: The optical (SFP) link can be directly connected to any 1000BASE−SX Ethernet port. Also, there is the required space and connectivity available on the control mezzanine to connect the control FPGA to the electrical Ethernet port located on the backplane, via an SGMII Phy (M88E1111 or similar).

The use of Ethernet for module control has been extensively explored in a previous project. Both UDP and bare Ethernet schemes have been used. Reference implementations (hardware/firmware/software) are available.

Warning -- the electrical Ethernet on L1Topo will not be compliant with the ATCA base interface, unless backplane pin-out is chosen appropriately. The required documentation is not available to L1Topo module designers!

3.4 Board level issues: signal integrity, power supplies, and line impedances

L1Topo is a large, high-density module, carrying large numbers of high-speed signal lines of various signal levels. The module relies on single ended CMOS (3.3V), and differential (some or all of LVDS, PECL2.5, CML3.3, and CML2.5) signalling. System noise and signal integrity are crucial factors for successful operation of the module. Noise on operating voltages has to be tightly controlled. To that end, large numbers of decoupling capacitors are required near all active components. FPGAs are particularly prone to generating noise on the supply lines. Their internal SERDES circuitry is highly susceptible to noisy operating voltages, which tend to corrupt their high-speed input signals and compromise the operation of the on-chip PLL, resulting in increased bit error rates. To suppress all spectral components of the supply noise, a combination of distributed capacitance (power planes) and discrete capacitors in the range of nF to hundreds of μF are required. On the FPGAs there are capacitors included in the packages for decoupling of noise up to highest frequencies.

L1Topo base frequency is 40.08 MHz. Parallel differential I/O operates at multiples up to 1Gb/s. Multi-Gigabit (MGT) links operate at 6.4 or 10Gb/s. This is only possible on matched-impedance lines. Differential sink termination is used throughout. All FPGA inputs are internally terminated to 100Ω or to 50Ω||50Ω, according to the manufacturer’s guidelines. All lines carrying clock signals must be treated with particular care. In the appendix there is a checklist for the detailed module design.

4 Firmware, on-line software and tests

L1Topo is an entirely FPGA based module. For both hardware commissioning and operation a set of matching firmware and software will be required. These two phases are well separated and requirements differ considerably. Hardware debug and commissioning will require intimate knowledge of the hardware components and will therefore be in the hands of the hardware designers. Both firmware and software will be restricted to simple, non-OO code. Hardware language is VHDL, software is plain C. GUI based tools are not required and will not be supplied by the hardware designers. Module commissioning from a hardware perspective is considered complete once the external hardware interfaces, board level connectivity, and basic operation of the hardware devices have been verified. The hardware debug and commissioning will involve JTAG/boundary scan, IBERT/ChipScope tests, and firmware/software controlled playback/spy tests with any data source/sink device available. Initially the GOLD will be available for test vector playback on a small number of 12-fibre ports. At a later stage a CMX prototype module will be used as a data source.

Module control is initially via an opto fibre connection to a VMEbus module carrying SerDes devices and optical transceivers. The opto-electrical interface will be a SFP module with LC-type opto connectors. Control software will be based upon calls to the CERN VME library. SFP outputs provided for DAQ and ROI data transmission will be tested for bit errors and link stability only. No specific data formats will be tested on these links.

In parallel to the hardware debug and commissioning, higher level software and firmware will be developed for later operation of L1Topo. As far as control software is concerned, a board level control scheme for future trigger modules needs to be devised. This will most likely not follow the initial approach of VME serialisation.

The test environment available in the home lab will allow for simple real-time data path tests only. There is no hardware, software installation, nor expertise available to run any tests involving DAQ/RODs/ROSes. Therefore all system level tests will have to be done in an appropriately equipped L1Calo test lab. Currently the CERN test rig seems to be the only available option.

There will be a separate document on software and on algorithmic firmware produced at a later date.

5 Interfaces : connectors, pinouts, data formats

5.1 Internal interfaces

A mezzanine module is connected via a FMC style connector (Samtec SEAM on the mezzanine module, SEAF on L1Topo):

	J1										
	K	J	H	G	F	E	D	C	B	A	
1	CTRL10	GND	CTRL11	GND	CTRL12	GND	CTRL13	GND	CTRL14	GND	1
2	GND	DP58 RX	GND	DP40 RX	GND	DP22 RX	GND	DP10 TX	GND	DP1 RX	2
3	GND	DP58 RX	GND	DP40 RX	GND	DP22 RX	GND	DP10 TX	GND	DP1 RX	3
4	DP68 RX	GND	DP50 RX	GND	DP32 RX	GND	DP17 RX	GND	DP6 RX	GND	4
5	DP68 RX	GND	DP50 RX	GND	DP32 RX	GND	DP17 RX	GND	DP6 RX	GND	5
6	GND	DP59 RX	GND	DP41 RX	GND	DP23 RX	GND	DP10 RX	GND	DP2 RX	6
7	GND	DP59 RX	GND	DP41 RX	GND	DP23 RX	GND	DP10 RX	GND	DP2 RX	7
8	DP69 RX	GND	DP51 RX	GND	DP33 RX	GND	DP18 RX	GND	DP7 RX	GND	8
9	DP69 RX	GND	DP51 RX	GND	DP33 RX	GND	DP18 RX	GND	DP7 RX	GND	9
10	GND	DP60 RX	GND	DP42 RX	GND	DP24 RX	GND	DP11 RX	GND	DP3 RX	10
11	GND	DP60 RX	GND	DP42 RX	GND	DP24 RX	GND	DP11 RX	GND	DP3 RX	11
12	DP70 RX	GND	DP52 RX	GND	DP34 RX	GND	DP19 RX	GND	DP8 RX	GND	12
13	DP70 RX	GND	DP52 RX	GND	DP34 RX	GND	DP19 RX	GND	DP8 RX	GND	13
14	GND	DP61 RX	GND	DP43 RX	GND	DP25 RX	GND	DP12 RX	GND	DP4 RX	14
15	GND	DP61 RX	GND	DP43 RX	GND	DP25 RX	GND	DP12 RX	GND	DP4 RX	15
16	DP71 RX	GND	DP53 RX	GND	DP35 RX	GND	DP20 RX	GND	DP9 RX	GND	16
17	DP71 RX	GND	DP53 RX	GND	DP35 RX	GND	DP20 RX	GND	DP9 RX	GND	17
18	GND	DP62 RX	GND	DP44 RX	GND	DP26 RX	GND	DP13 RX	GND	DP5 RX	18
19	GND	DP62 RX	GND	DP44 RX	GND	DP26 RX	GND	DP13 RX	GND	DP5 RX	19
20	DP72 RX	GND	DP13 TX	GND	DP12 TX	GND	DP11 TX	GND	DP18 TX	GND	20
21	DP72 RX	GND	DP13 TX	GND	DP12 TX	GND	DP11 TX	GND	DP18 TX	GND	21
22	GND	DP63 RX	GND	DP45 RX	GND	DP27_RX	GND	DP14 RX	GND	DP1 TX	22
23	GND	DP63 RX	GND	DP45 RX	GND	DP27 RX	GND	DP14 RX	GND	DP1 TX	23
24	DP14 TX	GND	DP54 RX	GND	DP36 RX	GND	DP21 RX	GND	DP6 TX	GND	24
25	DP14 TX	GND	DP54 RX	GND	DP36 RX	GND	DP21 RX	GND	DP6 TX	GND	25
26	GND	DP64 RX	GND	DP46 RX	GND	DP28 RX	GND	DP15 RX	GND	DP2 TX	26
27	GND	DP64 RX	GND	DP46 RX	GND	DP28 RX	GND	DP15 RX	GND	DP2 TX	27
28	DP15 TX	GND	DP55 RX	GND	DP37 RX	GND	GND	GND	DP7 TX	GND	28
29	DP15 TX	GND	DP55 RX	GND	DP37 RX	GND	SCL1	GND	DP7 TX	GND	29
30	GND	DP65 RX	GND	DP47 RX	GND	DP29 RX	SDA1	DP16 RX	GND	DP3 TX	30
31	GND	DP65 RX	GND	DP47 RX	GND	DP29 RX	TDO1	DP16 RX	GND	DP3 TX	31
32	DP16 TX	GND	DP56 RX	GND	DP38 RX	GND	3V3	GND	DP8 TX	GND	32
33	DP16 TX	GND	DP56 RX	GND	DP38 RX	GND	TMS1	GND	DP8 TX	GND	33
34	GND	DP66 RX	GND	DP48 RX	GND	DP30 RX	TDI1	GND	GND	DP4 TX	34
35	GND	DP66 RX	GND	DP48 RX	GND	DP30 RX	TCK1	VCC	GND	DP4 TX	35
36	DP17 TX	GND	DP57 RX	GND	DP39 RX	GND	3V3	GND	DP9 TX	GND	36
37	DP17 TX	GND	DP57 RX	GND	DP39 RX	GND	GND	VCC	DP9 TX	GND	37
38	GND	DP67 RX	GND	DP49 RX	GND	DP31 RX	3V3	GND	GND	DP5 TX	38
39	GND	DP67 RX	GND	DP49 RX	GND	DP31 RX	GND	3V3	GND	DP5 TX	39
40	RES1	GND	RES1	GND	TRST_L1	GND	3V3	GND	CTRL16	GND	40

Figure 5: FMC pinout

The TTCdec clock mezzanine module is connected via an xx-pin connector (Samtec)

5.2 Front panel

The front panel shows the CompactFlash card for System ACE configuration, an electrical connector (LVDS) for CTP interconnect, and five optical connections: One MPO/MTP connector each for the real-time output to the CTP from the processor FPGAs, and an SFP opto module to each DAQ, ROI and VMEbus extender. Further: a mini USB connector for FPGA configuration, and JTAG sockets.

5.3 Backplane connector layout

The backplane connector is made to standard ATCA layout in zones 1 and 2. Zone 3 is populated with five MTP/MPO connectors that connect onto a RTM with hermaphroditic blind-mate shrouds (MTP-CPI).

5.4 Interfaces to external systems

L1Topo interfaces to external systems mainly via optical fibres. The physical layer is defined by the fibre-optical components used. On the real-time data path fibre-bundles with multiples of 12 multimode fibres are used. The external connections are made by MTP/MPO connectors. L1Topo is equipped with male connectors.

The calorimeter and muon trigger processors are connected via 48-way fibre assemblies, for the CTP outputs 12-way assemblies will be used. Opto-electrical translation on the real-time path is made with miniPOD 12-channel transceivers. Ideally the far end transceivers should be of same type as on L1Topo. Thus the optical power budget can be maximised. For short fibres and in absence of any optical splitting, other transceiver types are assumed to be compatible. However, optical power budget should be checked carefully.

Data rates and formats are defined by the FPGAs used for serialization and deserialization. For the L1Topo prototype 6.4 Gb/s or 10 Gb/s data rates will be supported. For the production module any rate up to 13 Gb/s will be supported by the processor FPGAs, though maximum data rate will depend on the exact device type being purchased in 2013/14. At current the miniPOD transceivers will limit the data rate to a maximum of 10 Gb/s. A possible road map to higher data rates is not known.

All real-time data streams are used with standard 8b/10b encoding. The data links are assumed to be active at all time. There are neither idle frames nor any packetizing of data. For reason of link stability and link recovery an option of transmitting zero value data words encoded into comma characters is being considered. This might also simplify initial link start-up.

All non-real-time external links are SFP links (additional miniPOD based connectivity might be provided as well). Data rates and encoding scheme need to be kept within the capabilities of the control FPGA (Kintex-7, up to 6.6 Gb/s). Since the use of L1Calo RODs is envisaged in an initial phase from 2013/14, the DAQ and Level-2 links need to be compatible to the legacy data formats (G-Link). Firmware has been devised at Stockholm to generate compliant signals in Xilinx MGTs. The optical control link is assumed to be run at 1.25 Gb/s line rate and will therefore be compatible to Ethernet (SGMII). Two spare optical inputs (up to 6.6Gb/s) will be available on the DAQ/Lvl-2 SFP devices. They will be routed such that the LHC bunch clock can be received that way. It should be noted that the wavelength of those devices is not compatible to the current TTC system and an external converter needs to be employed.

A limited amount of electrical I/O is available into the processor FPGAs. These data lines are reserved for the most latency critical paths. Dependent on the needs they might be configured as either inputs from the digital processors, or outputs to the CTP. The signals are routed via a mezzanine module, so as to allow for signal conditioning. The maximum data rate on the electrical path will depend on the signal conditioning scheme chosen, and the cable length. The FPGAs themselves would allow for more than 1 Gb/s per signal pair. The electrical port width is 24 signal pairs per processor FPGA. Connector mechanics are affecting the mezzanine module only and are not within the scope of this review.

Here a table of interfaces ?

6 Appendix

6.1 Checklist for detailed design

Detailed rules regarding signal integrity are to be followed so as to make sure the high desity/high speed module can be built successfully. In addition a few details on signal wiring for FPGA control pins are listed. This list might be expanded for a detailed design review.

The rules with respect to power supply are:

- Use low-noise step-down converters on the module, placed far from susceptible components.
- Use local POL linear regulators for MGT link supplies
- Observe power ramp and sequence requirements for FPGAs
- Run all supply voltages on power planes, facing a ground plane where possible, to provide sufficient distributed capacitance
- Provide at least one local decoupling capacitor for each active component
- For FPGAs, follow the manufacturer's guidelines on staged decoupling capacitors (low ESR) in a range of nF to mF
- Observe the capacitance limitations imposed by the voltage convertors
- Minimise the number of different V_{CCO} voltages per FPGA to avoid fragmentation of power planes
- avoid large numbers of vias perforating power and ground planes near critical components
- According to the device specifications the following supply voltages need to be applied to the FPGAs: Vccint=1.0+/-0.05V, Vccaux=1.8V
- On all FPGA supply voltages observe the device specific ramp up requirement of 0.2ms to 50ms.

The rules with respect to general I/O connectivity are:

- Tie Vccaux and most bank supplies to 1.8V. A given FPGA is supplied by only one 1.8 V plane.
- Use all processor FPGA banks for LVDS (1.8V) only
- Use HP banks on the control FPGA for LVDS connections to the processor FPGAs and mezzanine modules
- For the control FPGA only: wire a small number of banks for 3.3V single ended operation (HR banks)
- Neither reference voltages nor DCI termination are required on the processor FPGAs. Use respective dual-use pins for I/O purposes
- For the control FPGA HR banks allow for DCI termination on single ended lines

The rules with respect to single ended signalling are:

- Run FPGA configuration and FPGA JTAG clock lines on approximately 50 Ω point-to-point source terminated lines
- Observe the requirements on overshoot and undershoot limitation, in particular for System ACE and FPGA JTAG and configuration lines. Use slew rate limited or low current signals and/or series termination

The rules with respect to differential signalling are:

- For discrete components, use internally sink-terminated devices throughout. Any non-terminated high-speed devices need to be documented in a separate list.
- Use LVDS on all general-purpose FPGA-FPGA links
- Use LVDS on all GCK clock lines
- Use DC coupling on all LVDS lines
- Design all LVDS interconnect for 1Gb/s signalling rate
- Use CML signalling on all MGT lines, for both data and clocks
- Design all MGT data links for 10Gb/s signalling rate
- Generally use AC coupling on all MGT differential inputs and outputs, for both data and clocks
  - SFP devices might be internally decoupled, microPOD transmitters might have a sufficient common mode range to allow for direct connection
- Use CML on all common clock trees; rather than using AC coupling, observe the signalling voltage and input compatibility rules as outlined by the device manufacturers

- Use AC coupling when crossing PECL/CML domains
- Use AC coupling or suitable receivers when crossing 2.5V/3.3V domains, except on LVDS
- Place coupling capacitors close to source
- Use bias networks on AC coupled inputs where required
- Route all differential signals on properly terminated, 100 Ω controlled-impedance lines
- Have all micro strip lines face a ground plane
- Have all strip lines face two ground planes or one ground plane and one non-segmented power plane
- avoid sharply bending signal tracks
- minimise cross talk by running buses as widely spread as possible
- Avoid in-pair skew, in particular for MGT links and clocks
- Avoid impedance discontinuities and stubs, in particular on MGT links and clocks

The rules with respect to FPGA pre-configuration and configuration control pins are: --- check !!!!

- Allow mode lines M0, M2 to be jumpered to either Vcc or GND. Pre-wire to Vcc
- Connect M1 to the CPLD (GND=JTAG mode, Vcc=slave serial)
- Connect PROGRAM, INIT and DONE lines to the CPLD
- Pullup DONE 330Ω, INIT 4k7 PROGRAM 4k7
- Connect Vccbatt to GND
- Wire DIN, DOUT and CCLK (series terminated) configuration lines to the CPLD
- Allow for wiring RDWR and CSI to either Vcco or GND

The rules with respect to system monitor pins are: --- check !!!!

- Do not use temperature sense lines DXN,DXP and short them to GND
- Decouple analog power and GND according to UG370 with ferrite beads and wire the system monitor for internal reference (both Vref pins to analog GND)
- Do not use analog sense lines Vn and Vp and connect to analog GND

6.2 Glossary

1000BASE−SX	Ethernet optical (multimode) physical layer
8b/10b	Industry standard data encoding scheme for purpose of DC balance and run length limitation (bit change enforcement)
ATCA	Advanced TCA, Advanced Telecommunications Computing Architecture
Avago	Manufacturer of 12-channel opto-electrical transceivers. The Avago transceivers used on L1Topo are of miniPOD type
Base interface	ATCA compliant backplanes provide pre-defined redundant IP connectivity via Ethernet 10/100/1000 from each slot to two modules in the crate (dual star)
BLT	Backplane And Link Tester module, fits in CMM slot of the L1Calo processor backplane
CAN	Controller Area Network, a differential serial bus (automotive)
CML	Current Mode Logic, a high-speed differential signalling standard
CMX	Future replacement of the L1Calo Common Merger Module
CTP	The Central Trigger Processor of ATLAS
DAQ	Data Acquisition (link). Physical layer G-link compatible (L1Calo standard)
FMC	FPGA Mezzanine Card, as defined in VITA-57. Connector types Samtec SEAF/SEAM or compatible
G-link	Pre-historic HP/Agilent Phy chip. ~ 1Gb/s, proprietary link encoding scheme
GOLD	Generic Opto Link Demonstrator
IBERT	Xilinx automated bit error rate test tool for MGTs
IPMB	Intelligent Platform Management Bus (redundant, IPMB-A and IPMB-B), located in ATCA zone 1
LVDS	Low-Voltage Differential Signaling standard

MGT	Multi-Gigabit Transceiver
miniPOD	High density 12-channel opto-electric transceiver
MPO/MTP	Industry standard optical connector for fibre bundles, here 12-72 fibres
Phy	A device implementing the physical level (electrical representation) of a network protocol
Quad	The Virtex-6 Serialiser/Deserialiser circuits are arranged in tiles of four MGT links each
ROI	Region of Interest, as signalled to 2^{nd} level trigger. ROI link to Level-2 has G-link data format (L1Calo standard)
RTDP	Real-time data path, i.e. the data path going to the CTP. Latency critical path.
RTM	Rear Transition Module (note: ATCA RTMs mate with the front modules directly in Zone 3, not via the backplane)
SGMII	Serial Gigabit Media Independent Interface (for Ethernet Phy), 1.25Gb/s
SFP	Small Form factor Pluggable, electromechanical standard for opto transceiver
TTCDec	L1Calo specific mezzanine module for connection to the ATLAS Timing, Trigger and Control system, based on the TTCrx chip
VME(bus)	Versa Module Eurocard (bus). L1Topo is optionally connected to a VME module for purpose of module control, via a bidirectional serial link initially
Zone	ATCA connector zones 1 (mainly power), 2 (backplane data links), 3 (RTM connections)

6.3 Change log

2012
May 23 – initial version