(Not just) Backplane transmission options

So far

- Preliminary design for phase 1 had been suggested
  - Extract topological information from digital processors (firmware upgrade)
  - Replace CMMs by serialiser w. fibre output
    - Up to 160 Mb/s backplane data rate
    - 3 Gb/s optical out
  - Aggregate bandwidth at merger slot 64 Gb/s
  - Total bandwidth of JEP and CP ~700 Gb/s
  - Two-stage top level calorimeter processor (quadrant)

? Hard facts on backplane bandwidth limits

? Detailed algorithms

? Simulation

? Muons

Recently…

- Some backplane results:
  - 160 Mb/s possible
  - … even with CMM (Richard, CPM only)
  - Higher rates possible only with sink termination
- Some simulation results

- (non-)schedule seems to be sliding
- Technology moves on

- BTW: are we really sure the current trigger scheme is good enough for design luminosity (phase 0) ?

→ Difficult to judge as long as there are no collisions at all !

What can we do by firmware only ? – backplane

- We can be rather sure that 80 Mb/s backplane operation suits current CMMs
- 120 Mb/s would probably require clean external clock, due to Virtex-E DLL limitations :
  - Spare differential inputs in the back of a CMM
  - SFP o/e transceiver cheap and low jitter
- Signal integrity seems ok even for 160 Mb/s

At an elevated data rate the data windows shrink due to known jitter and walk from TTCdec (TTCrx).

→ Need a per-slot phase optimization at source

- JEP: clkdes1/2 are in use. Could be made available (major f/w mod on input processor), s/w
- CP:

And on to the CTP

- Probably quite some spare bandwidth on the CMM outputs
- LVDS signalling rate depends on cable length and cable properties, double rate should be ok.
- Conversion to optical rather simple if DC balanced (firmware, SNAP12/MPO : $)
- Need detailed assessment of CMM capabilities
- Nothing known about CTP inputs (?)

Algorithms : just an example...

- Most algorithms of which we expect performance gains require massive increase in data rate throughout the system → not for phase 0

- Leading jets angle cuts require two most energetic ROIs only:
  - Moderate bandwidth requirement
  - Sort algorithm required at all stages
    - JEM: 2 of 8
    - Crate merger : 2 of 32
    - System merger: 2 of 4
  - Calculation of angle and thresholding (LUT)

Phase 1

- Backplane
  - CP rates probably limited to 160 Mb/s
  - JEP possibly higher if required (termination)
- Merger links (optical)
  - Xilinx Virtex-5/6 stuck at 6.5 Gb/s (2010/11)
  - Aggregate bandwidth ~200 Gb/s per chip
  - No information on Virtex-6 HXT (10 Gb/s)
- Merger could be ATCA or similar form factor
- Optical components for high density processors available
  - High density blind mate opto backplane connectors
  - Splitters
  - MPO fanout
  - (Optical backplanes too exotic)

Plans

- Improve performance of current system (firmware)
- Devise and simulate algorithms for phase 1
- Make optimum use of existent demonstrators
  - Stockholm link tester generate 3.2 Gb/s optical
  - BLT serialise backplane data to 6.5 Gb/s optical
- Build a demonstrator global merger with 6.5 Gb/s links
- Design for unrestricted choice of algorithms:
  aim to feed maximum of data into single point
  → maximum link density, high performance FPGAs
- Discuss timeline → decide on
  - Form factor
  - Amount of processing power required
  - Signal replication scheme
    - Extensive use of optical technology
    - Replication at source
    - Electrical multi-Gb/s link replication at sink

To Do – Who – What ?

- Mainz interested in
  - Firmware-based improvements on current JEMs
  - 6.5 Gb/s FPGA based link technology
  - Optical : passive replication – blind mate connector
  - Ready to work on global merger demonstrator
  - Not yet given up on possible JEM rebuild
- ?