Hardware status GOLD

Generic Opto Link Demonstrator

Pre-historic & GOLD

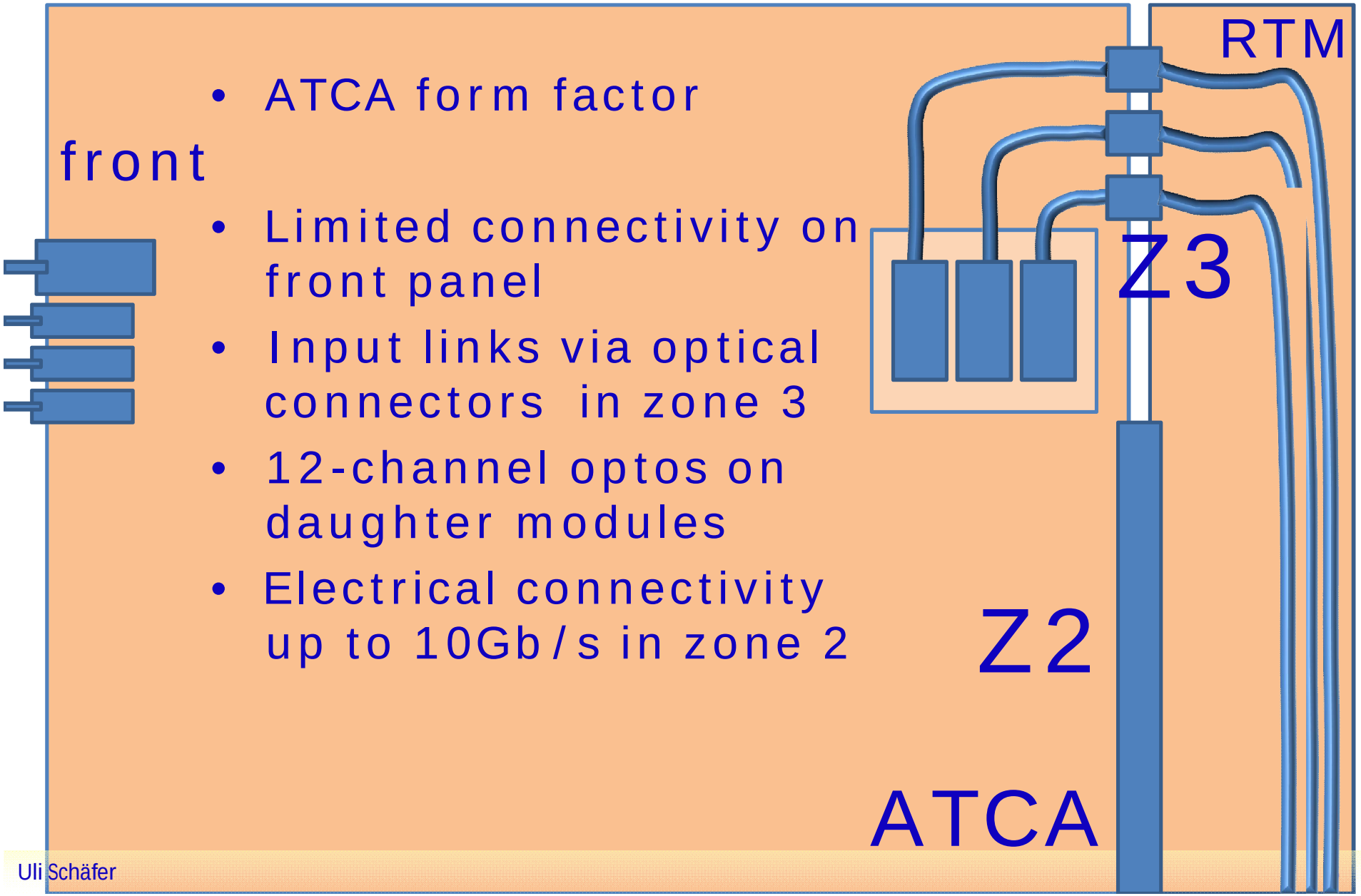
Backplane and link tester BLT built and tested in 2009

- 9U*40cm, fitting CMM slot in JEP/CP crate
- 1 Virtex-5
- 400 s/e backplane links
- Multi-Gigabit links
- 1 standard SFP optical link device
- 1 pair of SNAP12 optical devices
- Minor h/w issues
- Successfully operated on 160+ Mb/s backplane signals
- Successfully operated on Gigabit optical links (SFP)

To further explore optical links and new technologies → GOLD

- AdvancedTCA (ATCA) form factor
- Many Virtex-6
- Higher link count
- Higher link speed
- Optical backplane connectors

GOLD concept



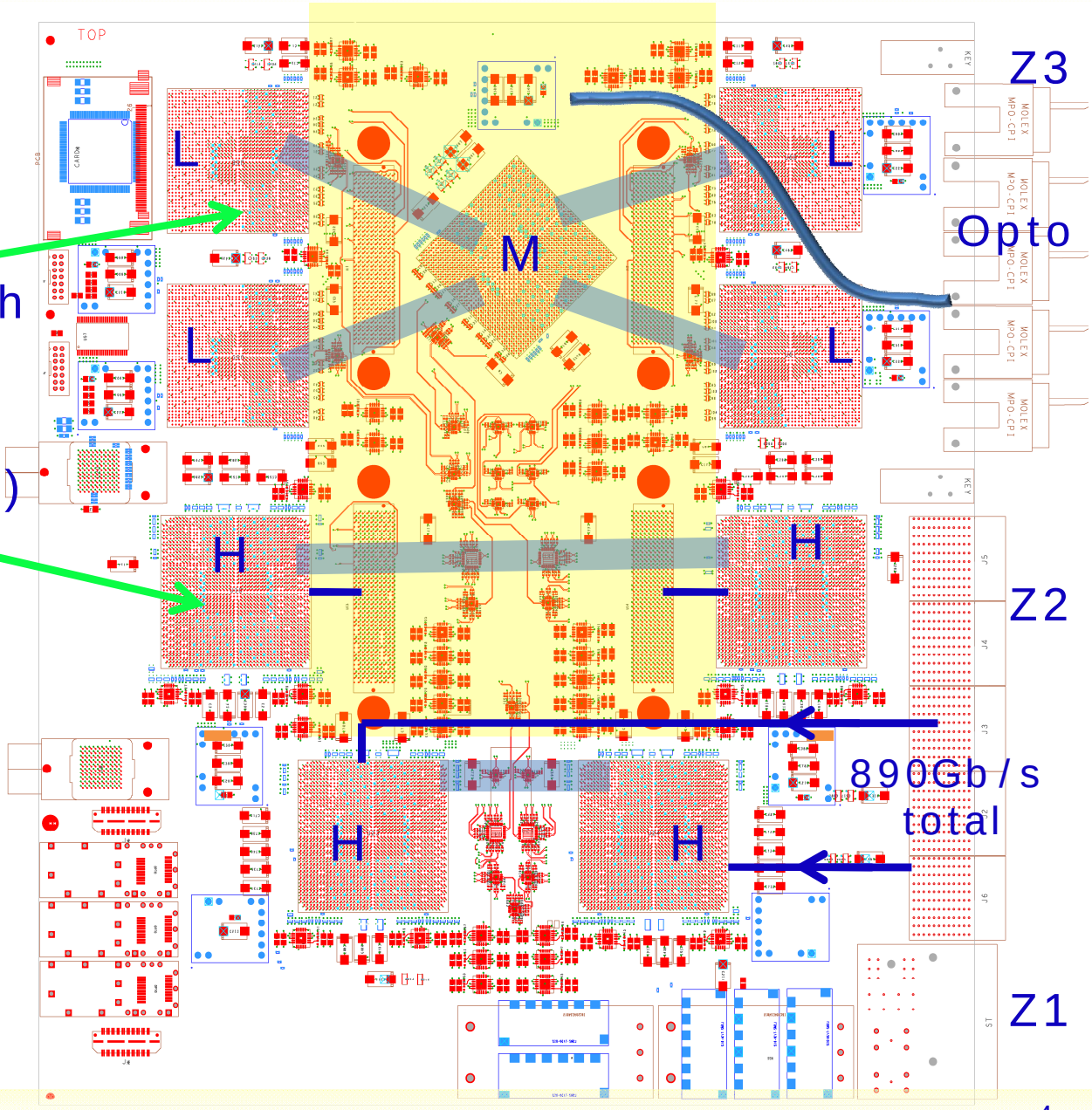
GOLD floor plan

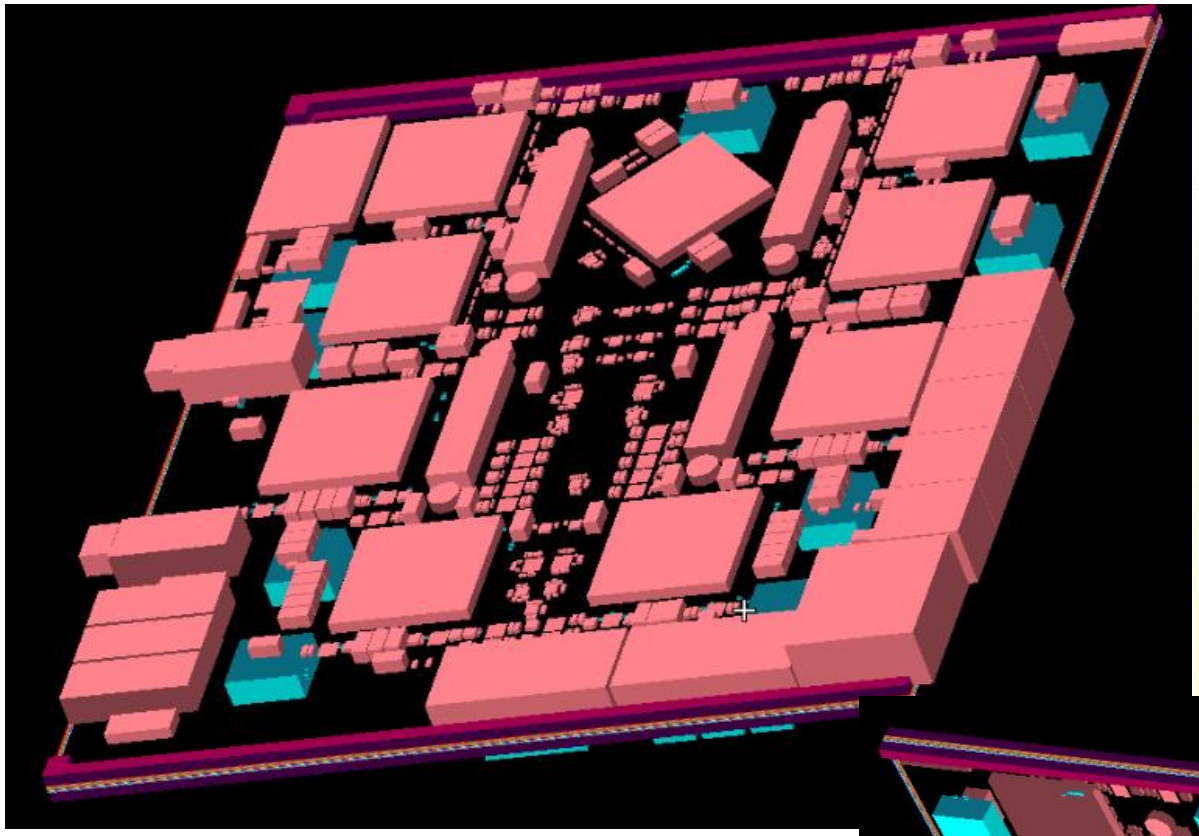
5 * XC6VLX
(Processor L, merger M) up to 36 links each

Two pairs of XC6VHX (H)
72 links each

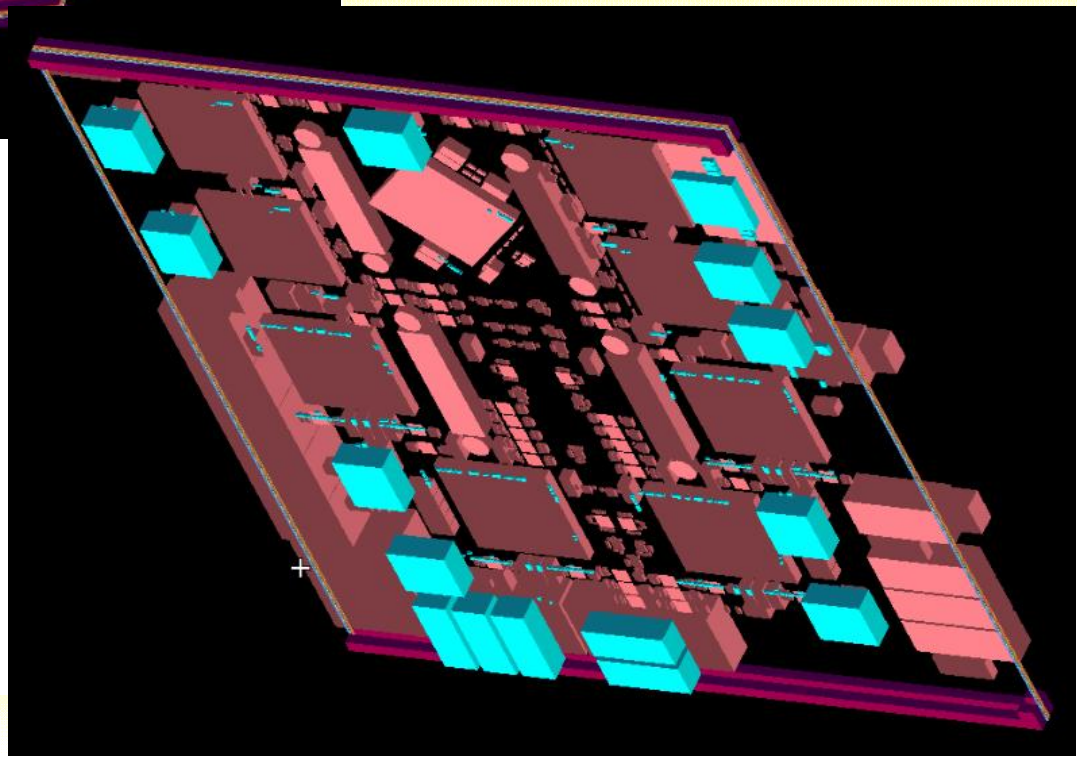
5+ 12-channel optos on daughter

144 multigigabit links in zone 2 (equiv. 22300 bit / BC)





real
GOLD



GOLD – forever ?

- Module originally planned for ca. 8 x 6VLX550T with opto backplane connection only
- Converted to a mixed scheme 6VLXT / 6VHXT (6.5/10Gbps)
- Added electrical backplane connectivity in zone 2
- Learned about power consumption of Virtex 6
  → re-design of on-module power distribution
- Currently designing for 480W per module (primary supply -48/12V converter)
- Difficult to find power converters with small footprint, high current and a lead time below 40 weeks
- Module densely packed, power converters on bottom
- Thick module, more than 1 ATCA slot
- Xilinx documentation for HXT devices far from complete

However, things are now starting to look promising

GOLD status

- Schematics and layout under way
- Components ordered in February
  - AVAGO optos (2*T, 2*R) : arrived
  - SNAP12 : ???
  - Xilinx 6VLXT: arrived
  - Xilinx HXT ???

... While Bruno's heroic battle against missing documentation and unavailable components continues ....

... some firmware activities:

Currently working on extension of VME bus from 9U processor crates, via BLT module, optically into GOLD (see next presentation)