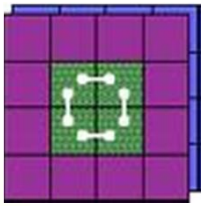


L1Calo – towards phase II

Mainz upgraders :
B.Bauss, V.Büscher, R.Degele, A.Ebling, W.Ji, C.Meyer, S.Moritz,
U.Schäfer, C.Schröder, E.Simioni, S.Tapprogge

- Current L1Calo
- Some technicalities : Latency and data duplication
- Strawman for phase 2

Prologue: the L1Calo trigger rates...

Simulations suggest horrible increase of calorimeter trigger rates with rising luminosity for current trigger scheme. What can we actually do about that ?

EM Triggers

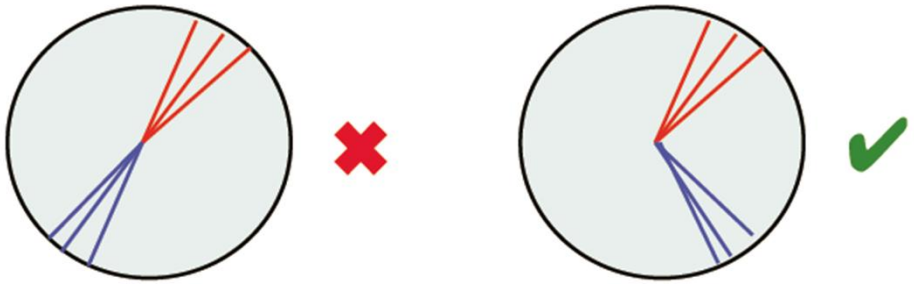
- longitudinal sampling from LAr may help
- higher transverse granularity information may help
- needs study – we don't yet know what is most useful
- will impact L1Calo requirements for LAr ROD

Jets

- not limited by trigger tower granularity – so no help here
- but would like to separate cleanly from EM triggers (not currently the case)

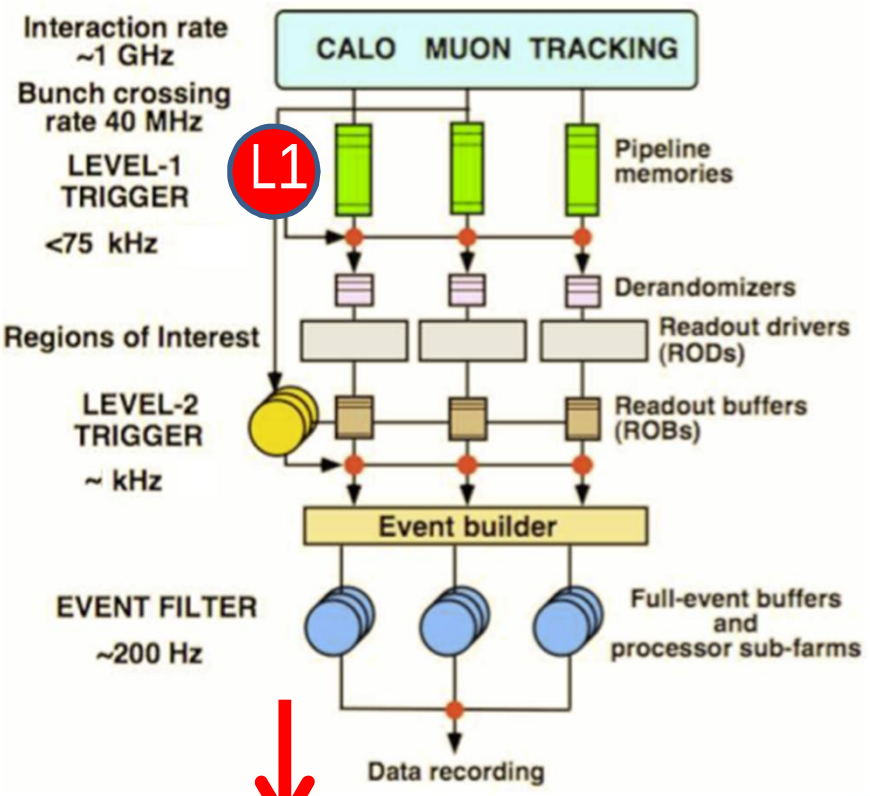
Topology

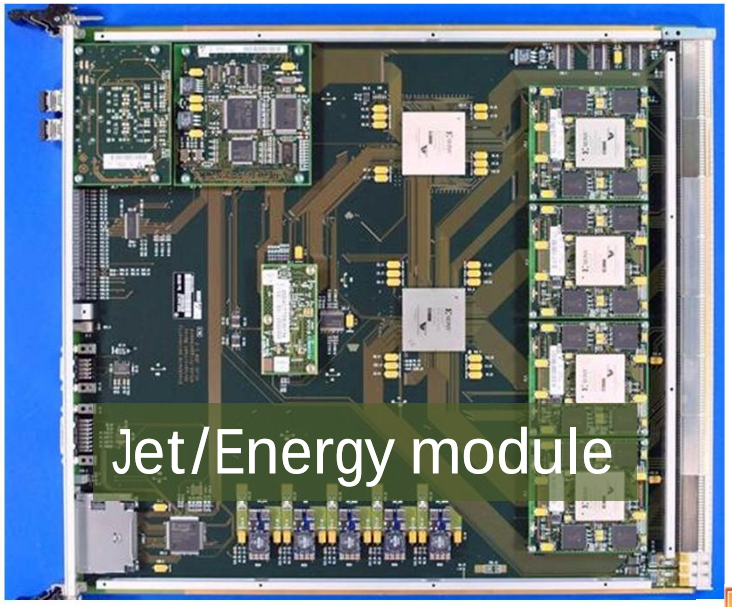
- correlate RoIs to pick out physics signatures
- e.g.

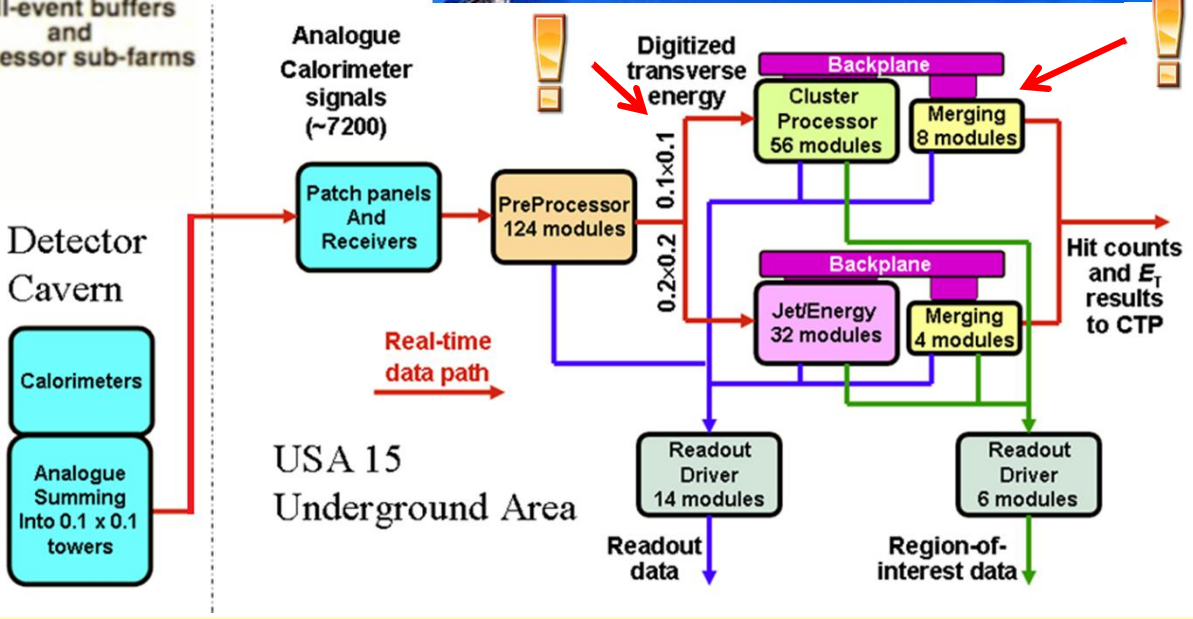


ATLAS Upgrade Meeting, Oxford, 29/3/2011 Mark Thomson

ATLAS Trigger / current L1Calo

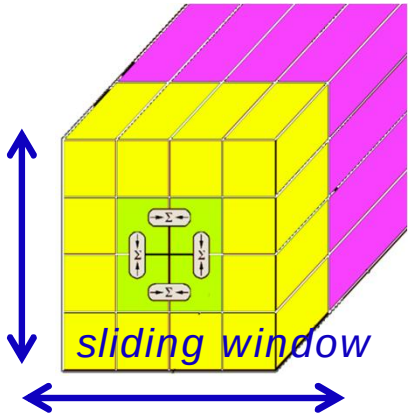






Current and future L1Calo

- Analog signals transmitted off the detector (0.1×0.1) η,φ
- Pre-Processor: ADCs, digital filters, baseline/gain/linearity, bunch crossing identification
- Digital processors:
  - Sliding windows for jet and em cluster extraction, data consolidation by thresholding and counting objects
  - Global results determined by summation on daisy-chained merger modules (CMMs)
  - Final results of object count and total and missing E_T sent to Central Trigger Processor



- Phase 0/1 (i.e. from 2013/14 !):
  - Improve pre-processing (new MCMs)
  - Increase digital processor backplane bandwidth to extract topology, replace mergers (CMM++)
  - Add topological processor stage, include muon data
- Phase 2 : complete replacement of L1Calo

Latency, data duplication, data paths ...

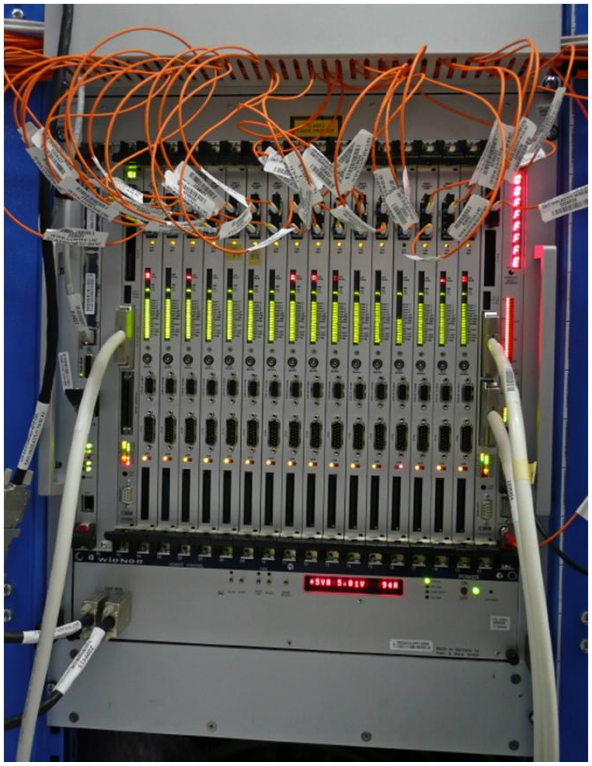
Total latency currently limited to c. 2.5 µsec

- Cables
- Serialisation / de-serialisation on module/chip boundaries
- Processing

Sliding windows algorithms require duplication of data across processor module and crate boundaries

- ➢ All L1Calo real-time data transmitted electrically : analogue, 480 Mb/s serial, 40/80/160Mbps parallel
- ➢ Data duplication by mixture of forward duplication (zero latency) and cross-module communication (1.x BX +)

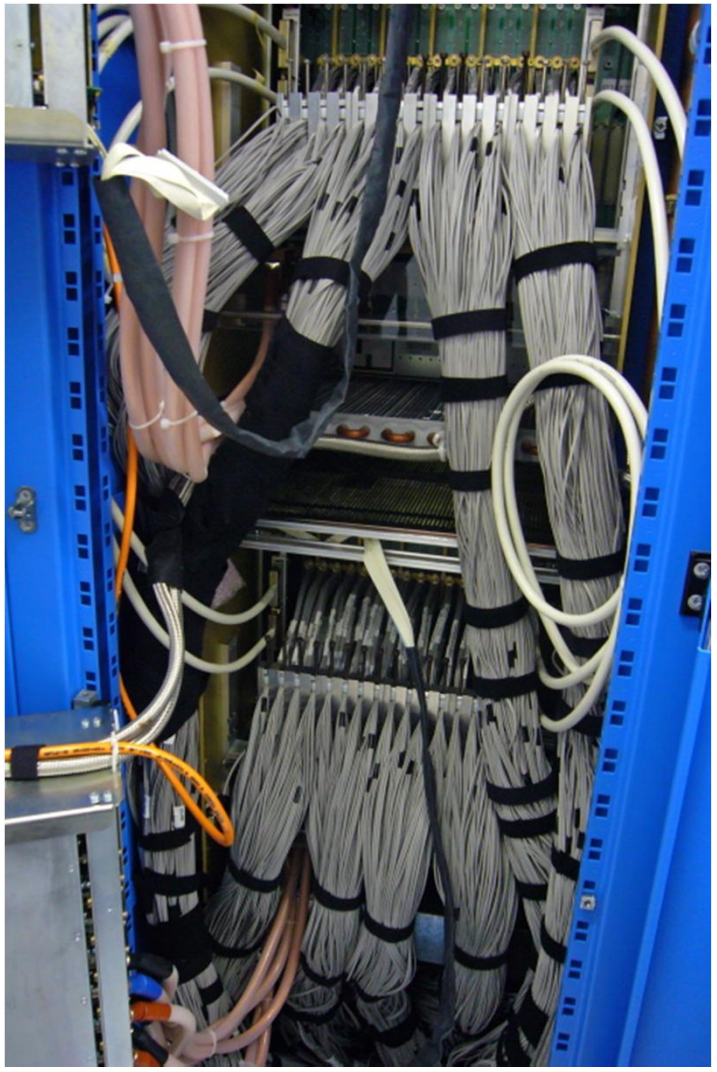
The horror lurks behind...



Jet/Energy processor

Pre-processor

Jet/En. processor



Upgrade : Go optical

Phase 0/1/2 upgrades will be based on optical interconnect

- Latency issues will not disappear by miracle
- Accept inherently higher latency per high speed link

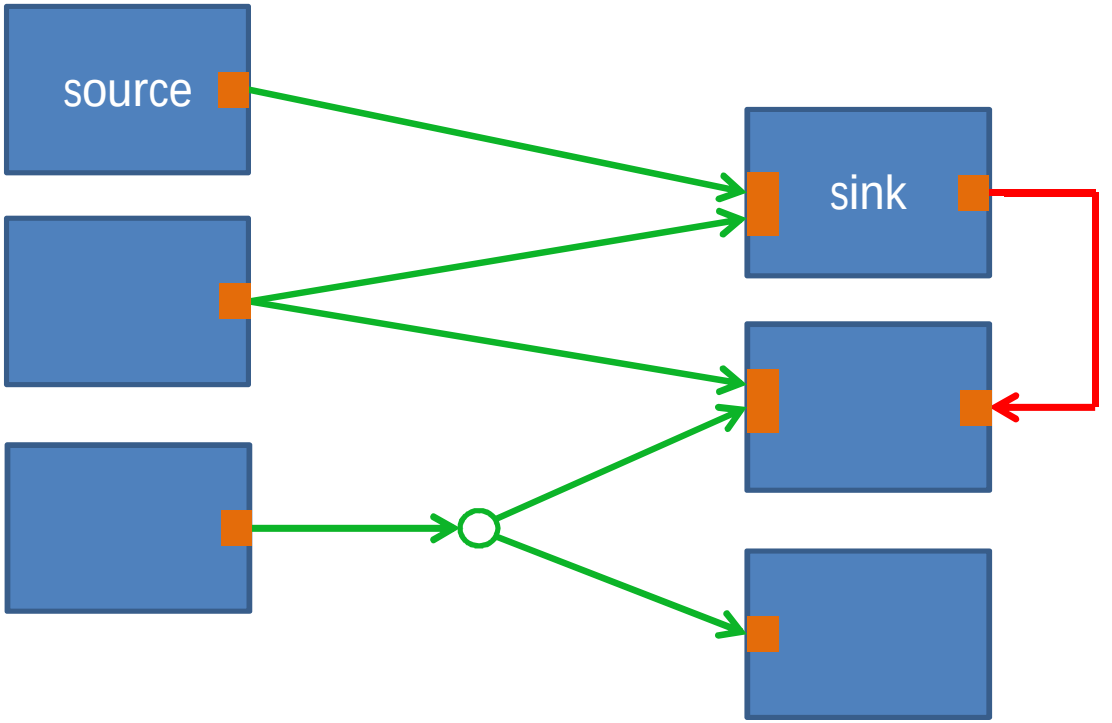
→ Increase system density by use of FPGA-internal Multi-Gigabit Transceivers (MGTs)

→ Partition the system such that excessive de-serialization/re-serialization is avoided

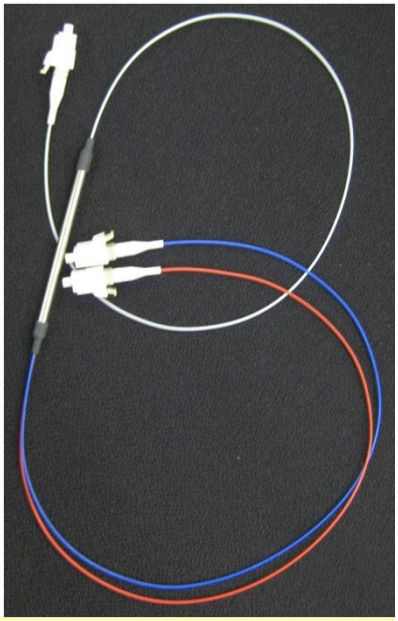
→ Optimize the data replication scheme

→ Explore options for latency reduction on the FPGA

Data replication



Do not share any data between modules of same subsystem to avoid additional SerDes latency



Forward data replication only:

- Duplication at source
  - Mirror a link
  - Assemble a different stream optimised for the replication
- Optical splitter (fibre coupler)

Phase 2

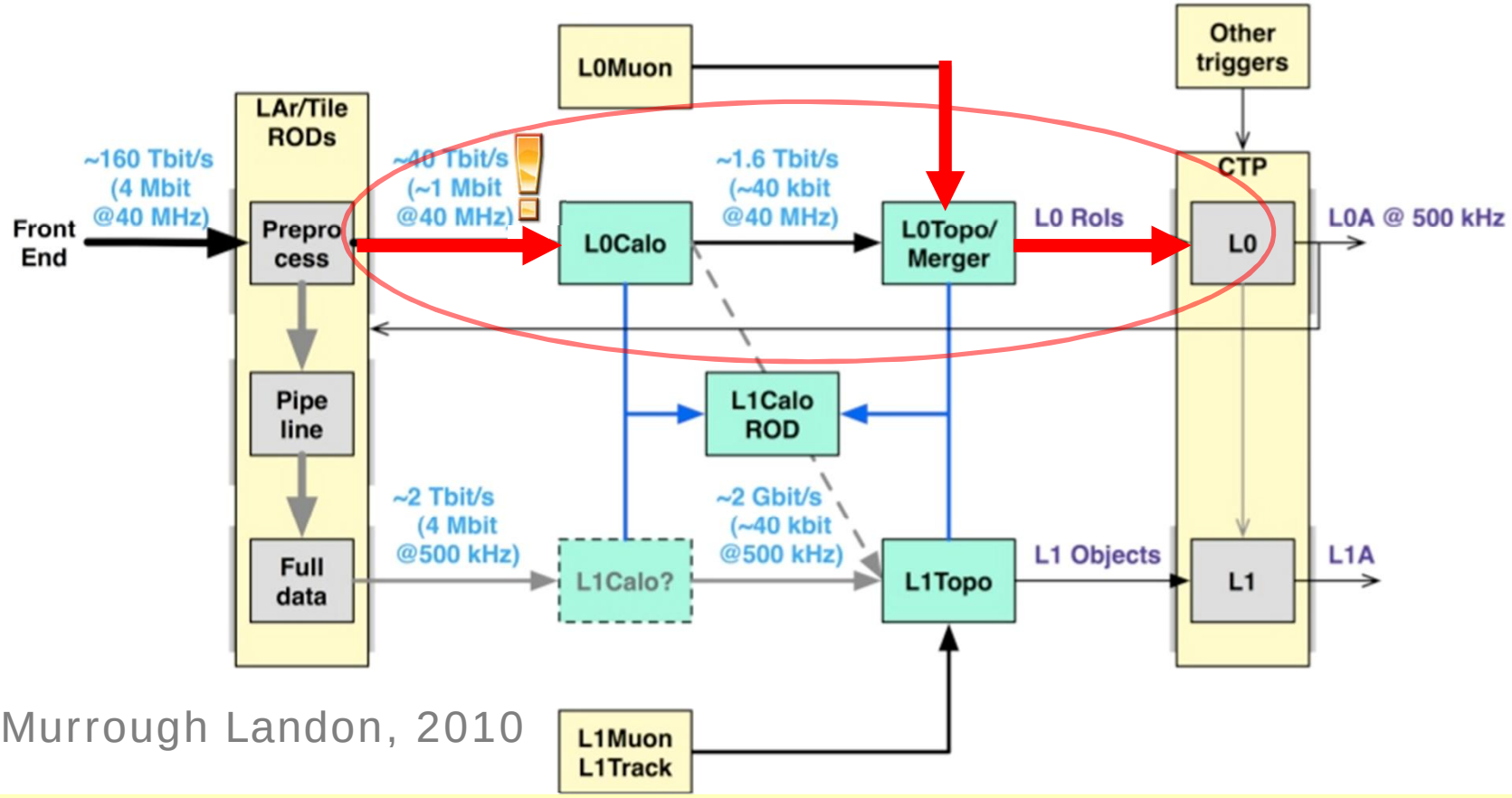
Latency impact on Phase 2 design…

- 3.2 μs latency insufficient for track trigger
- Probably needs seeding
- Current favoured solution is a two stage system L0 and L1
- Level 0
  - low latency, synchronous (“real-time”) trigger system
  - input to L0Calo goes digital (LAr and Tile)
  - includes Topo processing + muons
  - send RoIs to region-based track trigger
  - L0 accept at ~500 kHz (?)
- Level 1
  - includes calorimeter, muon and track trigger
  - might run asynchronously
  - higher latency (to be defined)
  - possibility of HLT-like algorithms

eventually ... Phase 2 !

« Once the calorimeter readout is replaced ... in 20xx ... »

- High granularity trigger data provided on optical links
- New sliding windows processor with optical interfaces only
- Synchronous low-latency L0 plus asynchronous L1



Murrough Landon, 2010

...as of last week (R.Middleton)

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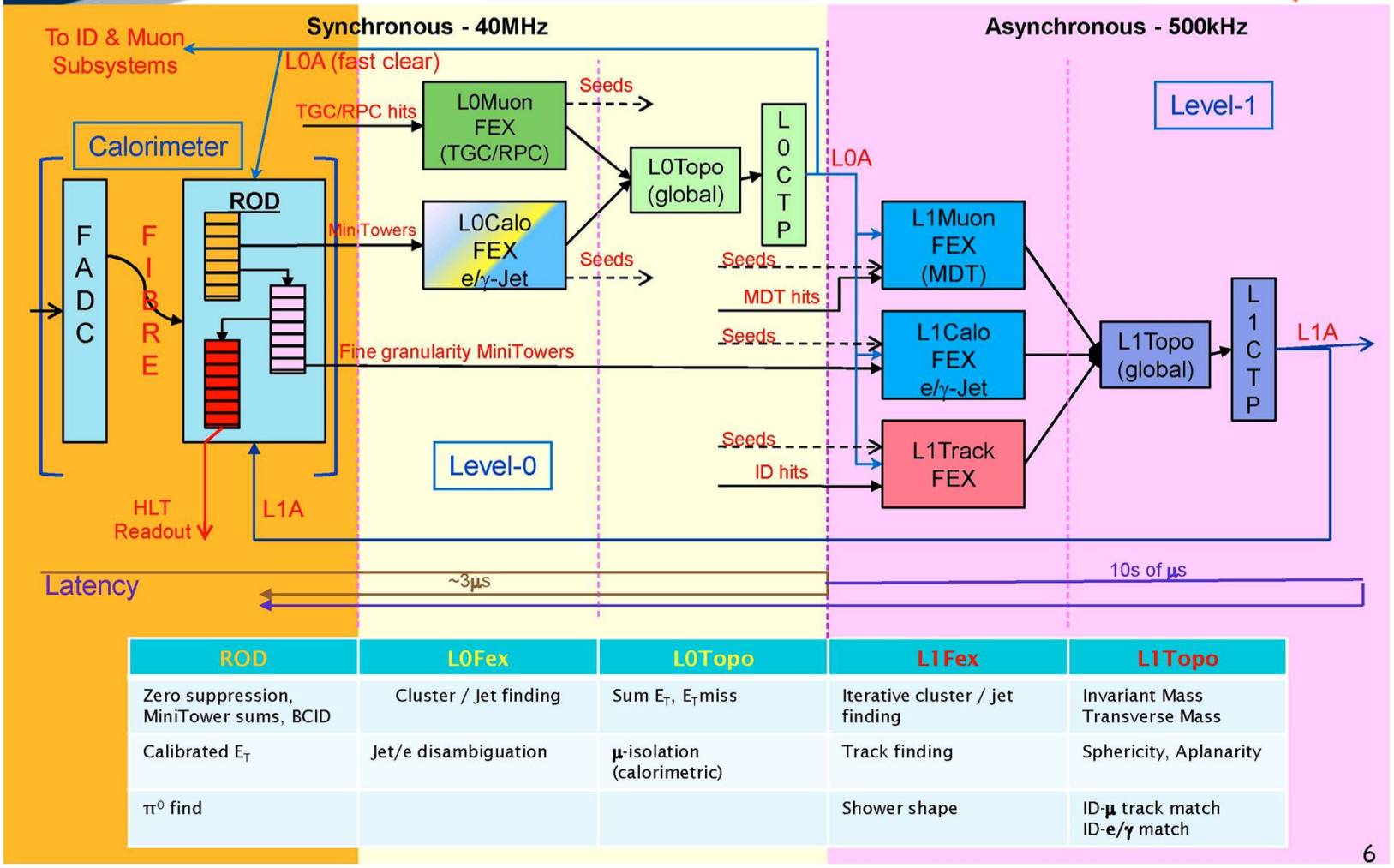
Strawman Architecture



ROD	L0Fex	L0Topo	L1Fex	L1Topo
Zero suppression, MiniTower sums, BCID	Cluster / Jet finding	Sum E_T, $E_T$miss	Iterative cluster / jet finding	Invariant Mass Transverse Mass
Calibrated E_T	Jet/e disambiguation	μ-isolation (calorimetric)	Track finding	Sphericity, Aplanarity
π^0 find			Shower shape	ID-μ track match ID-e/γ match

6

Cont'd...

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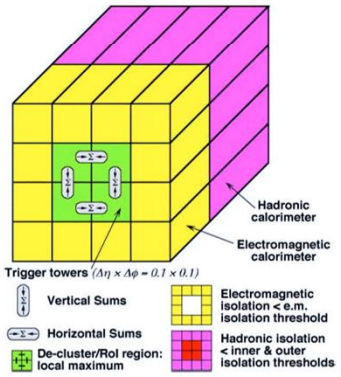
Components

- ROD
  - L0CaloFex -> form mini-towers, depth samples, BCID, etc
  - L1CaloFex -> fine granularity information
- L0CaloFex (feature extraction)
  - use mini-towers & depth information
  - sliding window algorithms, EM, Tau, Jet, Et partial sums
- L0Topo
  - inputs = L0Calo+L0Muon
  - compute topological triggers from features
- L0 CTP --> L0A (500kHz)
  - apply L0 menu, prescales, deadtime, etc.
- L1CaloFex
  - asynchronous (?) – 500kHz
  - refine using "full" calorimeter data
- L1Topo
  - compute topological triggers from REFINED features
  - inputs = L1Calo+L1Track+L1Muon
- L1 CTP --> L1A (100kHz)
  - apply L1 menu, prescales, deadtime, etc.



From 2013/4 ?

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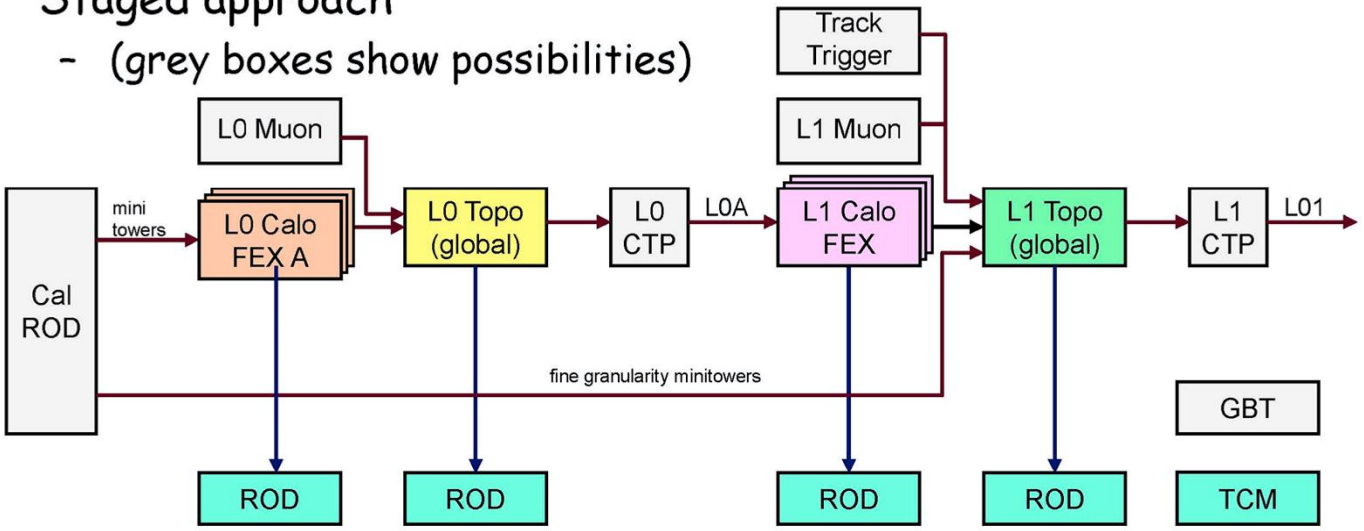
Slice Demonstrator

- Slice principle agreed at L1Calo meeting last week
- Discussions with calorimeter groups on
  - testbeam studies
  - small, zero perturbation tests in ATLAS
- Timeline ?
- Staged approach
  - (grey boxes show possibilities)



L1 Trigger in Phase II 14

- Some (almost) final words

https://indico.cern.ch/getFile.py/access?subContId=3&contribId=2&resId=1&materialId=slides&confId=133899

Some current upgrade activities in Mainz

- Simulations of topological algorithms at high luminosities ($10^{34}\,cm^{-2}s^{-1}$), high pile-up
- Simulation and implementation of the algorithms in VHDL
- Improvements on VHDL code for current processors
- Design of demonstrator modules for phases 0/1 and 2
  → Generic Opto Link Demonstrator
  - Topological processor (0/1/2)
  - Phase-2 Level-0 sliding windows processor
- Latency optimization
  - Data replication schemes
  - FPGA on-chip MGT operation modes and fabric interfaces