Level-1 Topology Processor for Phase 0/1

- Hardware Studies and Plans -

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Topology Processor

Simulations suggest a need for topological trigger criteria, so as to keep Level-1 trigger effective at high luminosities.

Example algorithms:

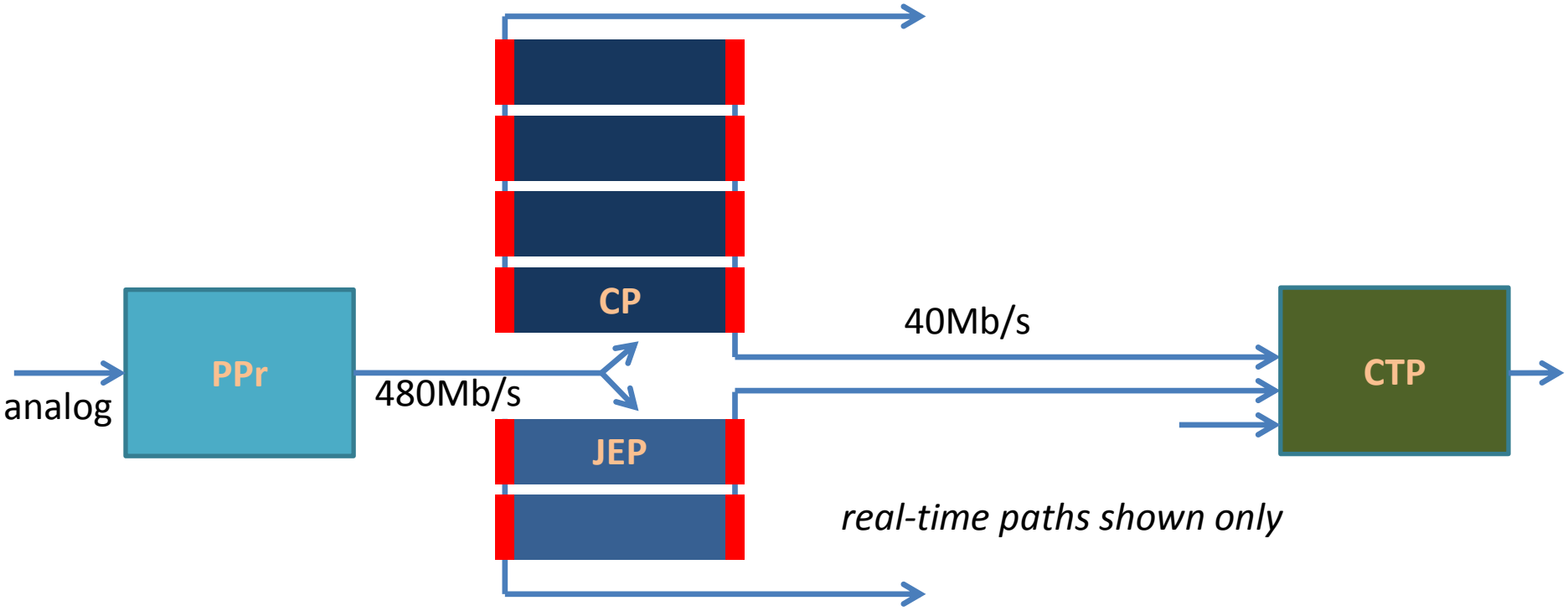
- Angular correlations (jets, direction of missing energy)
- Muon isolation
- …

Hardware implementation

→ Need to feed a maximum of data into a single point (module, FPGA)

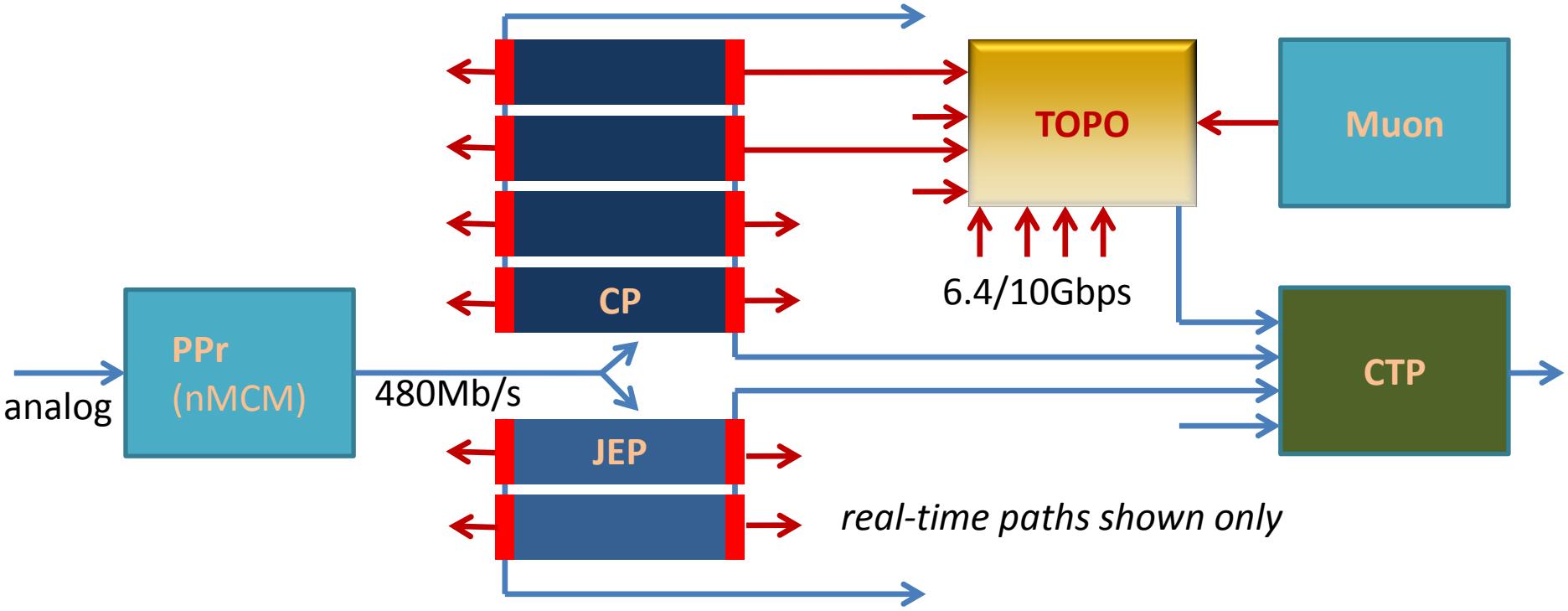
- Input from L1Calo and Muons
  - ~ 1 Tb/s aggregate bandwidth
  - Do not partition into multiple modules for reason of **LA***CY 💣☠ !

Current L1Calo Scheme



- Mixed Signal Pre-Processor
- FPGA based digital "sliding window" processors (e/m cluster, jet/energy)
- Object count and global quantities via chained mergers **CMM** into CTP
- Object positions to Level-2 and DAQ only

Phase 0/1 Scheme



- New **CMX** (CMM++) module with two interconnect options
  - Chained (legacy and opto links)
  - Star topology with all opto links into **topology processor**
- Muon information included on topo processor

… Topology Processor

- Input from L1Calo and Muons
  - ~ 1 Tb/s aggregate bandwidth
  - Fibre optical inputs @ 6.4/10 Gbps per fibre
- Output to CTP
  - electrical (LVDS)
  - fibre optical ~ 1Gb/s +
- Interfaces to TTC/GBT/…, Level-2, DAQ, control, DCS,…
- Small number of modules (~1)
- Probably dedicated crate, near CTP

→ Have started development programme

- 2010 : 6.4Gb/s data source **BLT** in CP/JEP crates to live in CMM slots → CMX ✓
- 2011 : Topo processor demonstrator GOLD !

The demonstrator : GOLD

- Functional demonstrator for phase-0 topology processor
- Technology demonstrator for technologies to be used throughout L1Calo upgrade programme, studies on fibre optical connectivity schemes

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- ATCA form factor
- Modular concept
  - Mezzanines
  - FMC connectors
- Optical backplane connectors rather than front panel I/O
- Opto/electrical conversion on input mezzanine
- Electrical connectivity up to 10Gb/s in ATCA zone 2
- Phase-0 topo-specific connectivity
  - Provide all interfaces

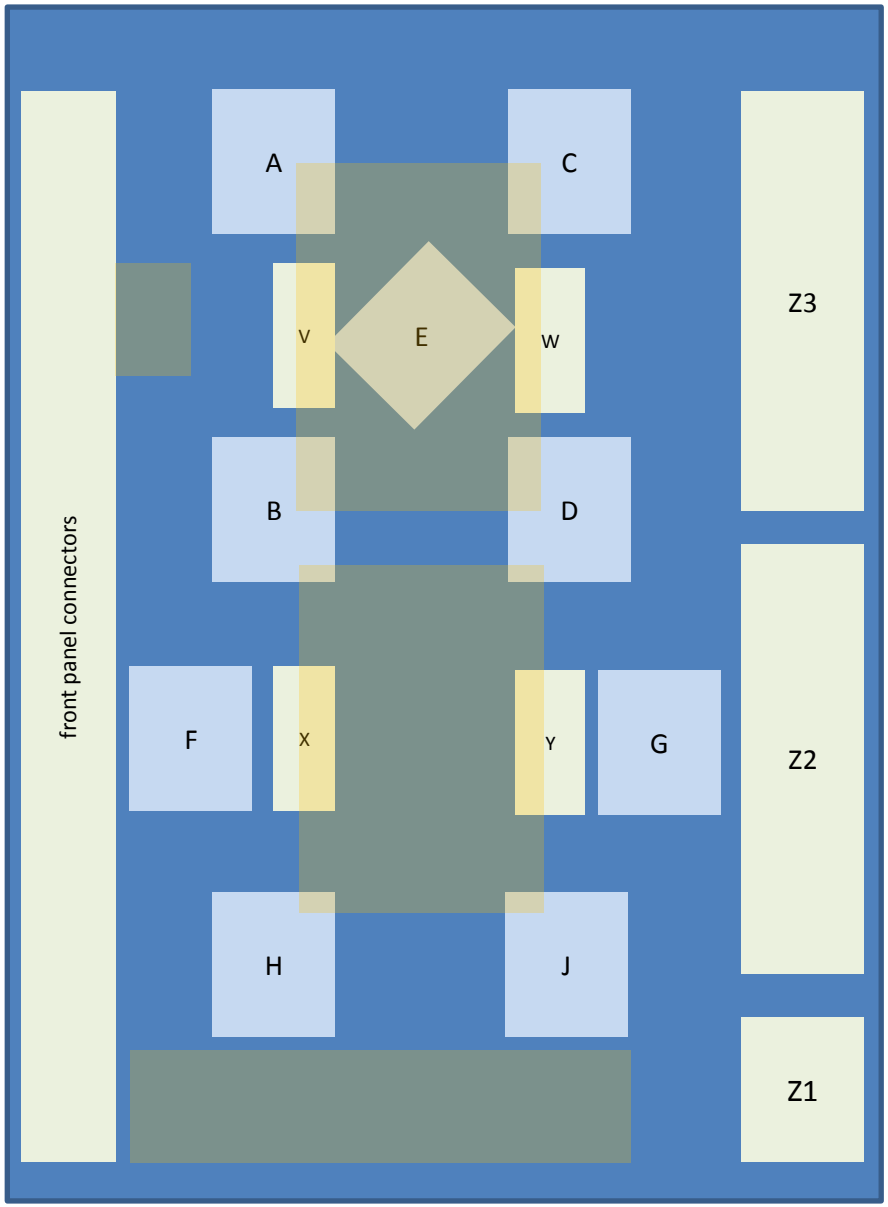
GOLD floor plan

A-J FPGAs

Mezzanines

V – Y : FMC connectors

AdvancedTCA
322x280 mm



Z3: opto connectors

Z2: electrical connectors

GOLD - some details

Main board, ATCA sized, 22 PCB layers

- FPGAs (Virtex-6 LXT, HXT)
- Connectors, sockets for e/o converters
- FPGA configurator and local clocks (DAQ/ROI, Ethernet,…)
- Main power distribution network (central and POL regulators)

Input mezzanine module, allow for choice of input devices and input signal routing

- 12 layers, moderate real estate
- Sockets for o/e converters, 10Gb/s fanout

Clock mezzanine module

- Recover and condition incoming (LHC bunch) clocks
- Some limited clock multiplexing and fan-out
- Provide additional space for auxiliary components and front panel connectivity

GOLD floor plan

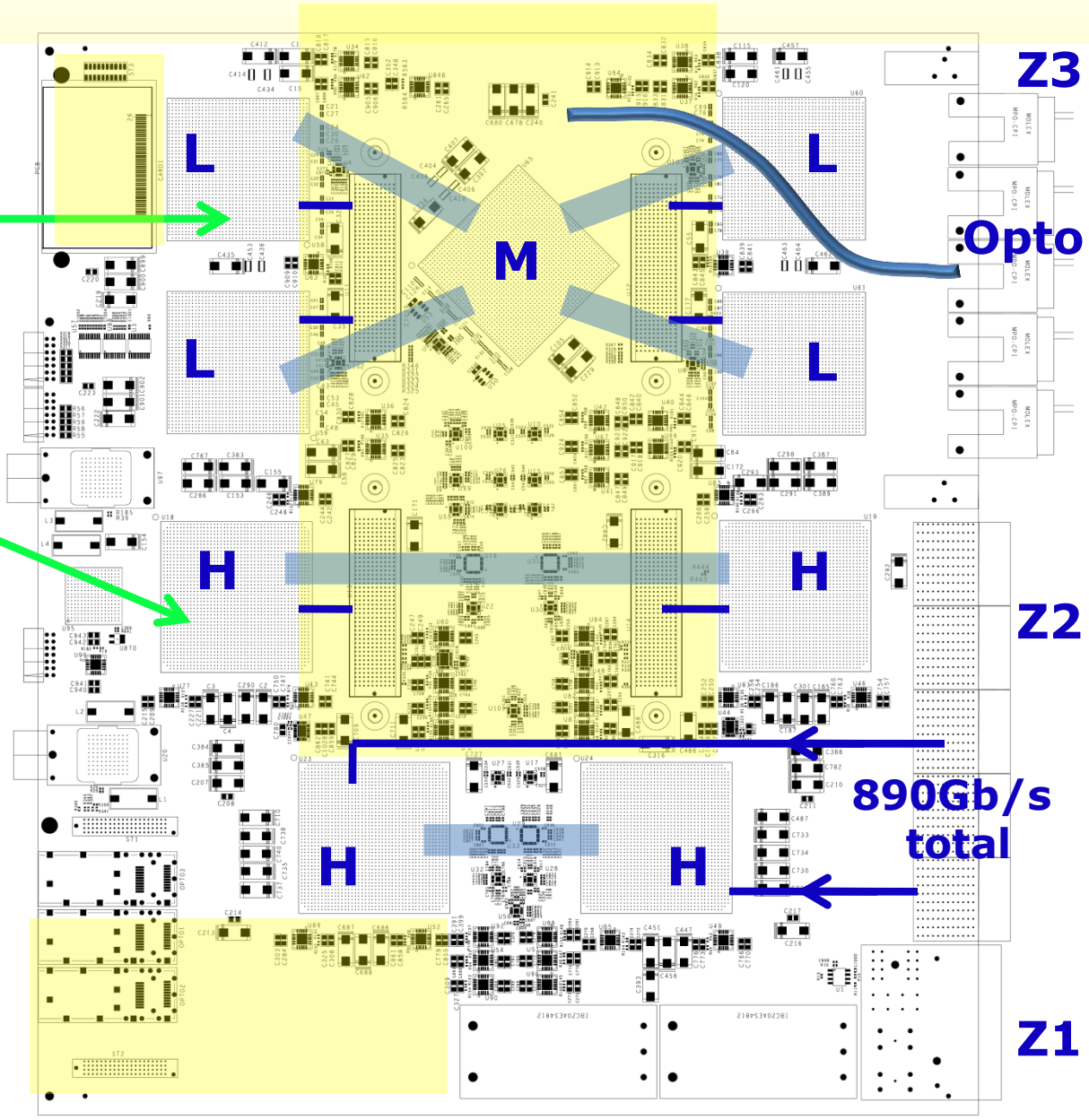
5 * XC6VLX
(Processor **L**, main processor **M**) up to 36 links each

Two pairs of XC6VHX (**H**)
72 links each

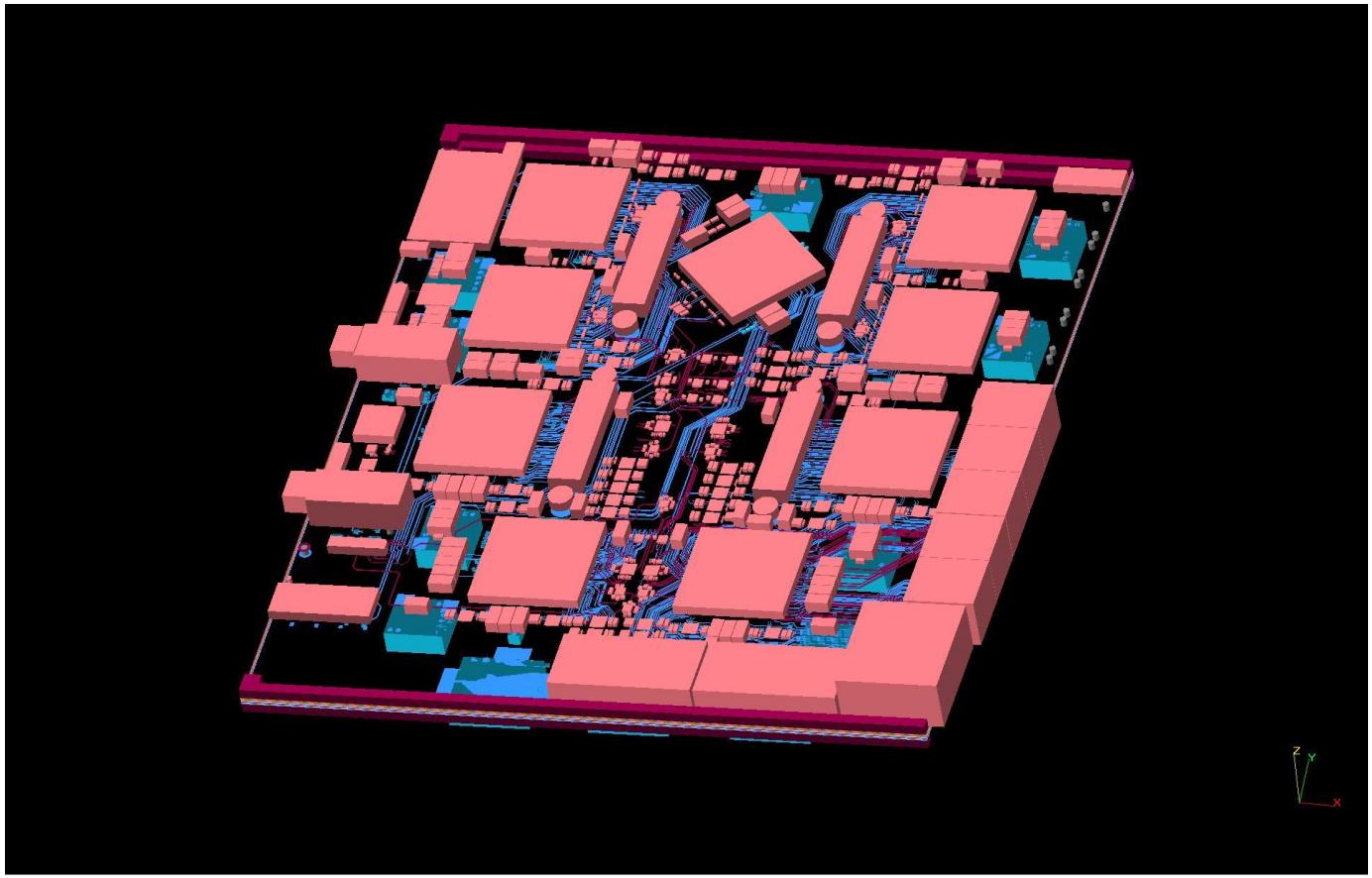
5+ 12-channel optos on daughter

Clock generation

144 multigigabit input links in zone 2 (equiv. 22300 bit / BC)



Densely packed, thick module



Production and test programme

- L1Calo internal review ✓
- Some cleanup & checks on the design (couple of weeks)
- PCB production, assembly ~ 2 months
- On-going development of service firmware, algorithmic firmware, online software

→ From July 2011 available for studies on

- Signal integrity and data transmission bit error rates
- Latency issues
- Optical interconnect schemes and link replication

→ Use for

- Test bench for topology algorithms
- System level tests along with current L1Calo modules and CMX merger module prototypes

Plans for Phase 0 / 1

- Start with detailed design work on topology processor prototypes in 2011, pending
  - Review availability and suitability of FPGA devices : Virtex 7 vs. Virtex 6 HXT
  - Finalise optical interconnect scheme
  - Review input connectivity requirements (including Muons)
  - Review processing power requirements (algorithm dependent)
- Commission production modules in 2013/14 shutdown
- Connect up with CMX and CTP
- Connect up with muons as soon as muon input signals become available
- For phase 1 no hardware modifications are currently planned, unless requirements change beyond the ones known by end 2011
- However, open for further improvements in next following long shutdown:

→ will continue to explore upcoming technologies (opto links, FPGAs, …) and ready to leverage for possible phase1 project