Phase-0 Topological Processor

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Topological Processor

Simulations suggest a need for topological trigger criteria, so as to keep Level-1 trigger effective at high luminosities.

Example algorithms:

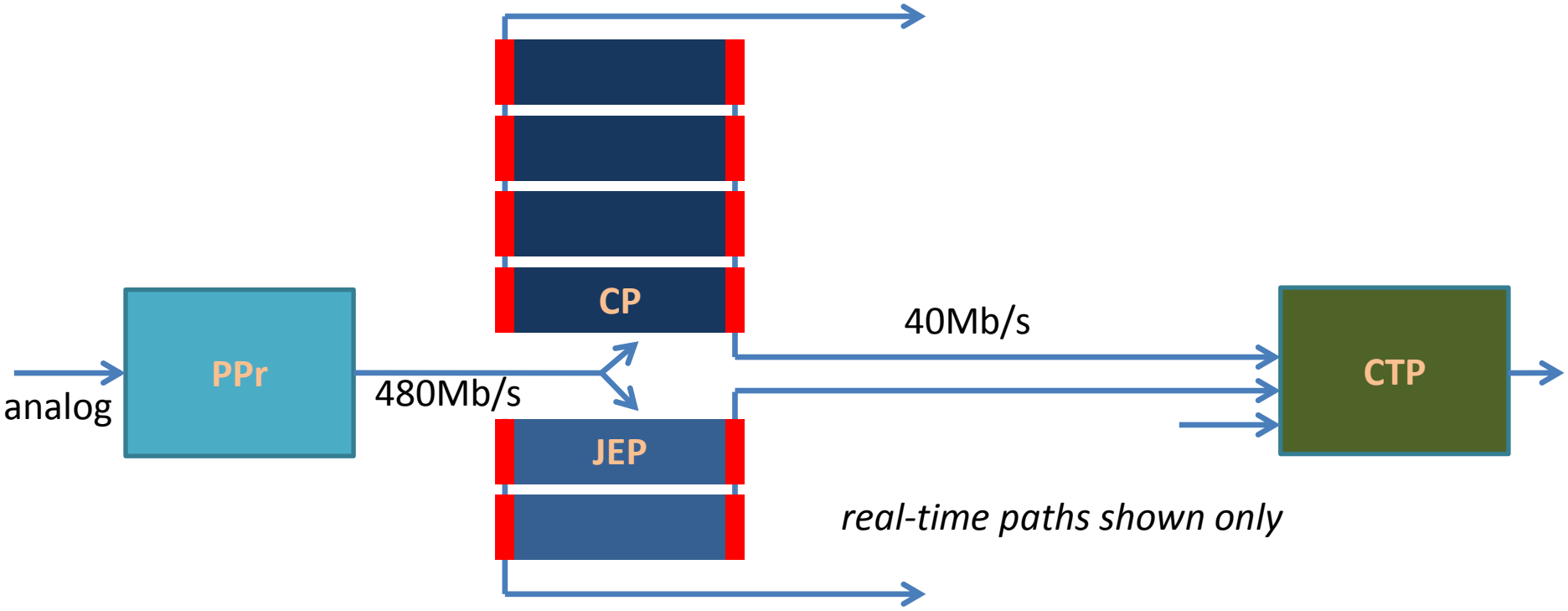
- Angular correlations (jets, direction of missing energy)
- Muon isolation
- …

Hardware implementation

→ Need to feed a maximum of data into a single point (module, FPGA)

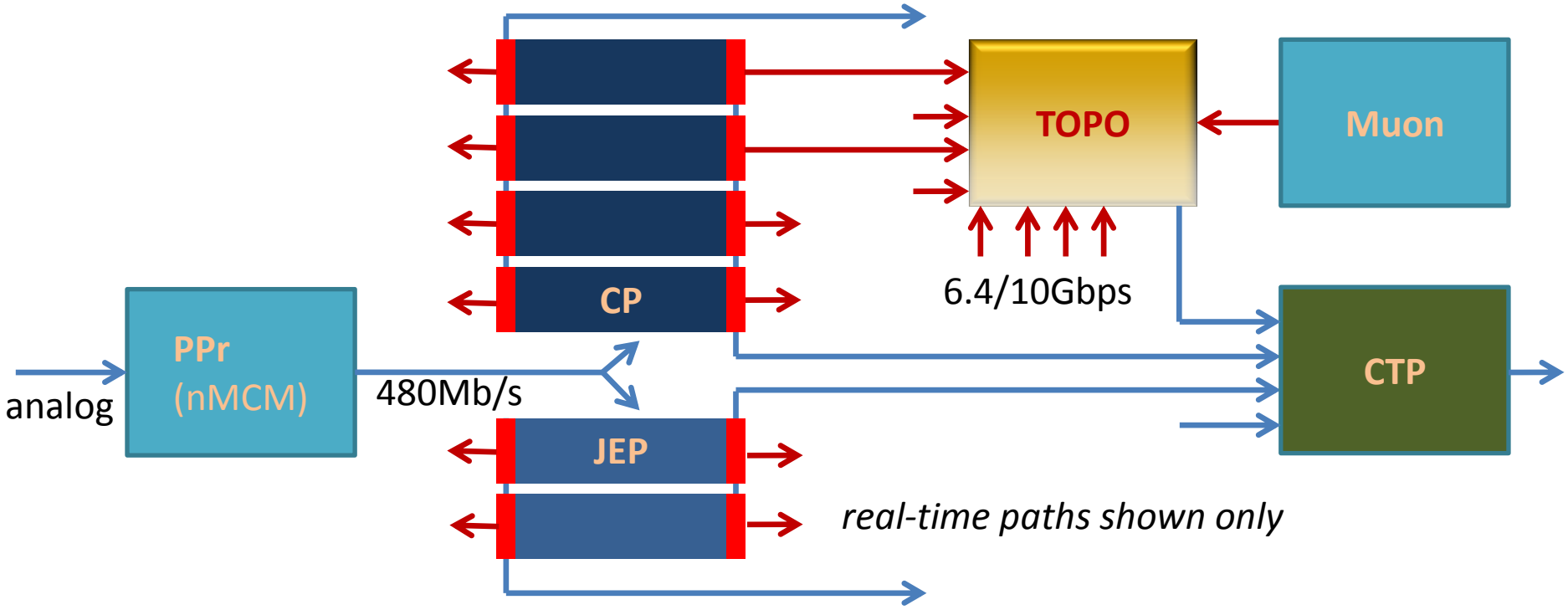
- Input from L1Calo and Muons
  - ~ 1 Tb/s aggregate bandwidth
  - Do not partition into multiple modules for reason of latency.

Current L1Calo Scheme



- Mixed Signal Pre-Processor
- FPGA based digital "sliding window" processors (e/m cluster, jet/energy)
- Object count and global quantities via chained mergers **CMM** into CTP
- Object positions to Level-2 and DAQ only

Phase 0 Scheme



- New **CMX** module with two interconnect options
  - Chained (legacy and opto links)
  - Star topology with all opto links into **topological processor**
- Muon information included on topo processor

… Topology Processor

- Input from L1Calo and Muons
  - ~ 1 Tb/s aggregate bandwidth
  - Fibre optical inputs @ 6.4/10 Gbps per fibre
- Output to CTP
  - electrical (LVDS)
  - fibre optical ~ 1Gb/s +
- Interfaces to TTC/GBT/…, Level-2, DAQ, control, DCS,…
- Small number of modules (~1)
- Probably dedicated crate, near CTP

Have started upgrade programme

- 2010 : 6.4Gb/s data source **BLT** in CP/JEP crates to live in CMM slots → CMX
- 2011 : Topo processor demonstrator GOLD

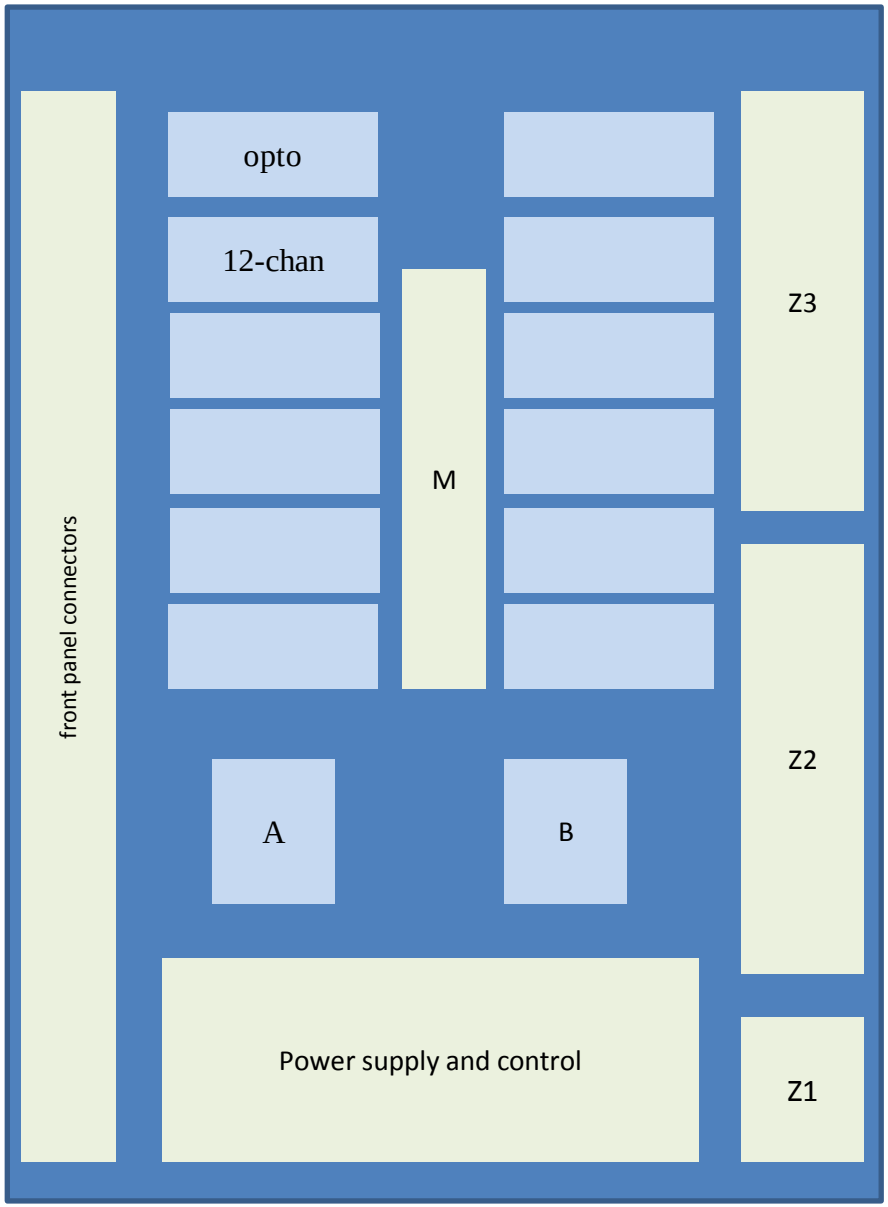
→ 2013/14 topological processor commissioned in USA15

Phase-0 Topo Processor floor plan

Mezzanine connector

A / B FPGAs XC7VX690T-FFG1927

AdvancedTCA 322x280 mm



Z3: opto connectors for real-time input

Z2: electrical connectors

Bandwidth / Algorithms / Latency

Baseline two FPGAs per processor

80 Links/FPGA @ 10Gb/s →1.6Tb/s total →1.28Tb/s payload

Preliminary data formats for jet and cluster processors:
96*(14*8+32) bit @40 MHz => 553Gb/s

For muon data assume data volume comparable to current MUCTPI input: 8*13*32 bit @ 40MHZ =>134Gb/s

Plus ε (energy, ?)

Some level of data reduction on the CMX is being considered

→ One or two FPGAs per processor seem appropriate

→ Dependent on processing resources required for algorithms one might wish to duplicate processors

- →Forward link duplication for latency minimisation
- →Multiple processors on module
- →Multiple modules in crate

Algorithms

Several algorithms have been suggested:

- Jet dφ
- Cluster dφ
- Muon isolation
- Muon MET
- Jet/cluster overlap removal

Some have been simulated and shown to be effective

Algorithms require

- Sorting of objects to size
- Cuts in η,φ
- Possibly cuts for absence of objects in given η,φ bin

→ Choose reference algorithm and put in hardware !

Reference Algorithm

- Define bandwidth requirements
- Determine consumption of logic resources
- Determine latency

- Baseline device for Phase-0 topo processor is Virtex-7
- Target for reference algorithm implementation is Virtex-6
  - Xilinx development board now
    - limitations in input channel count, link speed
  - GOLD topo demonstrator in a couple of months time

- Choose an algorithm that has been physics-simulated in MZ and shown effective: Jet dφ

Jet dφ

- Based on preliminary phase-0 JEP backplane data format
- 32 JEMs × (4 jet candidates × 14 bits + 8 presence bits) → 82Gb/s input bandwidth
- Select two largest candidates in a 6-deep sort tree
- Feed position information into lookup-table to allow for cuts in η and φ
- Report single result bit to CTP

First results on a XC6VLX240T:

- 8 % of available CLB LUT resources used
- 5 % of block memory resources used
- Algorithm latency, down to the FPGA pin : 3 LHC bunch ticks

But : mind the gap !

Latency

Latency is actually dominated by the MGT links. Including that we arrive at a total latency :

with buffered transmission scheme : 8 bunch ticks
with phase alignment : 7 bunch

Health warnings:

- Latency figures are preliminary, working on reduction
- Total latency comprises serialisation from 320Mb/s on CMX, de-serialisation to 40Mb/s on topology processor, and algorithm
- Latencies have been calculated from data sheet, obtained from VHDL simulation, and been measured
- Measured link latencies have been extrapolated from 3.2 Gb/s to 6.4Gb/s due to bit rate limitations on Xilinx development board
- Different partitioning of the sort tree into CMX / topo processor will not affect algorithm latency
- “phase alignment” low latency mode has been partially withdrawn / restricted by Xilinx for current devices (errata AR#39430)
- Eventually we will want to target Virtex-7 and should therefore deal with Virtex-7 errata rather than Virtex-6 ones

“GOLD” demonstrator / medium term plans

- (Full-function) demonstrator for phase-0 topology processor
  → https://indico.cern.ch/getFile.py/access?contribId=19&sessionId=7&resId=2&materialId=slides&confId=112739
- ATCA format, modular, optical RTM connectivity @ 6.4 / 10Gbps
- L1Calo internal review passed in May
- PCB in production / assembly
- From 08/’11 available for **signal integrity** and **latency** studies
- Test bench for topology algorithms
- Initial system tests with current L1Calo and CMX prototype
- Review input connectivity requirements (including Muons)
- Review processing power requirements (algorithm dependent)
- Topology processor **prototypes** in 2011/12, baseline : Virtex-**7**
- Commission **production** modules in 2013/14 shutdown
- Connect up with CMX and CTP
- Connect up with muons as soon as muon trigger signals become available
- . . .

Backup

The demonstrator : GOLD

- Functional demonstrator for phase-0 topology processor
- Technology demonstrator for technologies to be used throughout L1Calo upgrade programme, studies on fibre optical connectivity schemes

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- ATCA form factor
- Modular concept
  - Mezzanines
  - FMC connectors
- Optical backplane connectors rather than front panel I/O
- Opto/electrical conversion on input mezzanine
- Electrical connectivity up to 10Gb/s in ATCA zone 2
- Phase-0 topo-specific connectivity
  - Provide all interfaces

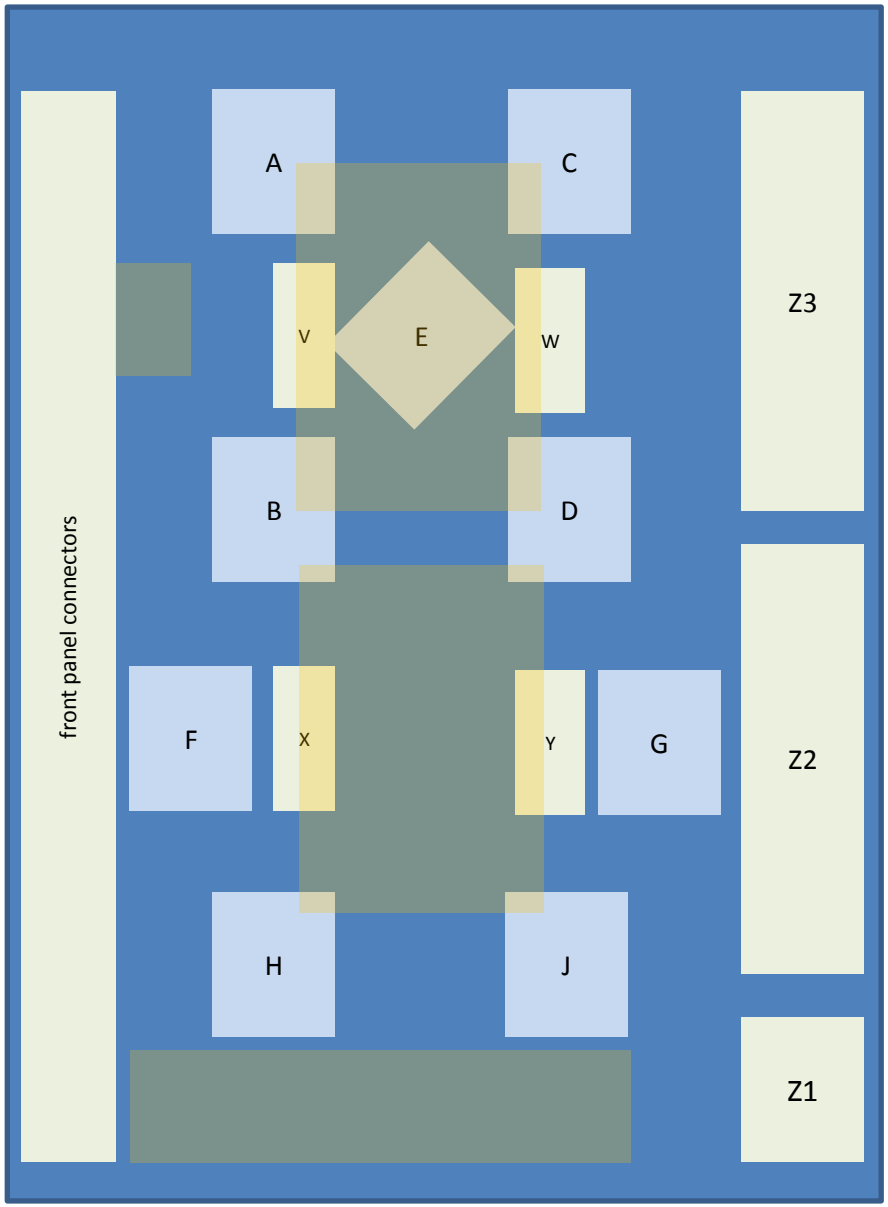
GOLD floor plan

A-J FPGAs

Mezzanines

V – Y : FMC connectors

AdvancedTCA
322x280 mm



Z3: opto connectors

Z2: electrical connectors

GOLD - some details

Main board, ATCA sized, 22 PCB layers

- FPGAs (Virtex-6 LXT, HXT)
- Connectors, sockets for e/o converters
- FPGA configurator and local clocks (DAQ/ROI, Ethernet,…)
- Main power distribution network (central and POL regulators)

Input mezzanine module, allow for choice of input devices and input signal routing

- 12 layers, moderate real estate
- Sockets for o/e converters, 10Gb/s fanout

Clock mezzanine module

- Recover and condition incoming (LHC bunch) clocks
- Some limited clock multiplexing and fan-out
- Provide additional space for auxiliary components and front panel connectivity

GOLD floor plan

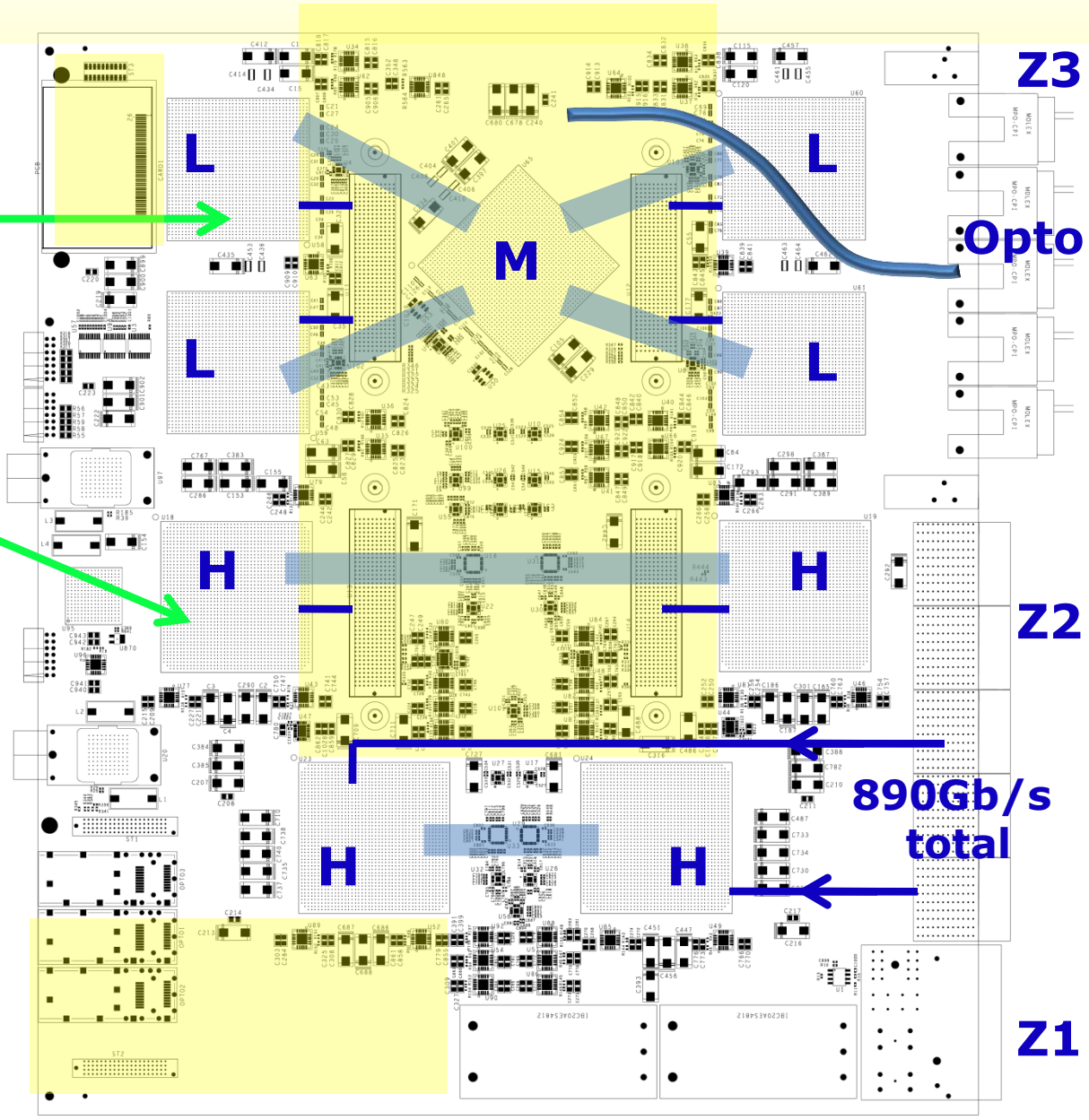
5 * XC6VLX
(Processor **L**, main processor **M**) up to 36 links each

Two pairs of XC6VHX (**H**)
72 links each

5+ 12-channel optos on daughter

Clock generation

144 multigigabit input links in zone 2 (equiv. 22300 bit / BC)



Densely packed, thick module