GOLD Status and Phase-1 Plans

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Phase 0 – GOLD hardware status

- All electronic components available
- GOLD PCB still with manufacturer
  - Due Jul. 29
  - Manufacturing problems with just one (very last) layer
    - Etching and plating currently not possible at required structure size (75µm)
    - Reason currently under investigation
    - Expect delays
    - Waiting for further information
- Slot to be negotiated with assembly company as soon as new estimate of PCB lead time known
- Mezzanine modules (initial test versions) in production
  - 12-channel receive/transmit opto module
  - Crystal clock module
  - Uncritical due to different manufacturer and structure sizes
- Mezzanine modules to be assembled in-house

Phase 0 – GOLD f/w status

- RTDP:
  - Whole Path implemented!
  - Latency approximation on Xilinx-Demoboard with half speed test done!
  - Full-speed-test: when GOLD available!
  - Trying out possibilities to minimize latency in algorithm and ser-/ deserialization: under work!
  - Algorithms: Δφ between two biggest Jets implemented & tested!
- Control:
  - VME-- from BLT(in CMX-slot) to all FPGAs on GOLD done!
  - I²C: FPGA to 12-channel o/e conv. on mezzanine done!
  - Xilinx IBERT for Multi-Gigabit-Transceivers(MGT) done!
  - Optimize settings of 12-channel-e/o-conv. and MGTs to get best signals when GOLD available!

Phase 0 – GOLD status

- Boundary Scan tool ready!

- Software:
  - Only simple C code with VME--
  - 'GUI' for I²C control of 12 channel o/e converter done!

- TODO:
  - Playback & Spy (f/w & s/w), …
  - Signal measurement with our new oscilloscope on test-input-mezzanine

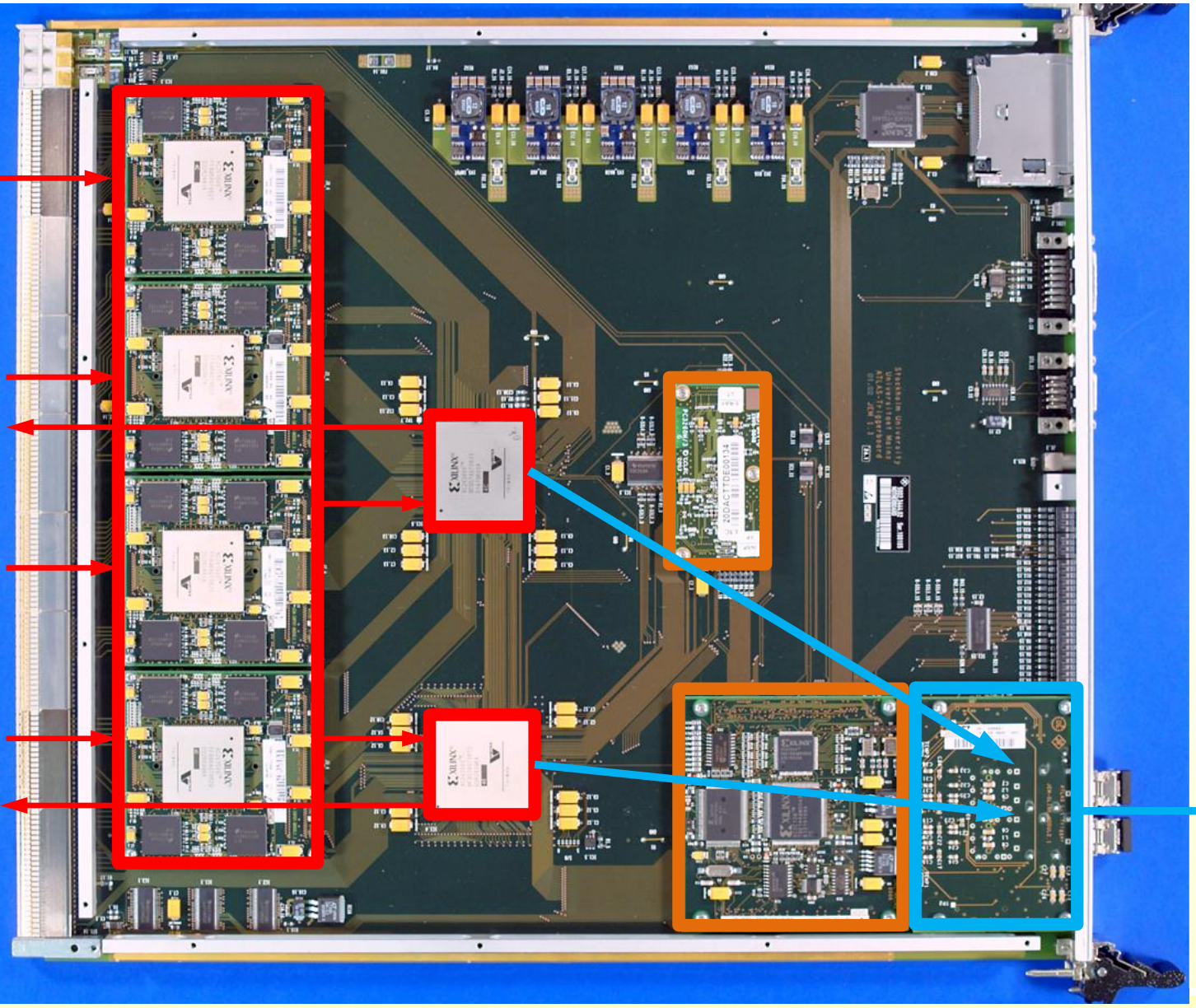
Phase 1 – plans : JEP

- JEP comprising 32 JEMs
- JEM is modular system
  - Large and empty main board
  - Seven mezzanine modules
- JEP conceived ~ Y2K
- Detailed design and production in 2003/6
- Expected to run until phase 2 (202x)
- Maintenance issue
  - FPGA design tools / device support (ISE 10.1)
  - Spare modules and electronic components
    - Number of spare mainboards seems adequate right now
    - Mezzanine modules of some concern
      - Input modules had been rather difficult to procure in sufficient quantities due to production issues
      - Problems with cleaning / drying procedure after assembly
      - A few modules had died early
      - Situation seems stable currently
    - No experience with long term operation of home built modules yet

→ Think about replacement JEMs, built in recent technology

Consider different partitioning of functionality into modules

JEM components and data paths



FPGAs and mezzanines

Real-time and DAQ paths

New Jet/Energy processor for phase 1

Minimal approach:

- Increase JEM optical output capacity by renewal of low-cost daughter modules
- Add option to downgrade JEMs to fixed functionality, non software configurable fibre driver modules via an alternative FPGA configuration
- Add new "nJEP" processor next to topology processor module, to receive JEM optical real-time output
- Keep current JEP running while nJEP being commissioned
- Eventually switch to nJEP based jet trigger

Once LArg signals are available optically at high granularity

- Run LArg fibres directly from Digital PreProcessor into nJEP
- Use old JEMs for e/o conversion of tile signals only
- Replace JEMs with simple and cheap converter modules as further spares are required
- In case we were running into a latency crisis, full JEP replacement by o/e converter modules would be effective and affordable
- Consider feeding nJEP directly from PPr, at granularity of up to 0.1×0.1 in $\eta \times \varphi$

Benefit from improved granularity physics-wise and:
once tile optical signals become available, connect them up as well

→ That might be rather phase-2ish already…

Phase-1 upgrade with new JEP