

Constraints & Numerology

Assumption: one crate, several modules.

- Each module covers full phi, limited eta range
- Data sharing with immediate neighbour only, for practical reasons
 - sensible baseline is eta coverage of 0.8 per module
 - for full eta coverage we need 8 modules
 - maximum environment size of 0.9 in eta
 - maximum environment requires 100% duplication !
- Each module will carry several FPGAs
 - assume 8 FPGAs, covering 0.8×0.8 ($\eta \times \phi$) each
 - total of 64 FPGAs for jFEX processor
 - compares to total of 32 jet FPGAs for current JEP
 - Seems reasonable due to intended improvement on granularity
- go for high density optoelectrical components
- design for short electrical traces of high speed links
- Latency aware

Components for 2018

Conservative approach: plan for devices only that are in the pipeline already now

- Virtex-7 : baseline XC7VX415T
 - Mid range
 - Several foot print compatible, larger devices exist
 - 48 GTH links (line rate dependent on speed grade/price tag)
 - Nothing currently known about possible gaps in line rate range
- 12-channel opto devices at ~10Gb/s
 - can reasonably expect that microPOD will be a viable option by then (fall-back to miniPOD)
- Expect to use ~48-fibre bundles

Basically design jFEX along the lines of L1Topo, with higher FPGA count and board-level data paths optimised for sliding window algorithm

Data replication

<< If local design density permits duplication of a small fraction of signals, it will just as well allow for large scale duplication. Just a matter of money >>

- No replication of any source into more than two sinks
- Forward duplication only
- Avoid any data retransmission
- Fan-out in eta handled at source only (DPS)
 - Try to persuade DPS to do duplication at the parallel end (on-FPGA), using additional MGTs
 - Possible fall-back: optical fibre splitting, if optical power budget permits (probably more expensive and bulky than parallel duplication)
- Fan-out in phi handled at destination only
 - Consider passive electrical splitting of 10Gb/s signals
 - Active signal fan-out would compromise design density
 - Fall-back: retransmission on parallel links → latency penalty of more than 1 tick (SelectIO SerDes).

How to fit on a module ?

- ATCA
- 8 processors
- 2-4 microPODs each
- Passive fan-out
- Small amount of control logic
- Electrical backplane basically unused



Bandwidth vs. granularity

Let's do the math for the suggested scheme. Go for the extreme. Do a rough estimate:

- Environment 0.9×0.9
- Each FPGA receives fully duplicated data in eta and phi: 1.6×1.6 worth of data required for a core of 0.8×0.8
- 256 bins @ 0.1×0.1 in $\eta \times \phi$
- Maximum aggregate bandwidth (payload @ 10Gb/s line rate) of chosen FPGA is 48*8Gb/s=384Gb/s
- per bin : 384/256 Gb/s = 1.5Gb/s, i.e. 37 bit
- That's probably ~ 3 energies
- Scalable to some extent by choice of FPGA and line rate

 \rightarrow We will be able to route large data volume into the jFEX processor chips, at large environment and at required granularity

fibre count / conclusion

- Due to full duplication in phi direction, exactly half the signals are routed into the modules on fibres
 - 192 fibres
 - 16 × 12-channel opto receivers
 - 4 × 48-way fibre bundles / MTP connectors
- The 8-module jFEX seems possible with ~2013's technology
- Allows for both sufficient granularity and large environment
- Can DPS handle the required duplication?
- How to arrive at sufficiently dense fibre contents for phase 2 (eta orientation of tile RODs ?) ?
- Is passive electrical splitting feasible ?
- \rightarrow Start to explore technologies and feasibility soon

Some further (last minute) remarks on next slide

And further...

Some last minute remarks (triggered by Sam's comments)

- Readout density into L1Topo would probably be low, leading to high fibre count into L1Topo (1 fibre per FPGA = 64 fibres total)
 - Probably depends on determination to avoid upgrade of L1Topo for phase-1
 - Consider merger FPGA (comes at the expense of more than 1 tick of additional latency)
- Not sure about maximum fibre density on a MTP/MPO connector. People talking about 72 fibres per connector, though at higher optical losses compared to 48-fibre variant !
- Readout into LVL-2 and DAQ will be included. Aiming at use of mini/microPOD at whatever data rate required by future RODs (or ROBins, in case on-board RODs are used)
- Towers .1×.1 with aggregate bandwidth of 37bits per tower available for total of e and h sections (no attempt made to sort out contents per fibre)
- Each module covering core of nominally .8 in η (different at FCAL)
- 8 FPGAs per module, each covering core of .8×.8, including environment: additional 4 bins each at +/-eta, +/- phi total data processed on one FPGA: 1.6×1.6 worth of data