Topology module : status and planning

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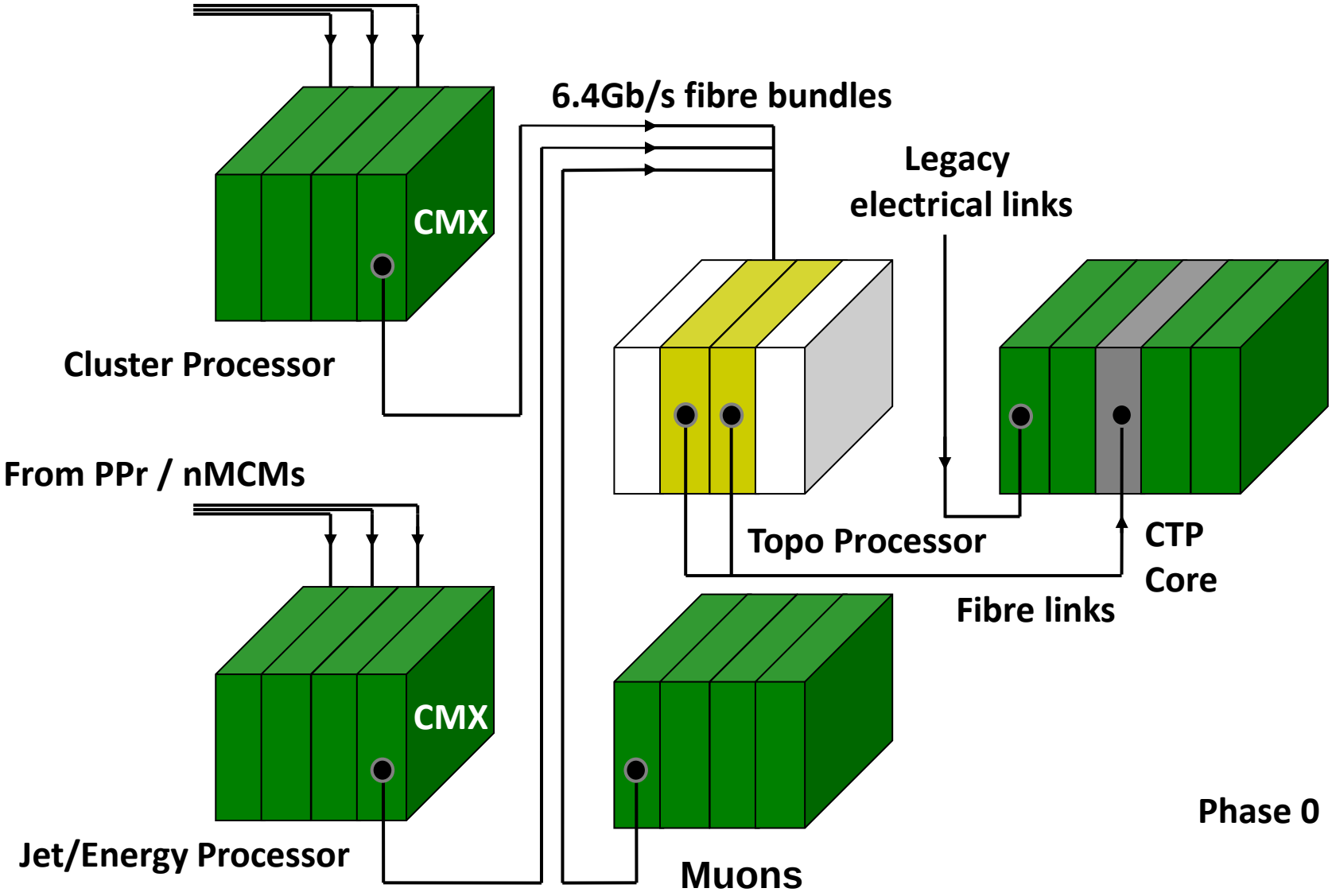
The Topology Processor in its habitat



Topology Processor

To provide a maximum of flexibility for applying topological trigger criteria

- All Level-1 trigger signals in a single module
- Allow to correlate all trigger object types within full solid angle
  - e/m clusters, tau
  - Jets
  - Missing Energy
  - Recently: muon signals in phase 0
- Ample logic resources to run many algorithms in parallel

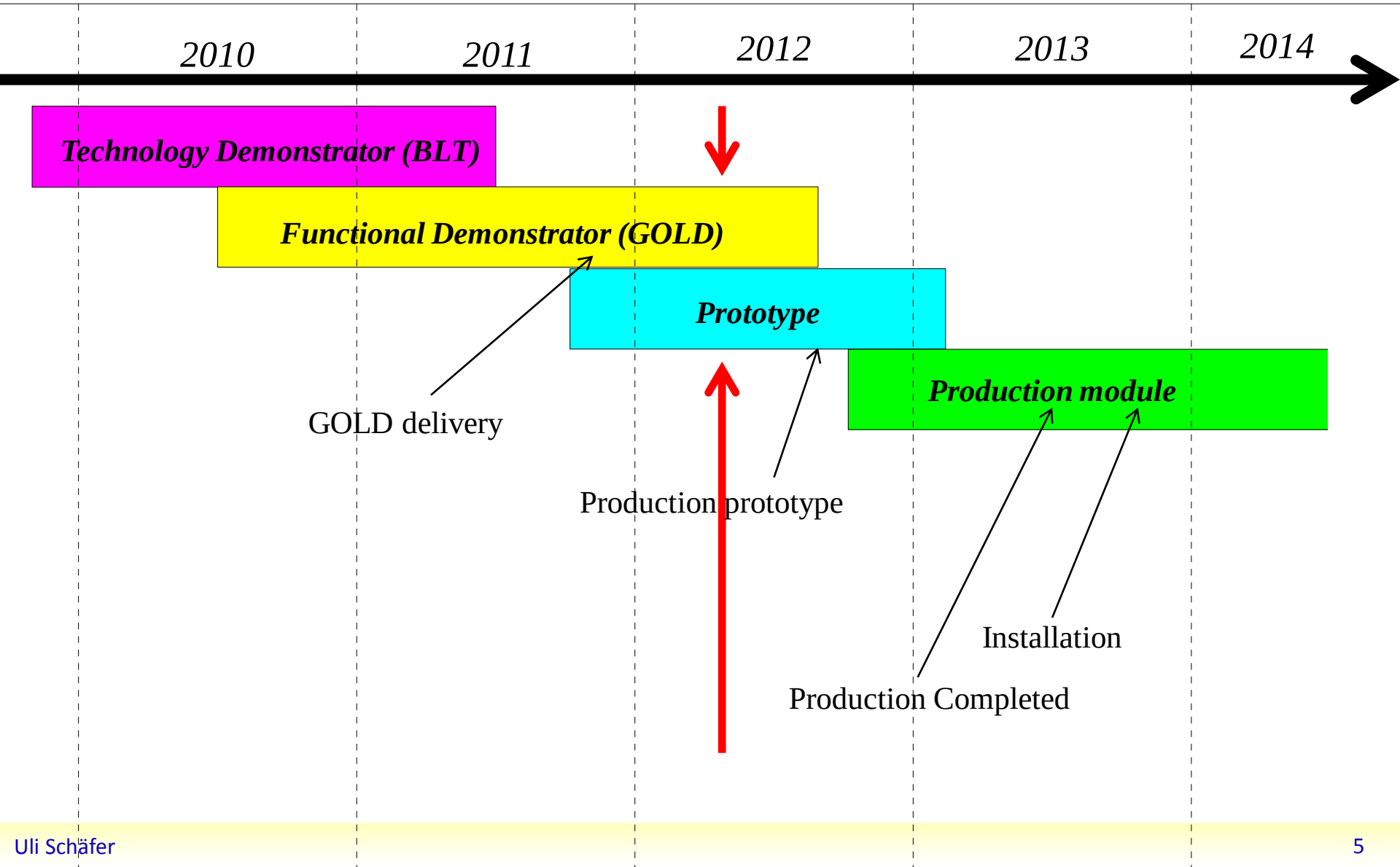
- Option to run separate algorithms on more than one topology module in parallel

Topo processor features

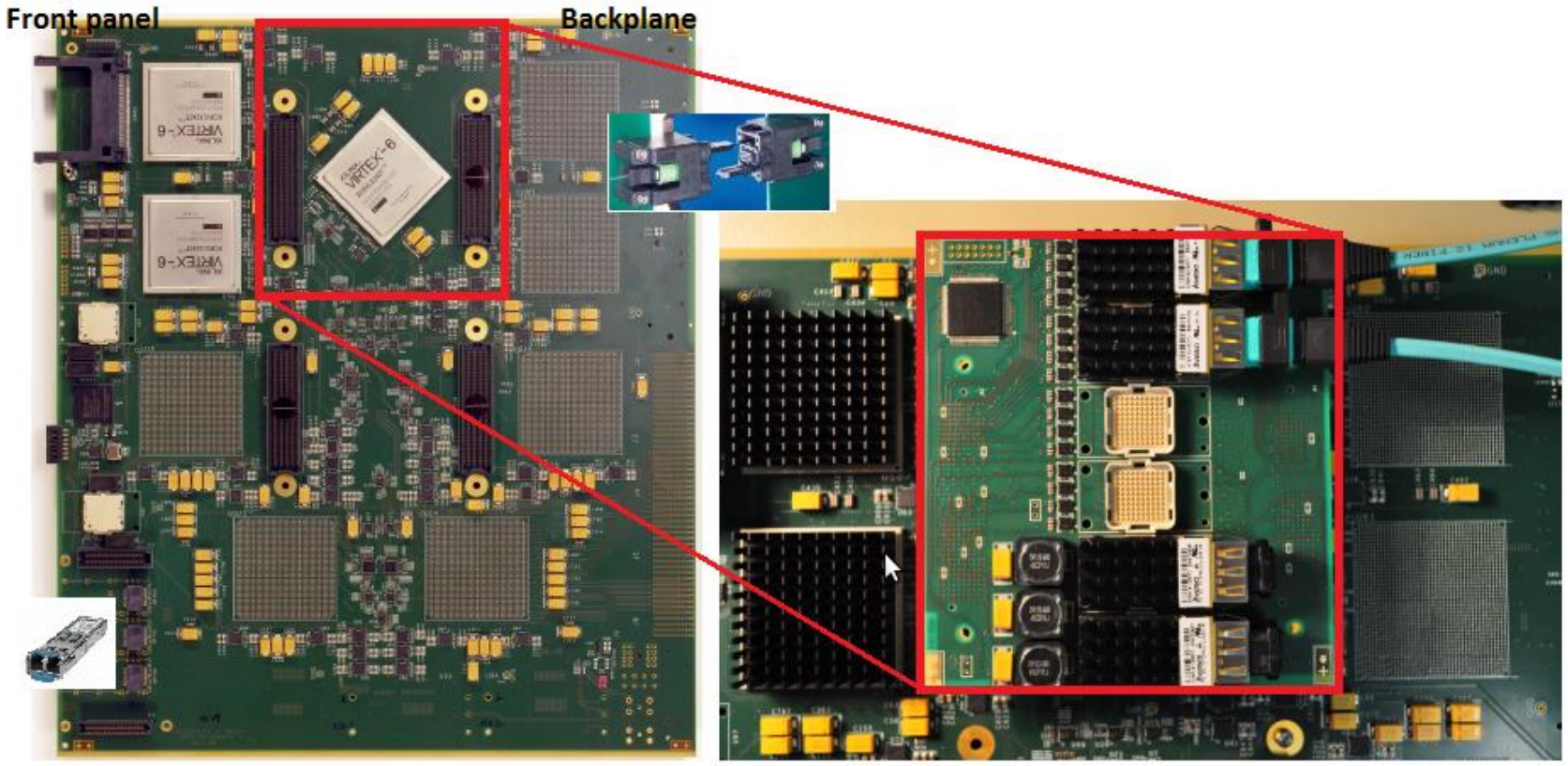
- AdvancedTCA form factor
- High input bandwidth (@ 6.4Gb/s line rate)
  - Electrons, tau, jets, MET : 553 Gb/s
  - Muons 267 Gb/s
  - Total aggregate bandwidth 820 Gb/s
- Low processing latency on real-time path
- On-FPGA multi-gigabit links
- High density 12-channel opto transceivers (10Gb/s)
- Fibre bundles from CMX
- Fibre bundle into CTP core

- Prepared for phase 1: accept line rates above 6.4Gb/s from future processors (FEXes, muons)

Topology Processor Schedule



Functional Demonstrator : “GOLD”

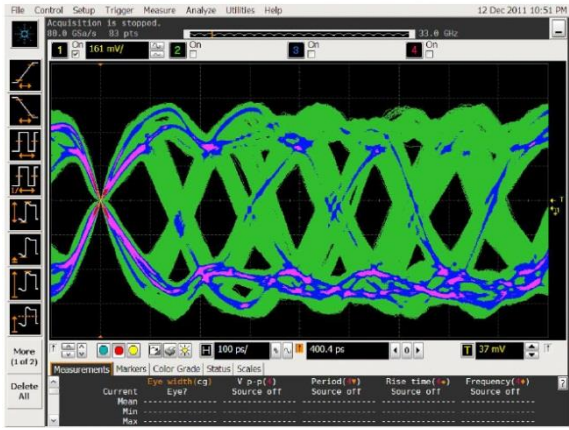


- Input from the backplane (up to 72 fibres per bundle)
- 10Gb/s 12-channel o/e converters on mezzanine
- High performance FPGAs (XC6VLX240T) with multiple 6.4Gb/s transceivers
- Output from opto links on the front panel towards CTP

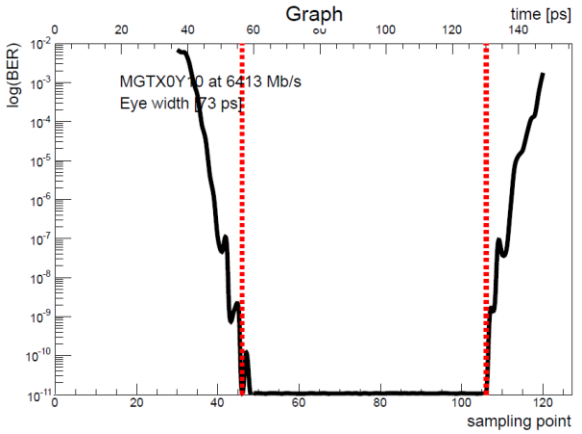
GOLD : first tests and results

- PCB partially assembled
- Smoke test / boundary scan
- Fibre loopback tests
- Signal integrity (eye diagrams, eye scan)
- Transceiver parameter optimisation

→ Successful @ 6.4Gb/s, BER < 5e-16



- Initial set of service- and algorithmic firmware exists
- Latency optimisation:
  - Used to be 7-8 ticks including MGTs
  - Recently: n-input parallel sort tree (n*(n-1)/2) comparators
    → ~ 1 LHC bunch tick for full jet channel count



GOLD : some current activites

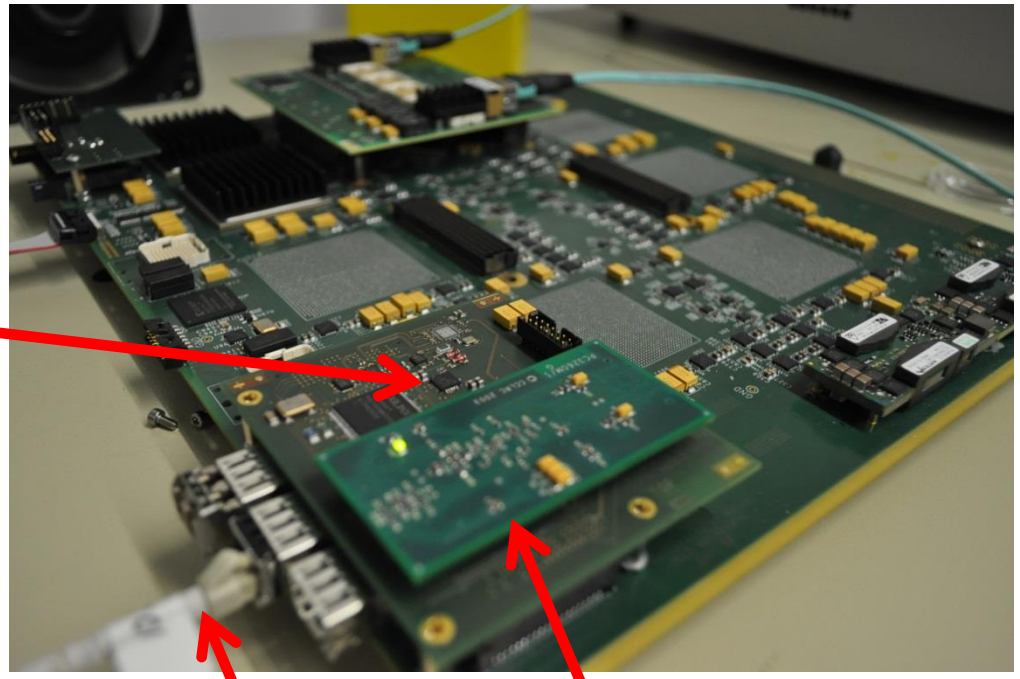
Convert Gigabit links to LHC synchronous operation

- TTCrx daughter
- Jitter cleaner

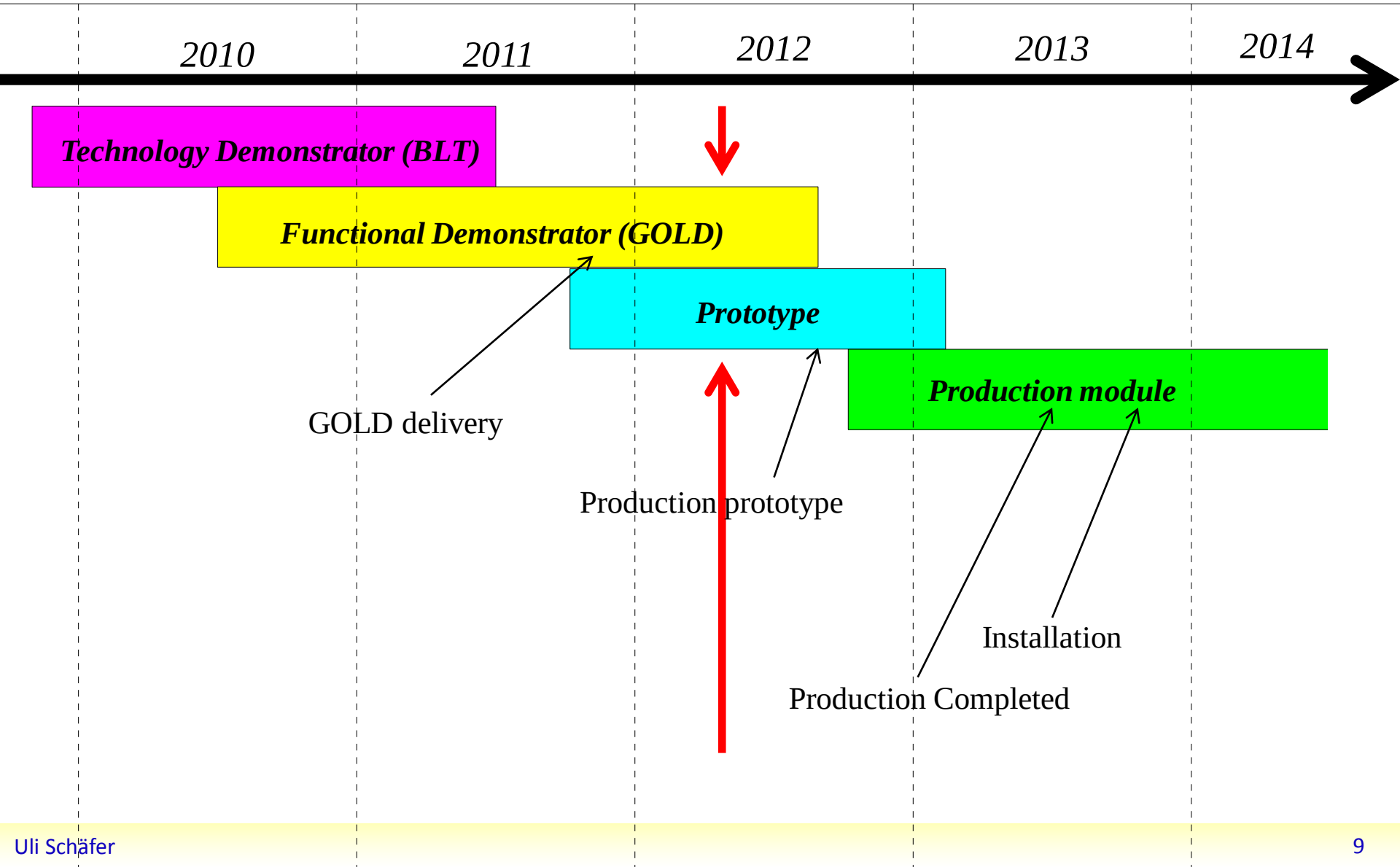
Systematic tests on all electrooptical data paths

Look into multi-fibre connectors (MTP/MPO up to 72 fibres) / attenuation

Latency, latency, la….

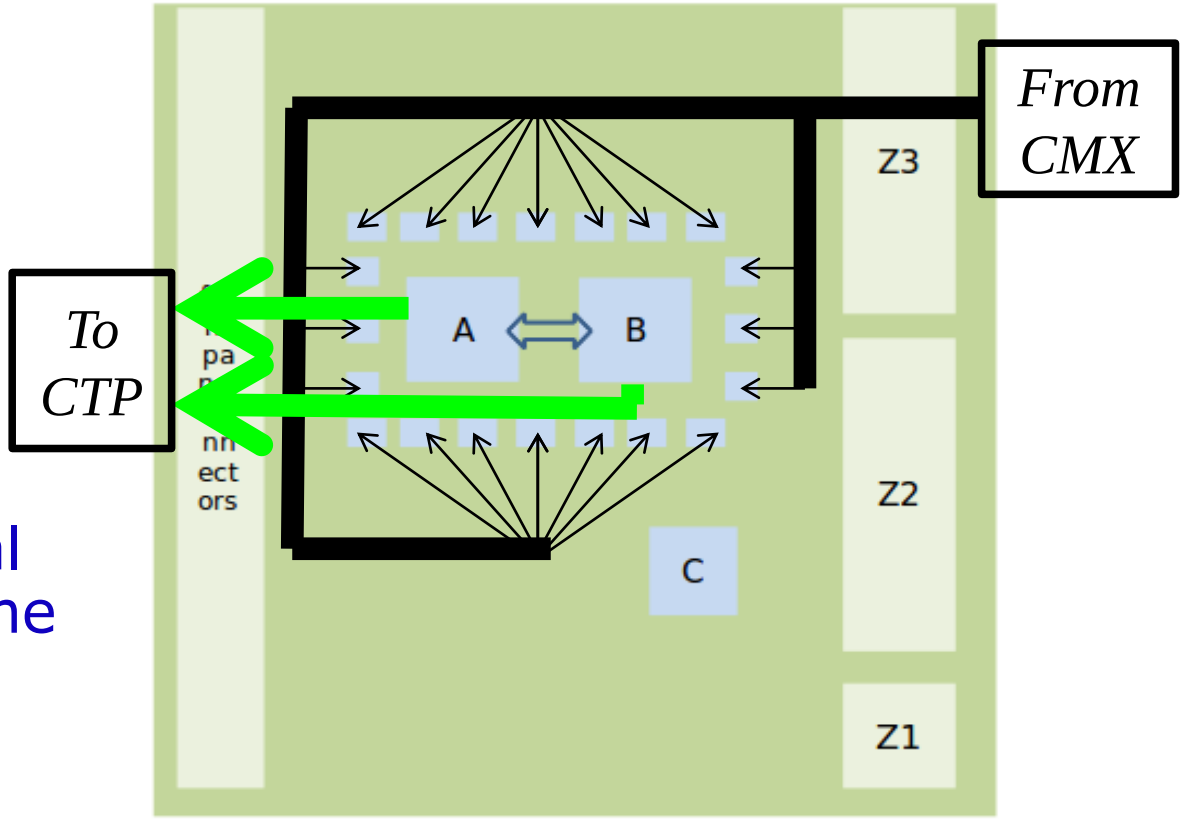


Topology Processor Schedule



L1Topo prototype design

- Fully ATCA compliant
- Minimize FPGA count
- 2 * XC7V485T
  → XC7V690T
- 1 XC7K325T (C)
- Short multi-gigabit traces
- High-density mid-board o/e converters (miniPOD) on main board
- No on-board electrical duplication of real-time signals
- Require upstream duplication



L1Topo : Milestones

Specifications for prototype under way:

- 30.05.2012 design review
- 29.09.2012 prototype layout finished
- 01.12.2012 production/assembly completed

Start preparations for final module production in parallel with prototype module tests. Make prototype module available for initial tests / commissioning @ P1

- 04/2013 prototype system tests at P1 finished
- 05/2013 PRR
- 08/2013 production finished
- 11/2013 start commissioning at P1
- 07/2014 commissioning finished

Summary

TP functional demonstrator (GOLD):

- Partially equipped and successfully tested
- Data path between FPGA and o/e converters works
- Parameters optimized at 6.4 Gb/s
- Large bit-error free window
- Further optimization on high speed link parameters and performance of algorithms in hardware ongoing

TP Prototype:

- Design ready, schematic capture in progress
- Preparing documents for the review (05/ 2012)
- On schedule for installation during shutdown 13/14