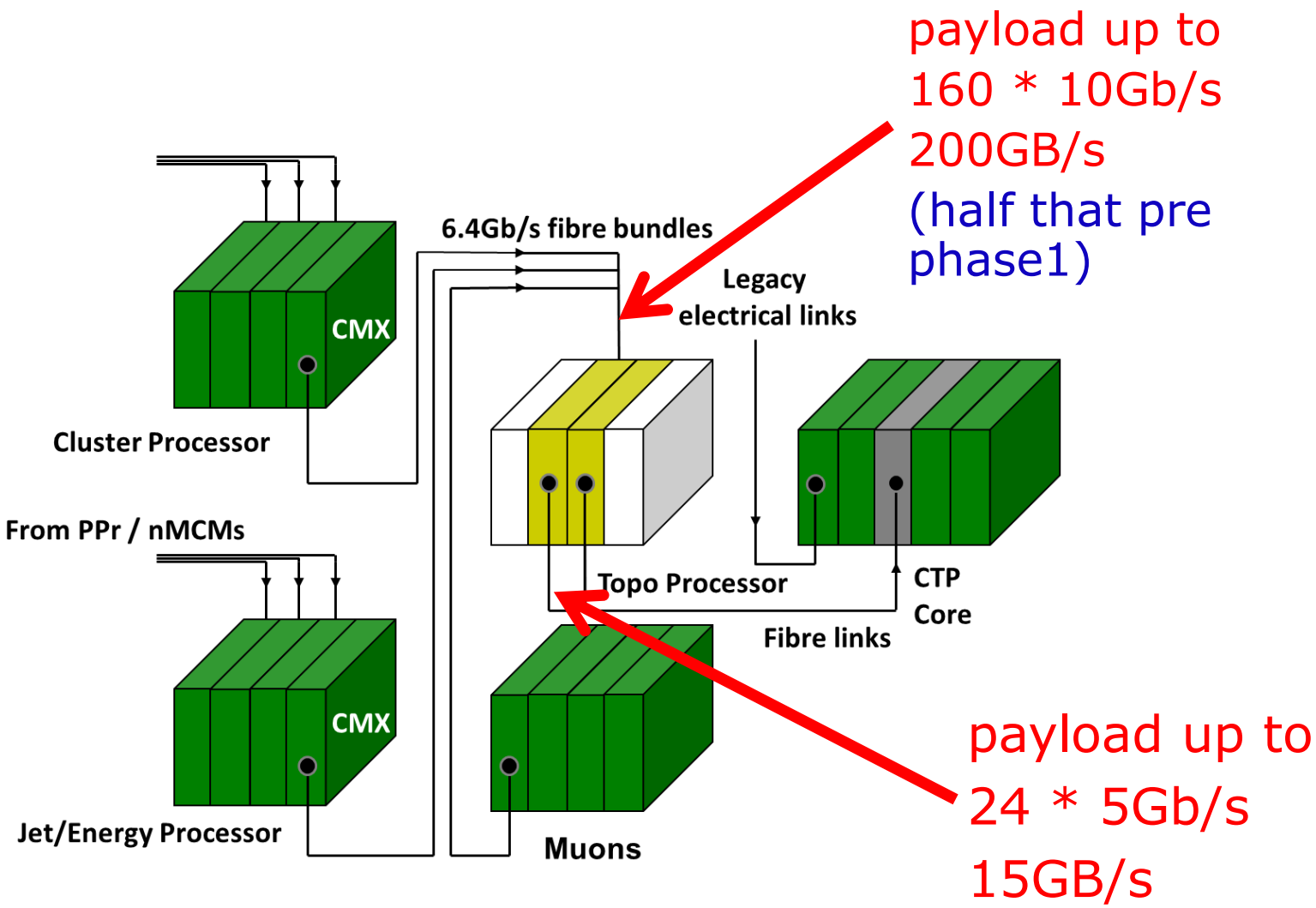
L1Topo : schedule and planning

Uli

Intro


payload up to
160 * 10Gb/s
200GB/s
(half that pre phase1)
6.4Gb/s fibre bundles
Legacy electrical links
CMX
Cluster Processor
From PPr / nMCMs
CMX
Jet/Energy Processor
Topo Processor
CTP Core
Fibre links
Muons
payload up to
24 * 5Gb/s
15GB/s

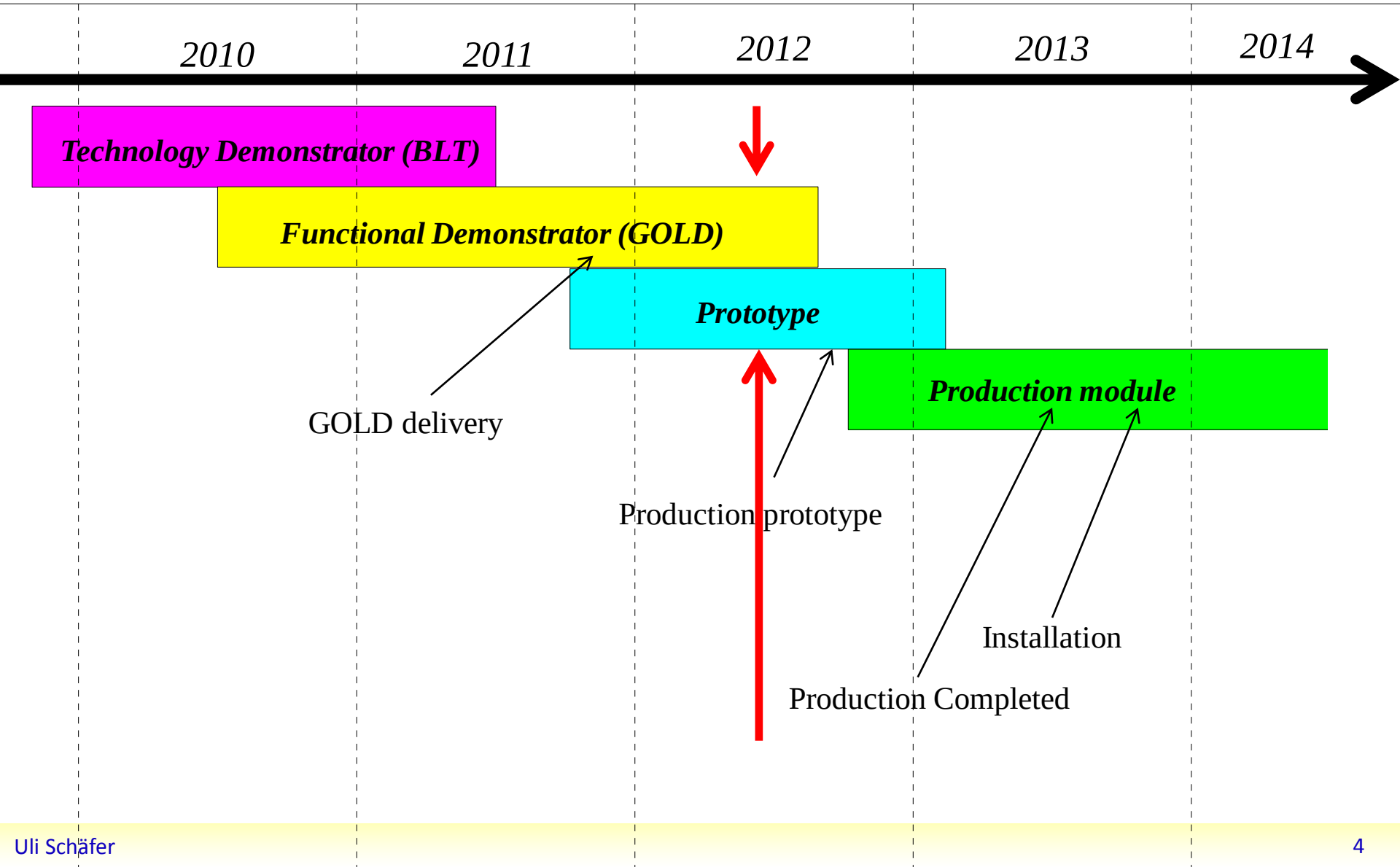
Intro

Allow for any conceivable topological algorithm:

Route a maximum fibre count / data volume into individual module / processor

- Bandwidth estimated for Stockholm (2011)
  - Electrons, tau, jets, MET : 553 Gb/s (pre phase 1)
  - Muons 267 Gb/s (phase 1)
  - Total aggregate bandwidth 820 Gb/s
  - Achievable @ 6.4Gb/s line rate
- Bandwidth available for phase 1 with FEXes
  - twice that @ 13Gb/s line rate
  - supported by FPGAs
  - Roadmap for pluggable opto components unknown
- Scalable in terms of bandwidth and processing power
  - FPGA type
  - Module count
- Consider some electrical, low latency real-time path

Schedule

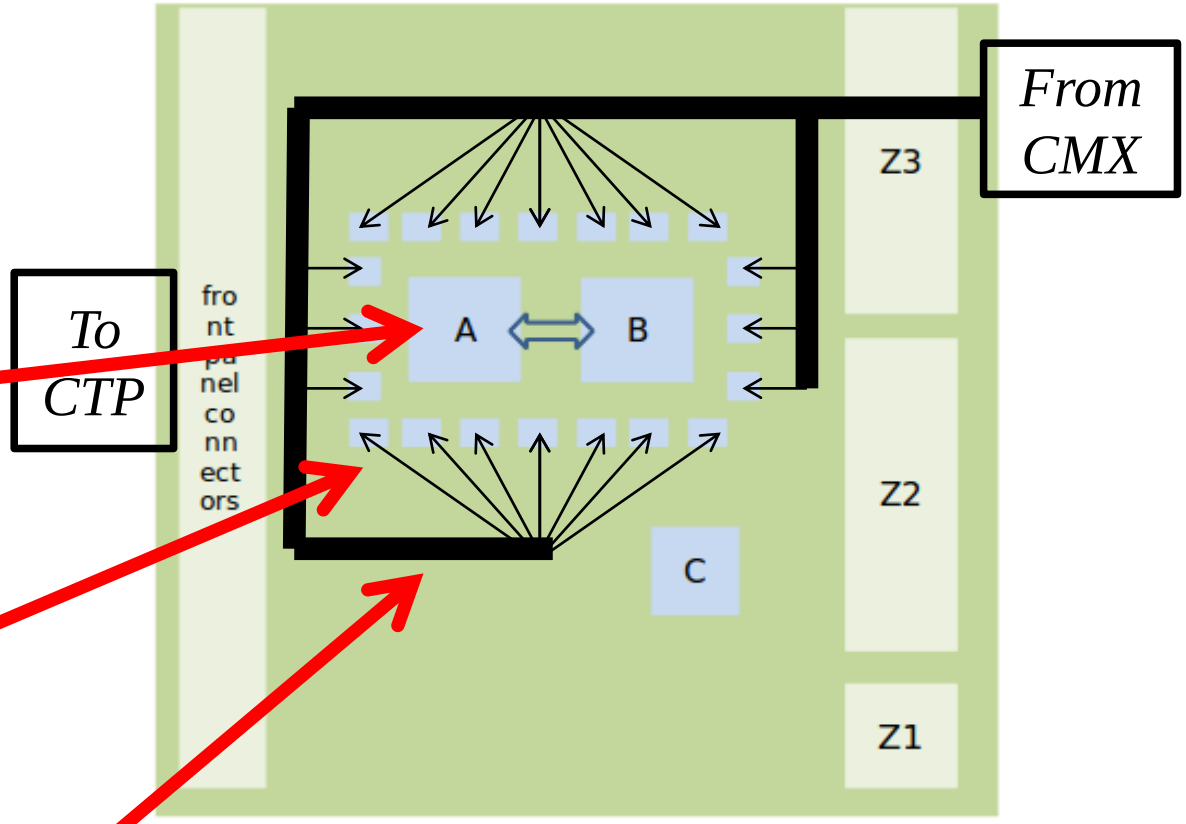

2010
2011
2012
2013
2014
Technology Demonstrator (BLT)
Functional Demonstrator (GOLD)
Prototype
Production module
GOLD delivery
Production prototype
Installation
Production Completed

(critical) components…

Design goal: Keep compact, with short traces and no on-board signal duplication

→ require:

- FPGAs A, B XC7V485T
  → XC7V690T
- 1 XC7K325T (C)
- High-density mid-board o/e converters (miniPOD)
- High density fibre plant



Next steps

- Have L1Topo review, session on June 12 (afternoon) @ CERN
  - Focus on system issues and interfaces (?)
  - Reviewers identified
  - Preparation of documents under way
  - Will turn up soon at http://www.staff.uni-mainz.de/uschaefe/ATLAS/Topo/
- Urgently purchase critical components in **JUNE !!!**
- FPGAs: Virtex-7 and Kintex-7: engineering samples on 1st prototype module, production silicon of XC7V485T thereafter. Final L1Topo production will be with footprint compatible XC7V690T
- Opto modules: miniPOD seem to be available at acceptable lead time and cost
- Fibre plant: baseline is 48-way MTP to POD octopus cable, again, seem to be available at acceptable lead time and cost

!!!!!

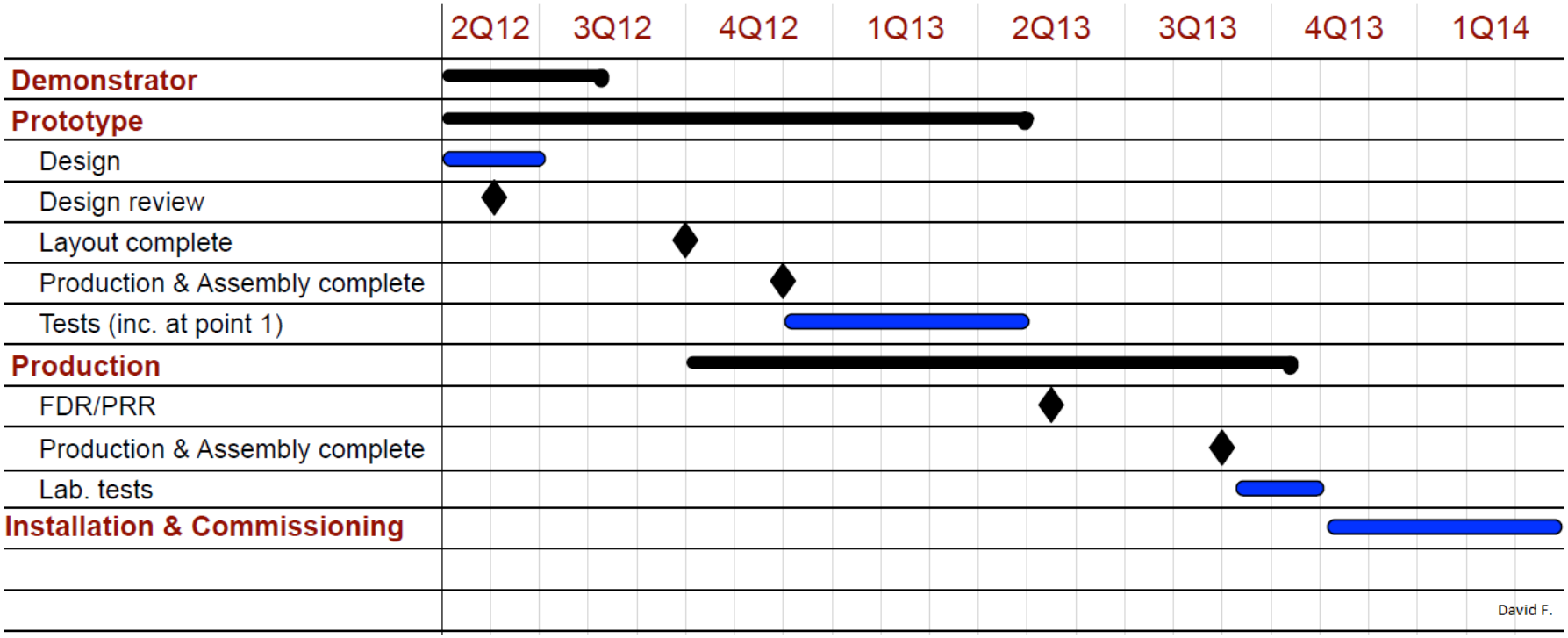
We do not want to separate L1Topo development from FEX R&D → have people talk about components and options **NOW** i.e. before volume purchase for L1topo proto modules (due mid June)

!!!!!

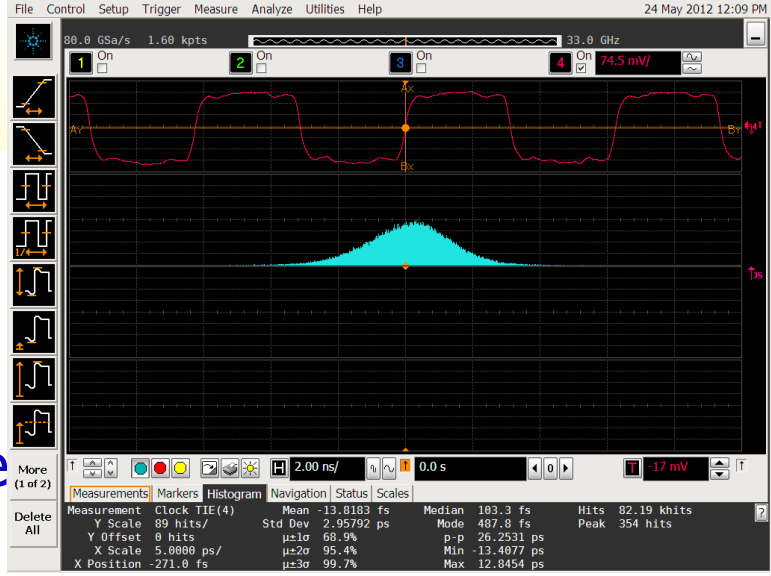
Schedule

TDAQ Phase I (2014)

- Topology module Tentative planning [April 2012]



GOLD



- f/w development on-going
- Verification of h/w functionality
  - Jitter cleaner ok
  - Some bug fixes on opto module
- Within a fortnight:
- Systematic tests on large numbers of input channels
  - Using jitter cleaned TTC clock
  - Tune Mainz TTC system for 40.08 MHz operation
- By mid June:
  - PMA far end loopback latency
  - Algorithm tests on GOLD
- Further on: operate miniPODs on GOLD

Summary / outlook

- GOLD measurements on-going
- L1Topo prototype on schedule
- Review mid June
- Urgent need for purchase of critical components
- Try and converge on opto/electrical equipment for imminent and future processors

Backup / components

Opto modules : single manufacturer, NDA on docs

- Choice of device types
  - Round ribbon vs. bare (flat) fibre ribbon
  - No heat sink vs. heat sink

Fibre assemblies : probably several manufacturers, documents on the web

- Choice of # fibres per POD connector 48
  - Choice of Round ribbon vs. bare (flat) fibre ribbon

Need to make sure fibre assemblies actually fit the modules

MPO/MTP connector - define gender : male connector on processor side

Can we try and converge very soon ? Rather pointless to go in different directions on various L1 modules.

→ review Jun 12