L1Topo / post review

www.staff.uni-mainz.de/uschaefe/browsable/L1Calo/Topo

Observations, options, effort, plans

Uli

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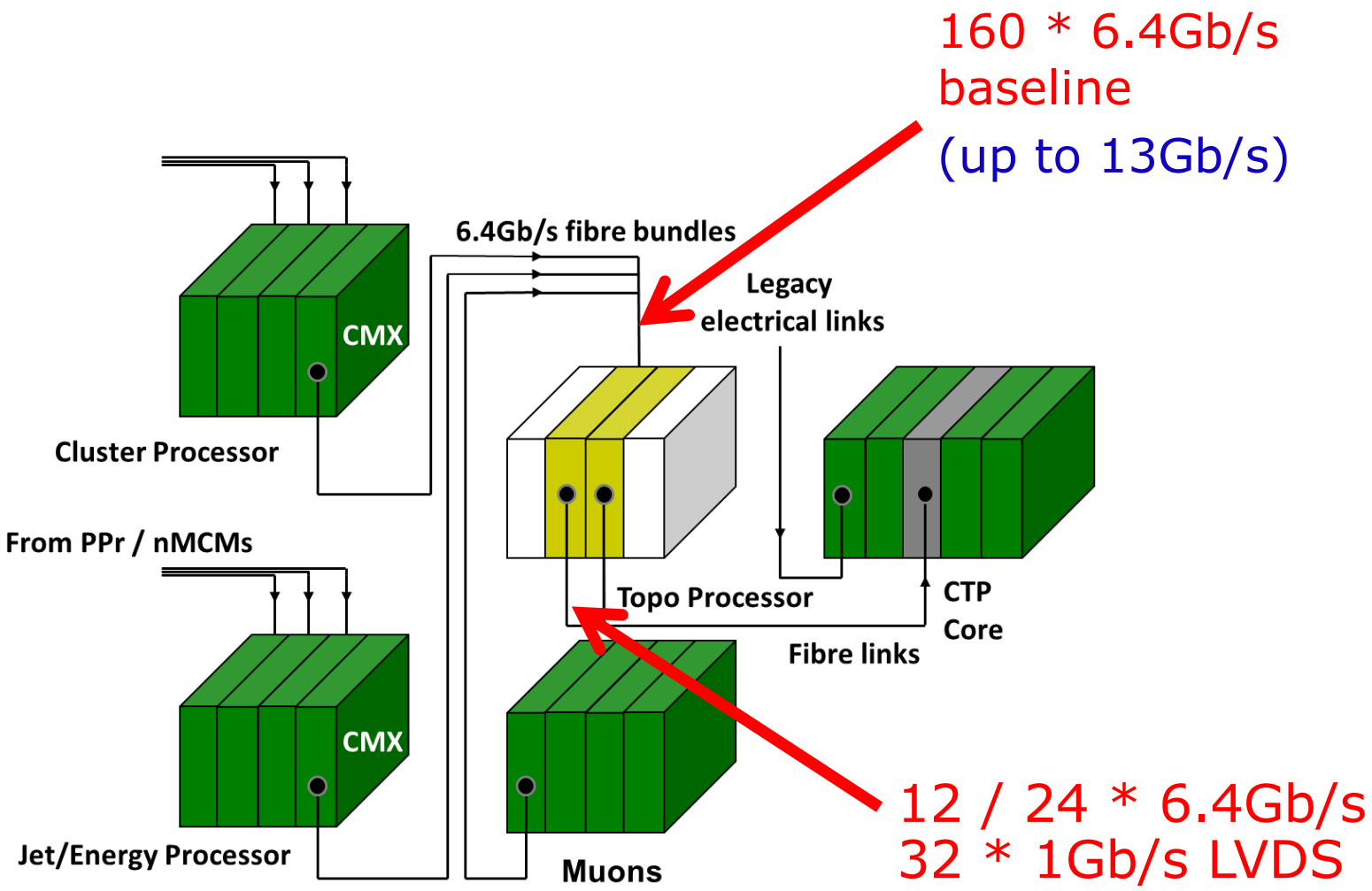
Intro – LVL-1 2013/14



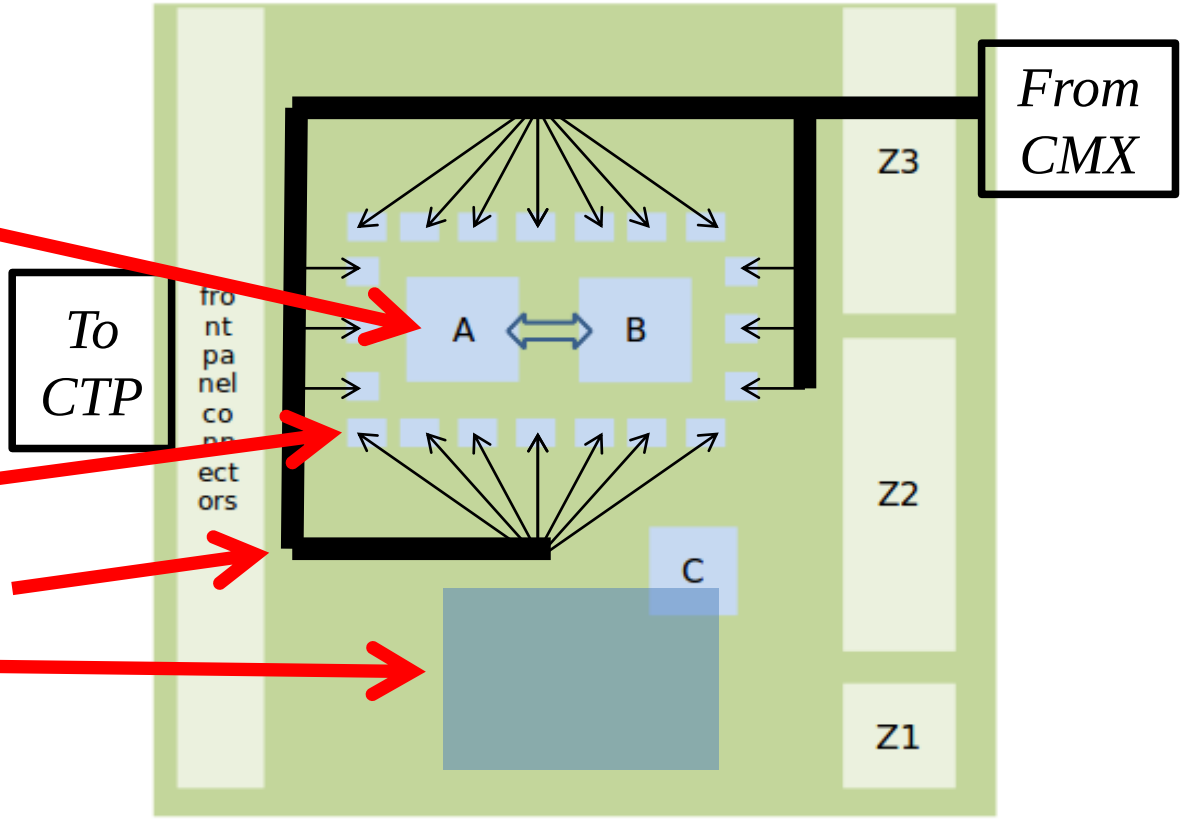
Floor plan, main components…

Design goal : Keep compact, with short traces and no on-board signal duplication

Form factor : advancedTCA

→ require:

- 2 processor FPGAs
  A, B: XC7V690T
  (XC7V485T initially)
- High-density mid-board o/e converters (miniPOD)
- High density fibre plant
- Module control
  - Kintex (C)
  - Zynq



L1Topo : some observations

Review on June 12, report available in EDMS. Quite a few comments on both technical and organizational issues

Some observations:

- Real-time bandwidth and processing capacity defined by FPGAs available on the market by 2013. Have chosen largest available devices anyway. There is no alternative to the present design!
- L1Topo is a modular processor that allows for optional components on mezzanines without too much impact on main board design.
- Large (confusing?) number of options presented in specs
- In the review session further options suggested by reviewers
- Need to consolidate design while keeping options
- Need to flag more clearly what's on mainboard and what goes to mezzanines
- Need to explore impact of options on the required effort : Seems rather obvious in the hardware regime. However, firmware and on-line software affected !

Hardware mods envisaged

Comment on…	Design mod	Impact	on
ATCA compliance	Add base interface and suitable IPMC	Low - need to copy a proven microcontroller scheme	Mezzanine
Module control via embedded processor	Replace / complement Kintex by Zynq (FPGA w. ARM processor)	Low – both devices are similar. Have to understand Zynq. Kintex and/or Zynq ?	Mainboard partially on mezzanine?
Optional PCIe based module control	?	Low	Mainboard
DAQ / ROI	Check bandwidth – probably no h/w mods	?	?
MGT reference clocks / MGT rates	Add a few more clocks	Low	Mainboard
FPGA configuration	Add SD card (on Zynq)	Low	Mainboard

Floor plan, so far…

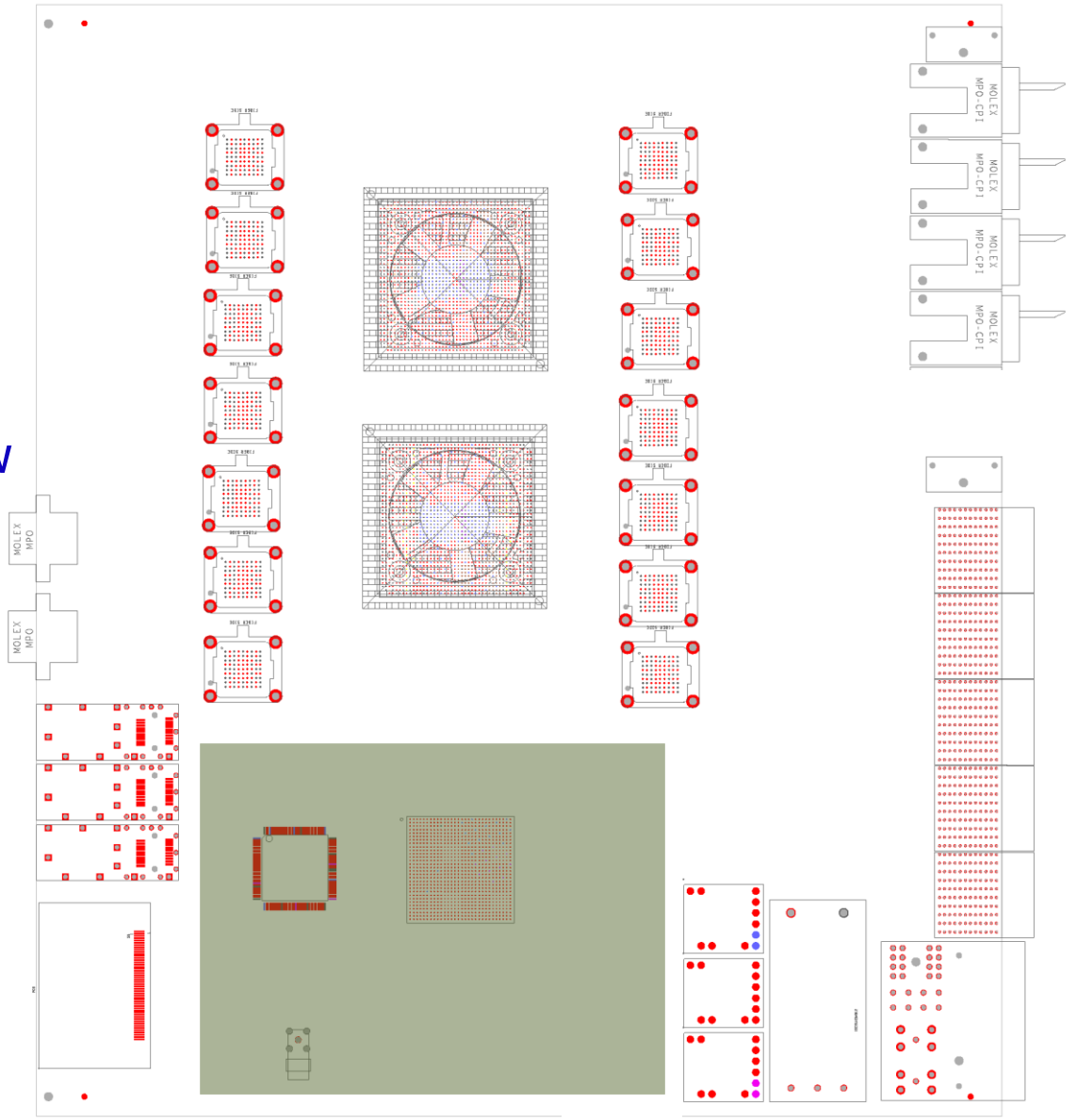
RTDP:

- High density fibre plant w. 48-way connectors
- 14 miniPODs for optical input
- 2 processors XC7V690T
- To CTP: miniPOD and low latency LVDS

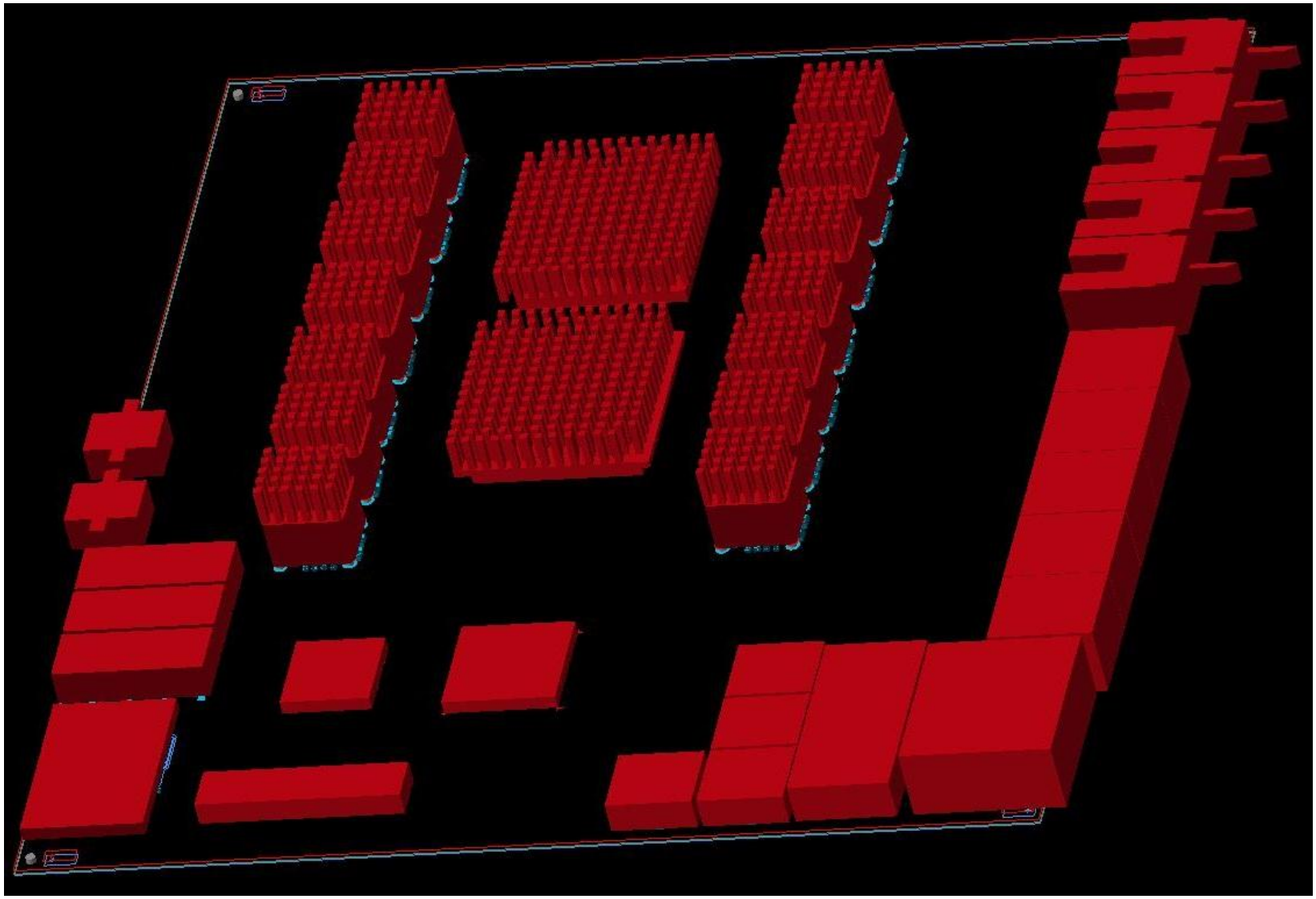
Control etc.:

- XC7K325T and/or XC7Z0XX
- Add SD-card for configuration and boot
- Add memory

Some components not yet placed : CTP /spare PODs…



… and in 3-d



Firmware, on-line software

Impact of architectural decisions on f/w and s/w might be considerable:

- Embedded ROD vs. use of L1Calo ROD
  - JEM DAQ interface being converted to L1Topo needs
  - **Phase-0** DAQ bandwidth dominated by CMX link volume : Zero suppressed fmt w. 46 fibres @ 6.4 Gb/s @ 100kHz L1A → ~500 Mb/s per bunch tick being read out, 1.7 Gb/s/tick for uncompressed data (96bit/processor slot)
  - Effort required for embedded ROD cannot be quantified
- Ethernet based control / embedded processor / IPbus
  - Basic access via serialised VMEbus is available anyway, is in use on GOLD
  - Both IPbus and embedded processor are supported by h/w but will require s/w and f/w effort

Effort & needs

MZ figures haven't changed:

- h/w Bruno & Uli
- f/w
  - Volker W. working on real-time f/w
  - ~ 1 FTE of postdocs
- s/w – so far none beyond some minimum VME-based control software required for hardware tests / PHD students

Firmware required:

- Real-time path
  - MGT related stuff
  - Some topology algorithms
- Diagnostics and monitoring (playback / spy)
- Register map
- DAQ
- IPbus firmware (for FPGA-based Ethernet option)
- PCIe ??

Software required:

- Some basic software access for h/w tests
- HDMC register description (in case of register mapped access)
- General software framework for Ethernet based control
- Embedded processor software (ARM/Linux) **or**
- IPbus specific software
- Microcontroller software (IPMC)
- PCIe ??

S/W development would be eased considerably if done within L1Calo infrastructure

PCB status and components

- Detailed design under way
- Incorporate some design modifications inspired by review
- Initially engineering samples on prototype
  - 1st copy using XC7V485T-2CES – ordered / available soon
  - 2nd copy using XC7V485T-2C – ordered / available Q4, 2012
  - XC7V690T from 2013
- Initial batch of miniPOD trans/ceivers ordered / available soon
  - With heat sink
  - For bare fibre connectors
- First samples of fibre assemblies (48-way) ordered / being ordered.
  - POD connector style : for bare fibre
  - Male MPO/MTP connector
- Lead times seem reasonable