L1Topo Status & Plans

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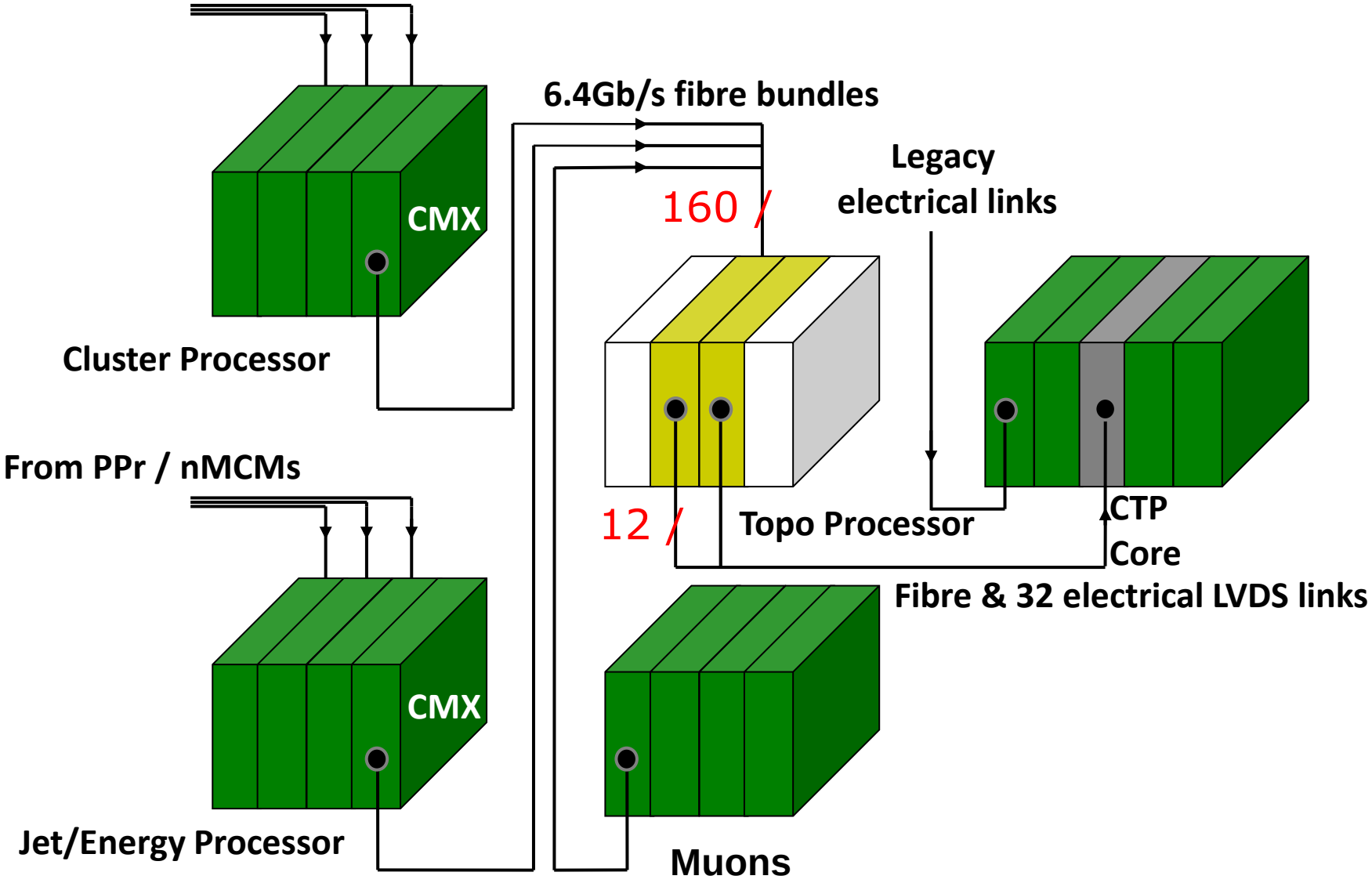
Topology 2013/14 (RTDP)



Topology Processor

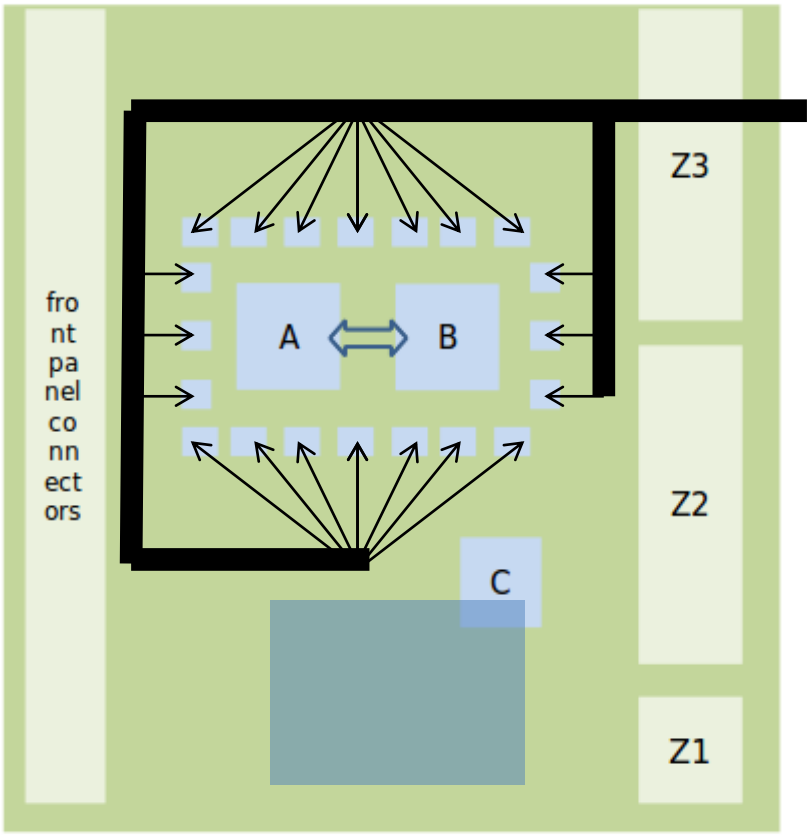
To provide a maximum of flexibility for applying topological trigger criteria:

- Maximise aggregate input bandwidth without compromising on on-board RTDP bandwidth
  - Two high-end processors
  - 820 Gb/s @ 6.4Gb/s (2014 baseline rate)
  - Jets, clusters, Muons into single module
  - Allow to correlate all trigger object types within full solid angle
- Option to run separate algorithms on more than one topology module in parallel
- High density 12-channel opto transceivers (miniPODs)
- Fibre bundles from L1Calo CMXes and Muons
- Both fibre bundle and low latency LVDS into CTPcore
- Some critical circuitry on mezzanine, to allow for later mods
- Make use of data duplication at source, if required

- Well prepared for phase 1:
  - accept line rates above 6.4Gb/s from future processors (FEXes, muons)
  - Employ zero suppression

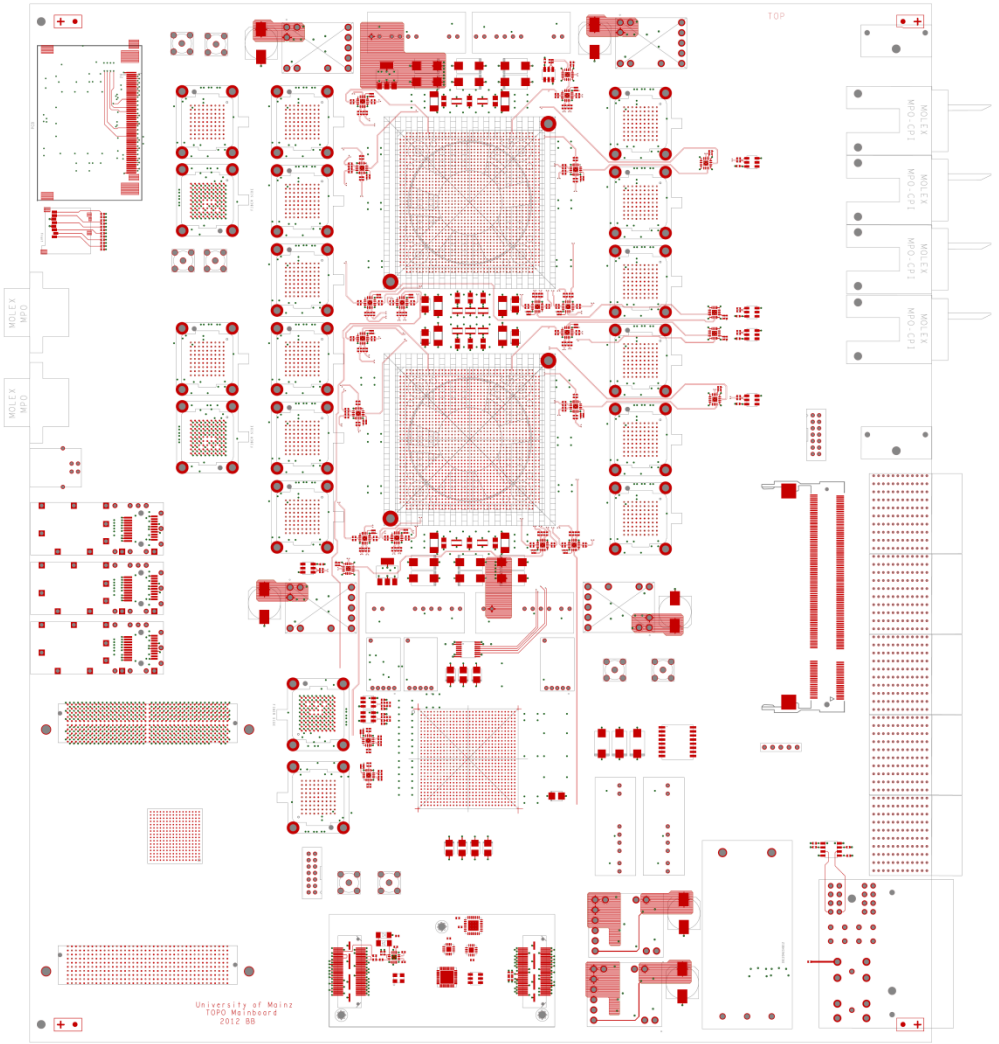
Topo processor details – post PDR

- Real-time path:
  - 14 fibre-optical 12-way inputs (miniPOD)
  - Via four 48-way backplane connectors
  - 4-fold segmented reference clock tree, 3 Xtal clocks each, plus jitter-cleaned LHC bunch clock multiple
  - Two processors XC7V690T (prototype XC7V485T)
  - Interlinked by 238-way LVDS path
  - 12-way (+) optical output to CTP
  - 32-way electrical (LVDS) output to CTP via mezzanine
- Full **ATCA** compliance / respective circuitry on mezzanine
- Module control via Kintex and Zynq processors
  - Initially via VMEbus extension
  - Eventually via Kintex or Zynq processor (Ethernet / base interface)

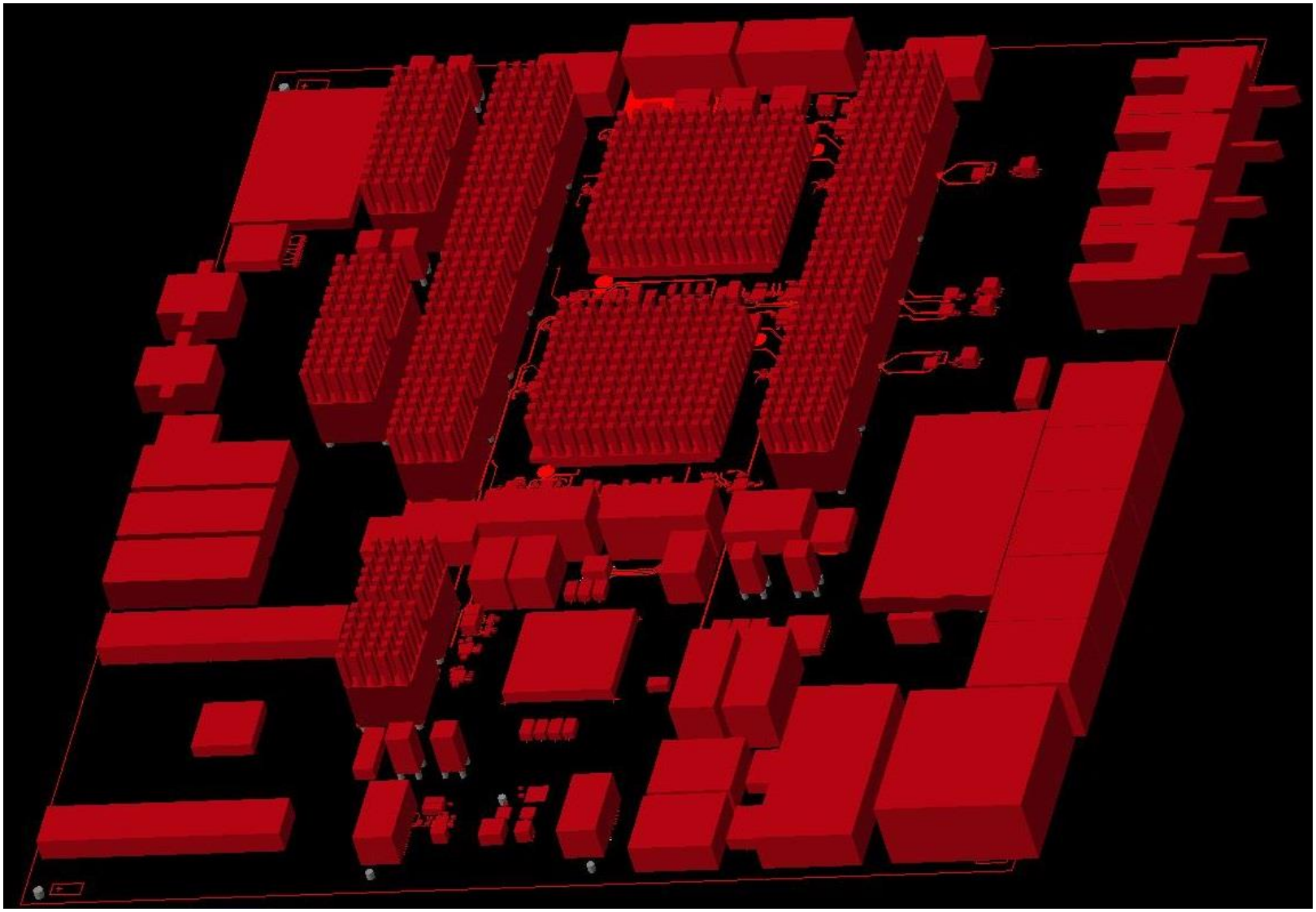


floor plan, so far…

- Processor FPGA configuration via SystemACE and through module controller
- Module controller configuration via SPI and SD-card
- DAQ and ROI interface
  - Two SFPs, L1Calo style
  - up to 12 opto fibres (miniPOD)
  - Hardware to support both L1Calo style ROD interface, and embedded ROD / S-Link interface on these fibres



… and in 3-d

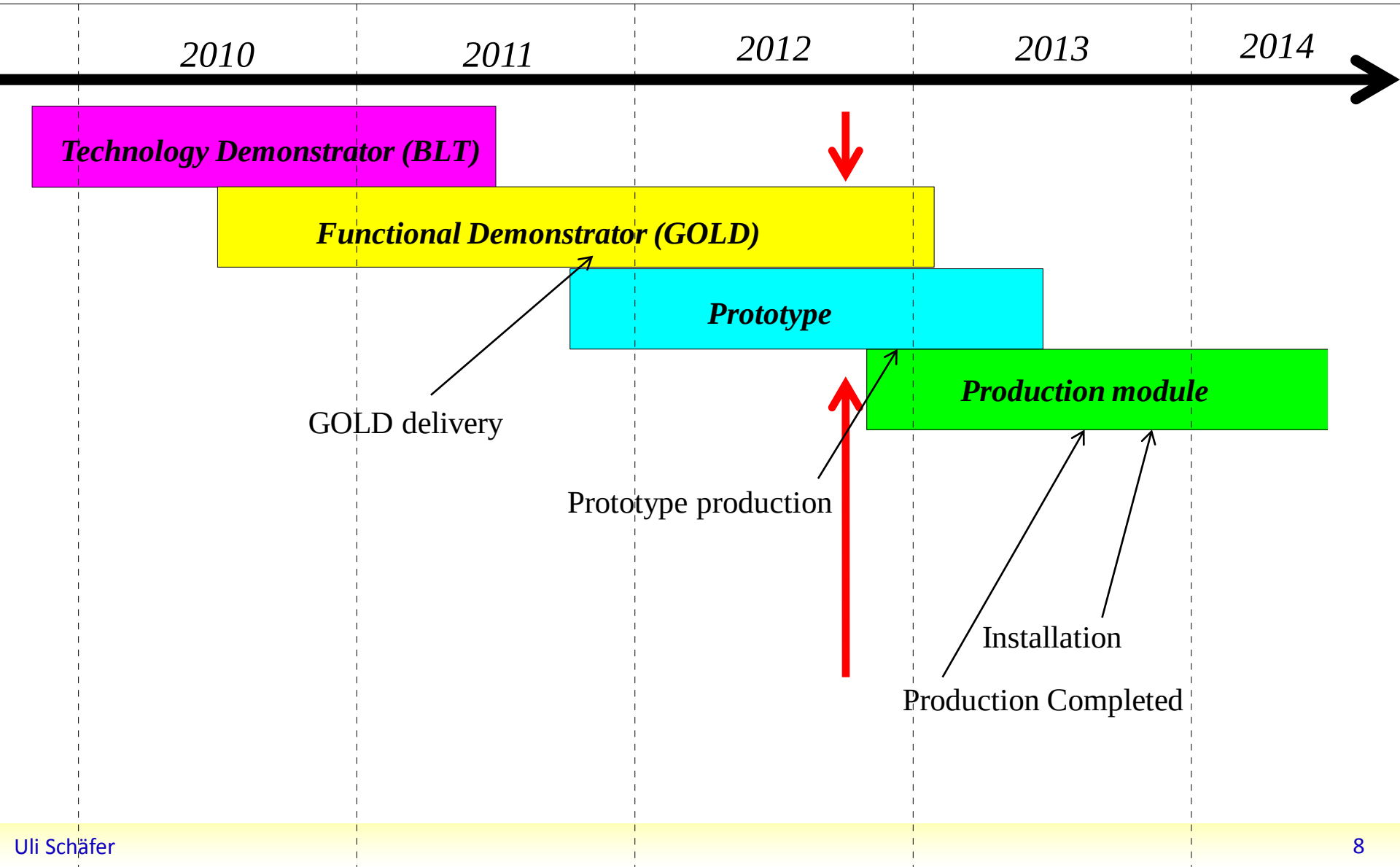


Hardware status

- Implemented recommendations from PDR
- Schematics near final
- Layout done to ~60%
- Bruno busy completing design
- Some ATCA and module control specific circuitry moved to mezzanine, to be finalized later
- Initial version of mezzanine design to be made as soon as L1Topo mainboard out for manufacture

→ Have follow-up to PDR end November

Topology Processor Schedule



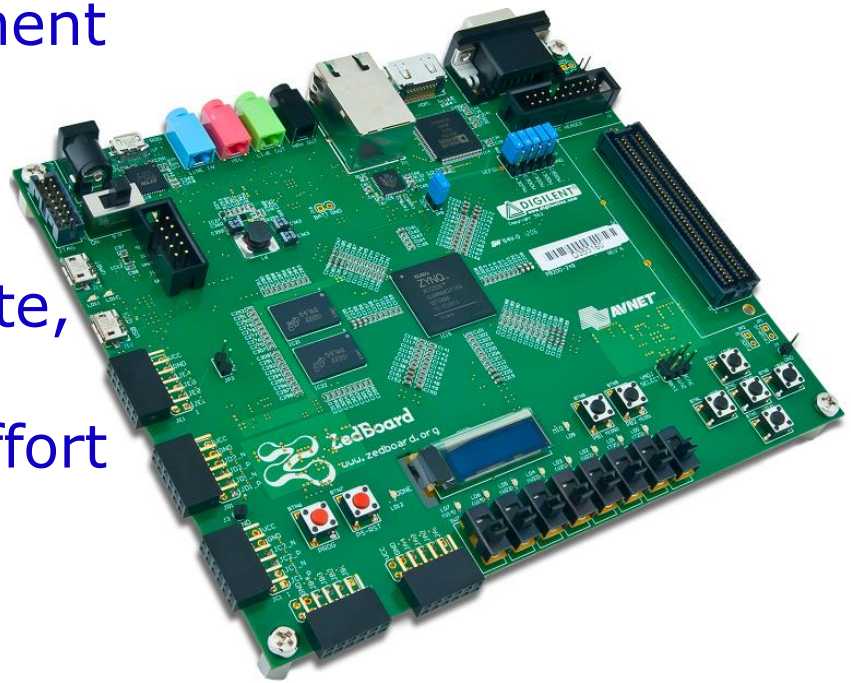
Current activities: module control

Sebastian working on register model (s/w)

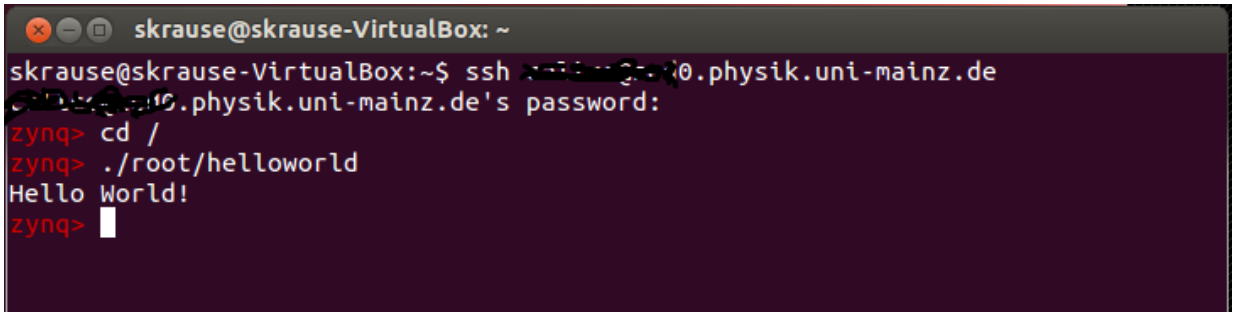
Andreas R. making the fibre-optical VME extension more robust (f/w)

Sascha K. started work on Zynq processor (FPGA fabric plus ARM processor)

- Device chosen for L1Topo (Mars ZX3) not yet available
- Currently using Zedboard to get acquainted to the processor and design environment
- Got system up with supplied software (Linux) and firmware images
- Got networking into usable state, wildly patching initrd image
- Major software development effort using cross compiler tool chain on Ubuntu (see next slide…)



Module control



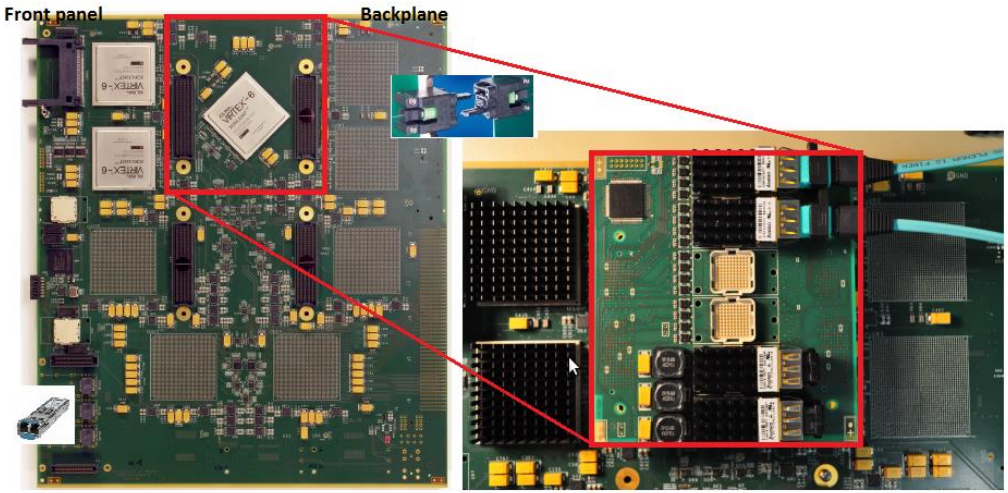
Almost done !

Now digging at hardware access

- Out of the box there is a GPIO interface implemented in the fabric, allowing for some lights to be flashed from Linux command line
- Build L1Topo specific hardware interface (VME-like register model ?) in firmware
- Attach the interface to the ARM core and write support software

→ need to get used to Xilinx EDK

Functional Demonstrator : “GOLD”

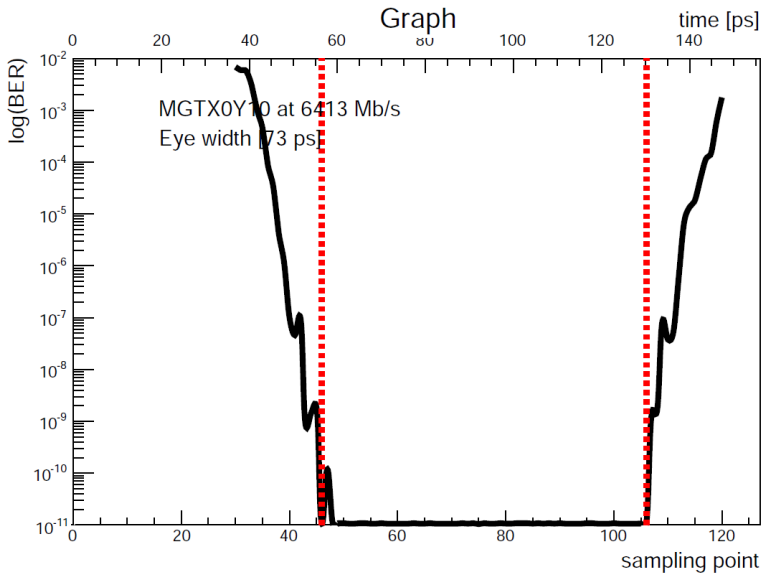


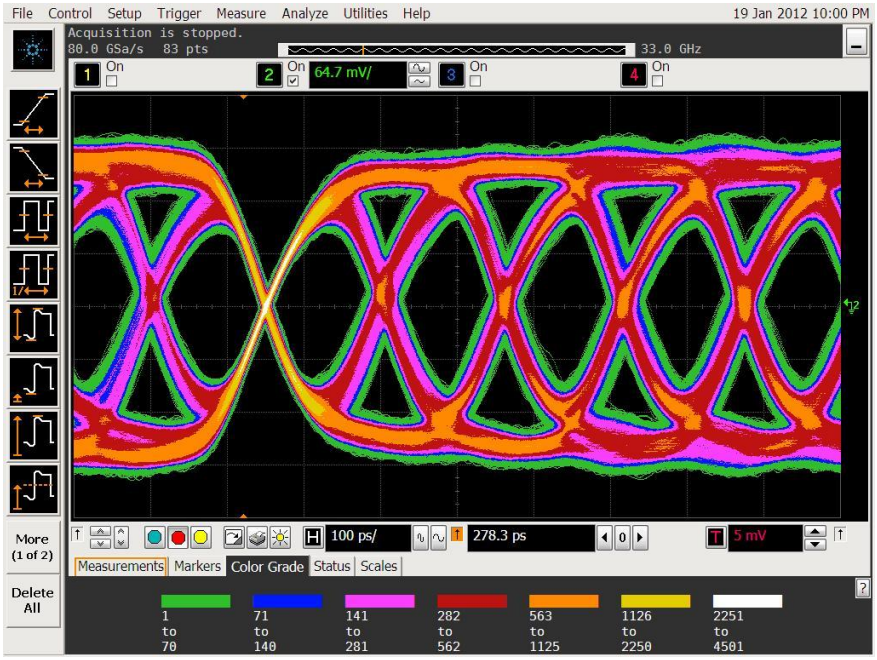
Try out technologies and schemes for L1Topo

- Fibre input from the backplane (MTP-CPI connectors)
- Up to 10Gb/s o/e data paths via industry standard converters on mezzanine
- Using mid range FPGAs (XC6VLX240T) up to 6.4Gb/s, 24 channels per device
- Typical sort/dφ algorithm (successfully implemented) takes ~ 13% logic resources
- Real-time output via opto links on the front panel (currently used as data source for latency measurements etc.)
- Will continue to be used as source/sink for L1Topo tests

Recent GOLD results (Virtex-6)

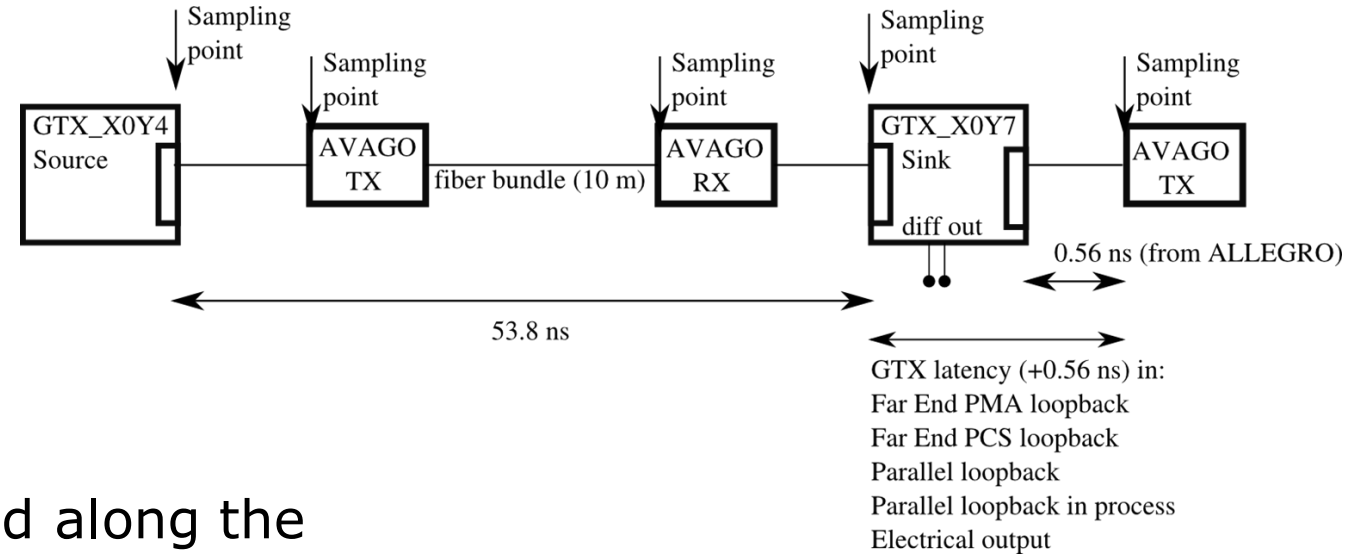
- Jitter analysis on cleaned TTC clock (σ = 2.9 ps)
- Signal integrity: sampled in several positions along the chain
- MGT and o/e converters settings optimization
- Bit Error Rate (BER) < 10^{-16} at 6.4 Gbps / 12 channels
- Eye widths above 60 ps (out of 156 ps)
- Crosstalk among channels measured in some cases but with negligible effect





Sampled after fan-out chip

GOLD latency (Virtex-6)



Latency measured along the
real-time path in various points
at 6.4 Gbs, 16 bit data width, and 8b/10b encoding

- Far End PMA loopback: 34 ns latency
- Electrical (LVDS) output: 63 ns latency
- Far End PCS loopback: 78 ns latency
- Parallel loopback in fabric: 86 ns latency

Firmware mod for latency measurement including algorithm, and electrical out towards CTP under way (Volker almost got there…)

Further firmware / tests…

- Some CPLD f/w for o/e converters, jitter cleaners, TTCRx control exists for GOLD, being adapted for L1Topo
- For initial Virtex-7 tests, VC707 eval board will be used (via SFP) and some firmware needs to be developed to that end
- Initial loopback test (single channel) already successful (half day, 0 errors)
- BER cores worked out of the box but there are bugs on the ChipScope analyser which prevent to run automatic parameters scans
- Since GOLD will continue to be used as source/sink module, some further f/w will be required for V6

Algorithms

- Weina updating dφ algorithm to most recent data format
- Stephan M. joined group and will work on algorithms
- Initially on highly parallel sort with largish number of output objects ?
- Expand dφ algorithm to clusters …
- Obviously need to move further code onto Virtex-7 asap (in particular for latency tests)

Try to move on to Vivado as soon as it gets stable, and as more effort goes into V7 firmware

L1Topo : Milestones

Specifications for prototype under way:

- 30.05.2012 PDR
- End November prototype layout finished
- End November follow-up to PDR
- 20.02.2013 production/assembly completed

Start preparations for final module production in parallel with prototype module tests. Make prototype module available for initial tests / commissioning @ P1

- 06/2013 prototype tests finished
- 06/2013 PRR
- 09/2013 production finished
- 12/2013 start commissioning at P1
- 08/2014 commissioning finished

Summary

L1Topo functional demonstrator (GOLD):

- High-speed o/e data paths successfully tested
- MGT Parameters tuned at 6.4 Gb/s for large bit-error free windows
- Latency measurements taken, activity on-going

L1Topo Prototype:

- Design ready, reviewed, schematic capture almost finished
- Modifications due to review incorporated
- Layout well advanced
- Some not yet finalised circuitry to go onto mezzanine module
- PDR follow-up in November
- Considerable effort going into s/w, f/w, system-level integration
- On schedule for installation during shutdown 13/14