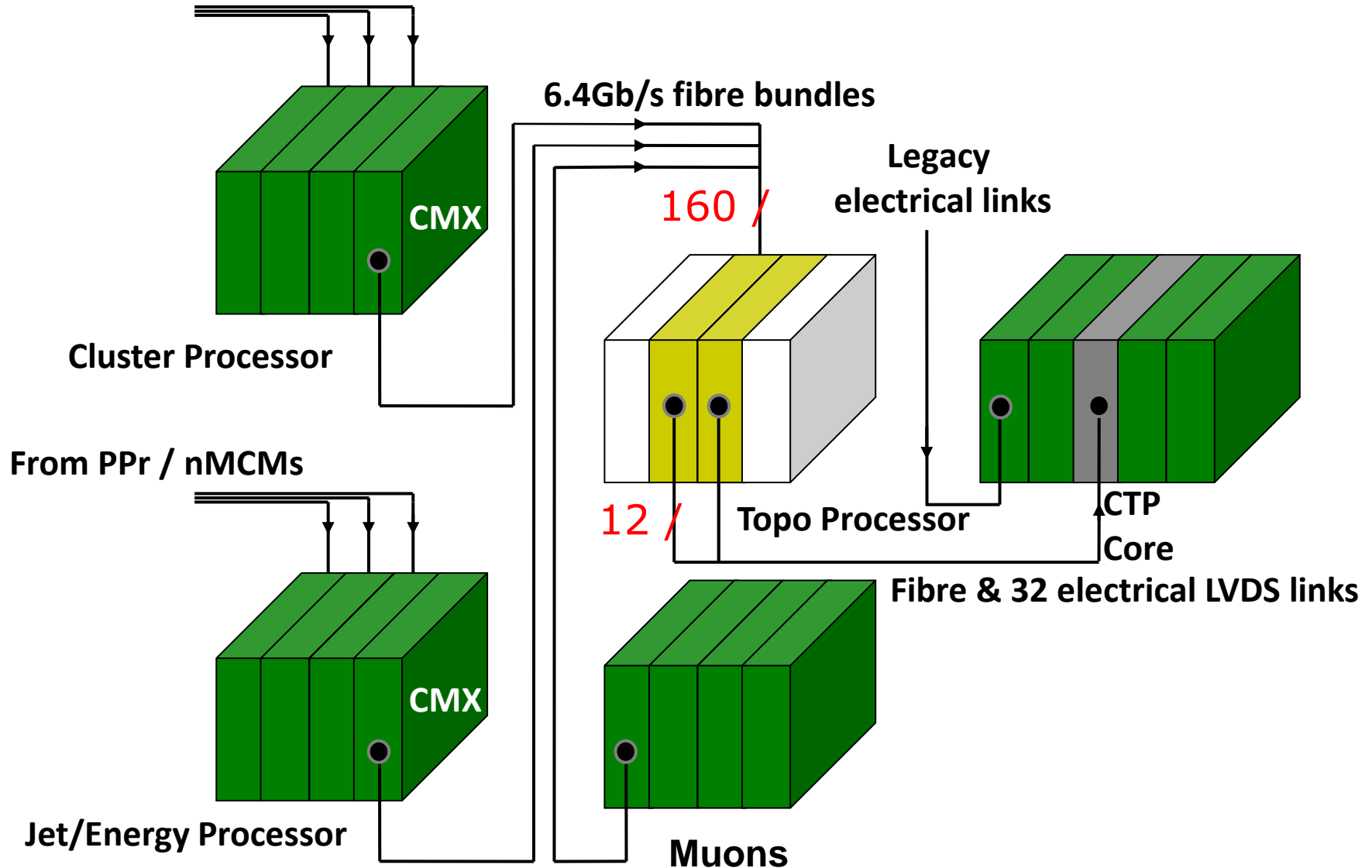# L1Topo Status & Plans

B.Bauß, V.Büscher, W.Ji, S.Krause, S.Moritz,
U.Schäfer, A.Reiß, E.Simioni, S.Tapprogge, V.Wenzel

- Topo system
- Topo processor, post-PDR
- Current activities
  - Some results from Gold
  - Targeting V7
  - Zynq
  - Service firmware
  - Algorithmic firmware
- Hardware status
- Timeline
- Summary

Topology 2013/14 (RTDP)

6.4Gb/s fibre bundles

CMX

Cluster Processor

From PPr / nMCMs

CMX

Jet/Energy Processor

160 /

12 /

Topo Processor

Legacy electrical links

CTP Core

**Fibre & 32 electrical LVDS links**

Muons

Topology Processor

To provide a maximum of flexibility for applying topological trigger criteria:

- Maximise aggregate input bandwidth without compromising on on-board RTDP bandwidth
  - Two high-end processors
  - 820 Gb/s @ 6.4Gb/s (2014 baseline rate)
  - Jets, clusters, Muons into single module
  - Allow to correlate all trigger object types within full solid angle
- Option to run separate algorithms on more than one topology module in parallel
- High density 12-channel opto transceivers (miniPODs)
- Fibre bundles from L1Calo CMXes and Muons
- Both fibre bundle and low latency LVDS into CTPcore
- Some critical circuitry on mezzanine, to allow for later mods
- Make use of data duplication at source, if required

- Well prepared for phase 1:
  - accept line rates above 6.4Gb/s from future processors (FEXes, muons)
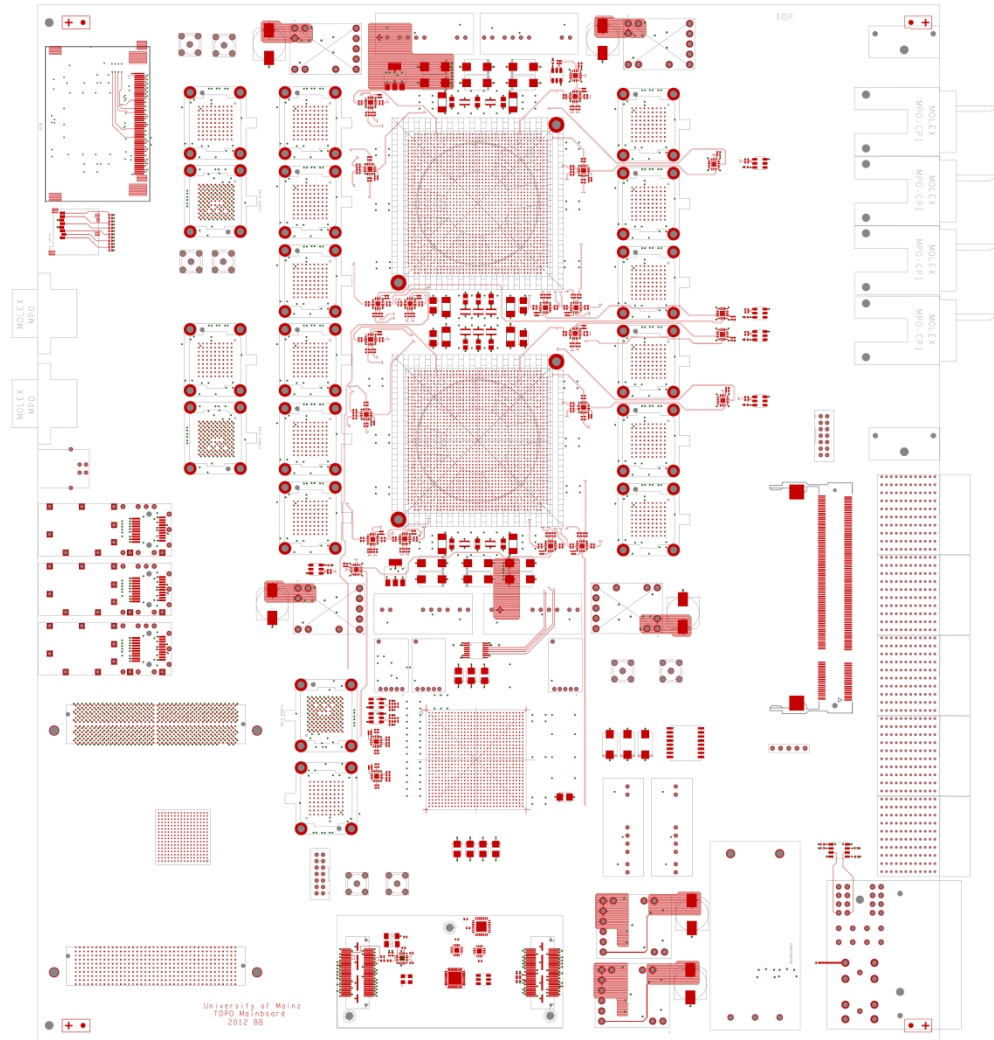 - Employ zero suppression

Topo processor details – post PDR

- Real-time path:
  - 14 fibre-optical 12-way inputs (miniPOD)
  - Via four 48-way backplane connectors
  - 4-fold segmented reference clock tree, 3 Xtal clocks each, plus jitter-cleaned LHC bunch clock multiple
  - Two processors XC7V690T (prototype XC7V485T)
  - Interlinked by 238-way LVDS path
  - 12-way (+) optical output to CTP
  - 32-way electrical (LVDS) output to CTP via mezzanine
- Full **ATCA** compliance / respective circuitry on mezzanine
- Module control via Kintex and Zynq processors
  - Initially via VMEbus extension
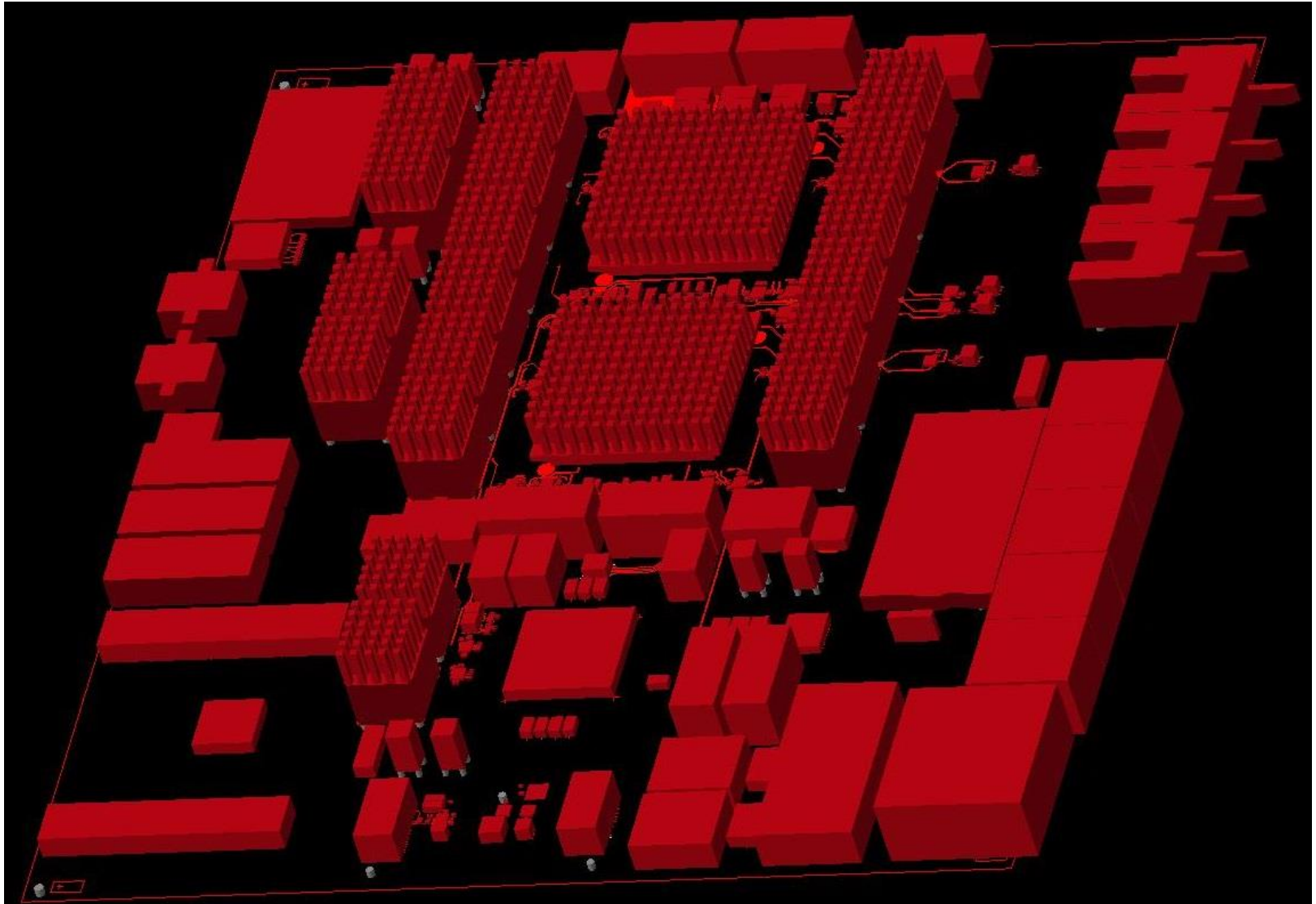 - Eventually via Kintex or Zynq processor (Ethernet / base interface)
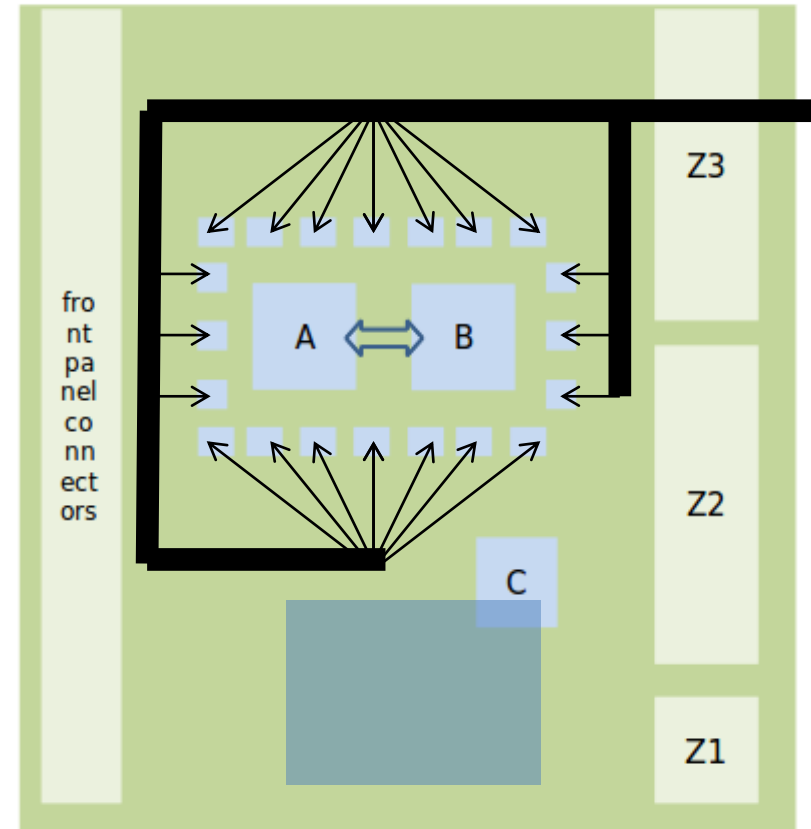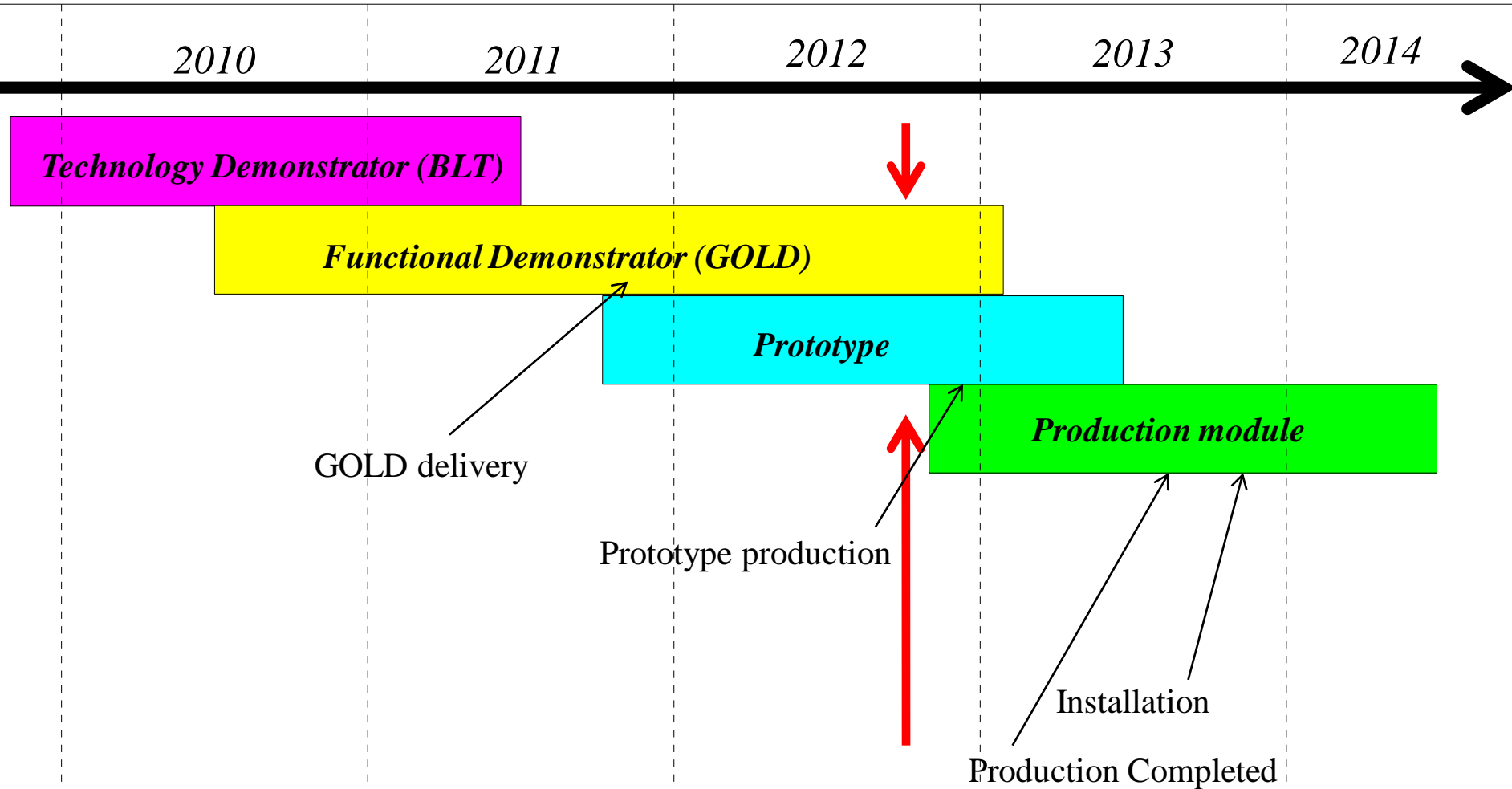
floor plan, so far…

- Processor FPGA configuration via SystemACE and through module controller

- Module controller configuration via SPI and SD-card

- DAQ and ROI interface
  - Two SFPs, L1Calo style
  - up to 12 opto fibres (miniPOD)
  - Hardware to support both L1Calo style ROD interface, and embedded ROD / S-Link interface on these fibres

… and in 3-d

Topology Processor Schedule

2010   2011   2012   2013   2014

Technology Demonstrator (BLT)

Functional Demonstrator (GOLD)

Prototype

Production module

GOLD delivery

Prototype production

Installation

Production Completed

Current activities: module control

Sebastian working on register model (s/w)

Andreas making the fibre-optical VME extension more robust (f/w)

Sascha started work on Zynq processor (FPGA fabric plus ARM processor)

- Device chosen for L1Topo (Mars ZX3) not yet available
- Currently using Zedboard to get acquainted to the processor and design environment
- Got system up with supplied software (Linux) and firmware images
- Got networking into usable state, wildly patching initrd image
- Major software development effort using cross compiler tool chain on Ubuntu (see next slide…)
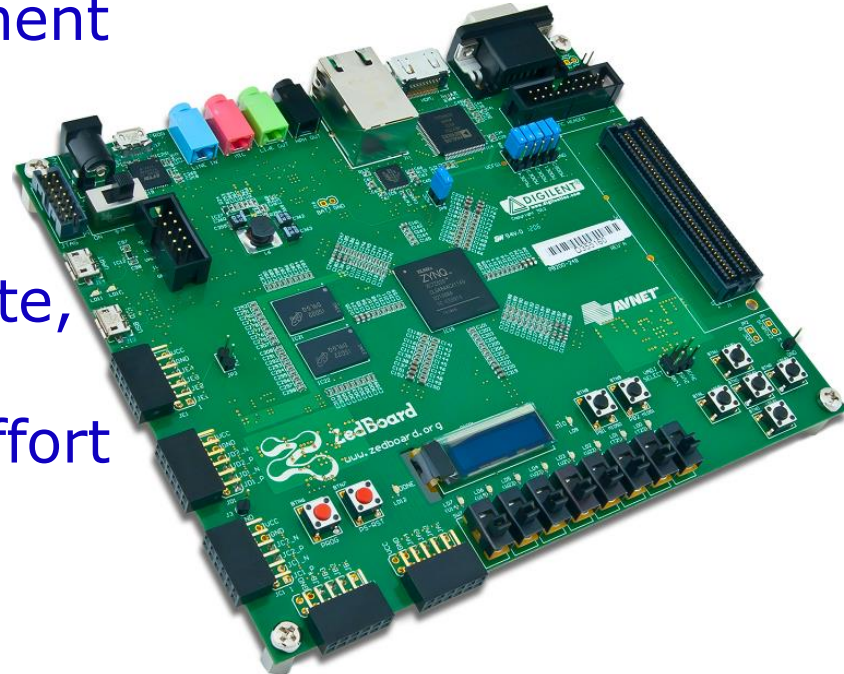
Module control

Almost done !

Now digging at hardware access

- Out of the box there is a GPIO interface implemented in the fabric, allowing for some lights to be flashed from Linux command line

- Build L1Topo specific hardware interface (VME-like register model ?) in firmware

- Attach the interface to the ARM core and write support software

→ need to get used to Xilinx EDK

Functional Demonstrator : "GOLD"
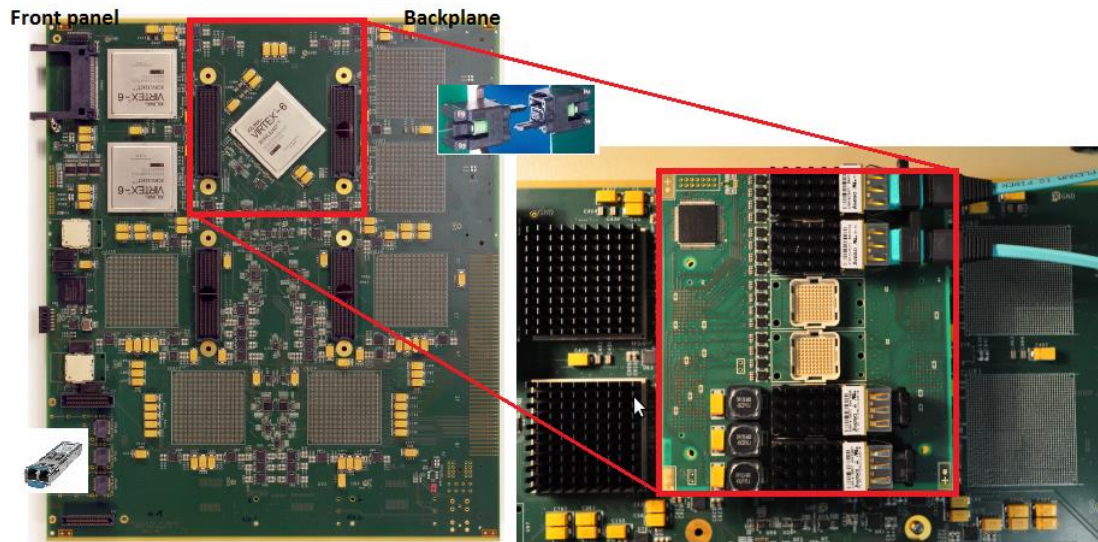
Try out technologies and schemes for L1Topo

- Fibre input from the backplane (MTP-CPI connectors)
- Up to 10Gb/s o/e data paths via industry standard converters on mezzanine
- Using mid range FPGAs (XC6VLX240T) up to 6.4Gb/s, 24 channels per device
- Typical sort/dφ algo takes ~ 13% logic resources
- Real-time output via opto links on the front panel

Recent GOLD results (Virtex-6)

- Jitter analysis on cleaned TTC clock (σ = 2.9 ps)
- Signal integrity: sampled in several positions along the chain
- MGT and o/e converters settings optimization
- Bit Error Rate (BER) < 10^{-16} at 6.4 Gbps / 12 channels
- Eye widths above 60 ps (out of 156 ps)
- Crosstalk among channels measured in some cases but with negligible effect
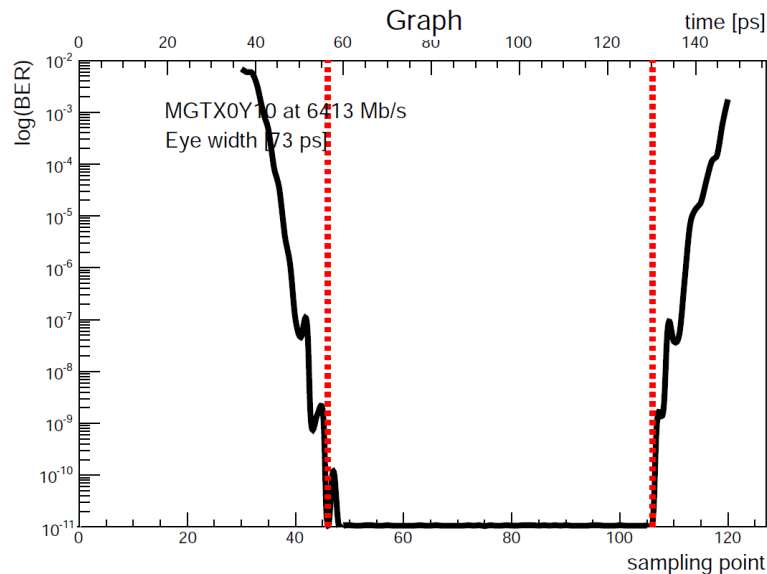
Sampled after fan-out chip

GOLD latency (Virtex-6)
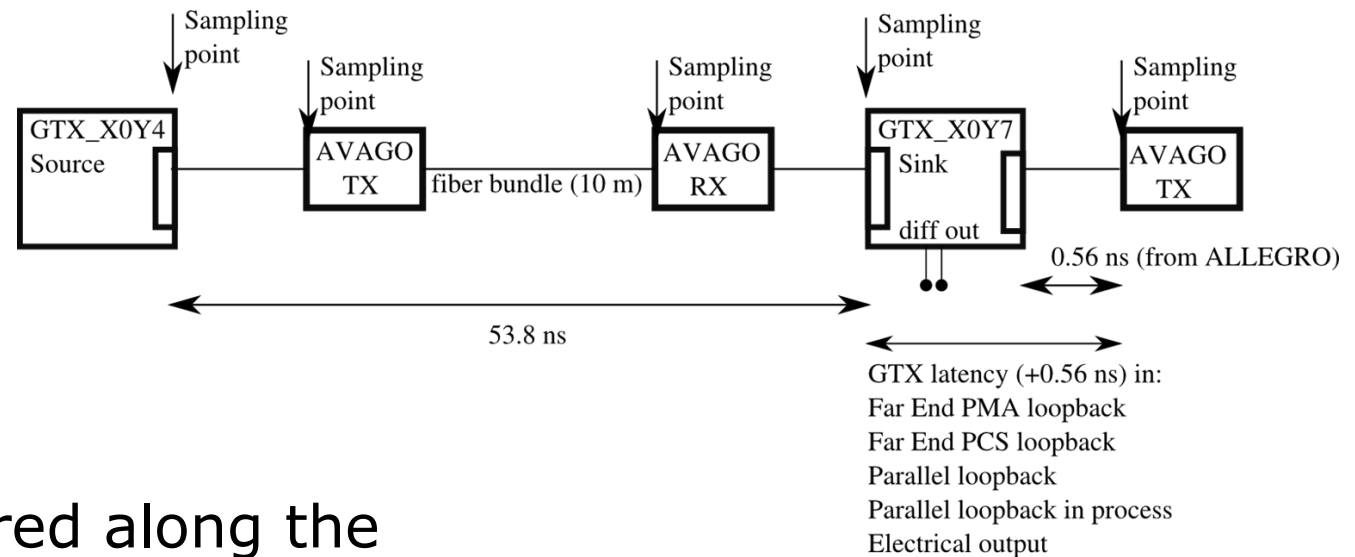
Latency measured along the
real-time path in various points
at 6.4 Gbs, 16 bit data width, and 8/10 bit encoding

- Far End PMA loopback: 34 ns latency
- Electrical (LVDS) output: 63 ns latency
- Far End PCS loopback: 78 ns latency
- Parallel loopback in fabric: 86 ns latency

GOLD TESTS (Virtex-7)

- We are experiencing with Virtex7-VC707 evaluation board using the GOLD as a source

- BER cores worked out of the box but there are bugs on the ChipScope Analizer which prevent to run automatic parameters scans

- 4 channels pulled to 10 Gbs with a not optimized setting and no errors measured in a short data acquisition of half day

- Repeating the Latency measurement on Virtex-7

Service FW

- CPLD FW for o/e converters, jitter cleaners, TTCRx

- GOLD will used as a source/sink for testing purposes

- Feed the VC-707 via SFP with defined data vectors (for V7 latency measurements)

- Feed the sorting algorithm programmed in one input GOLD FPGA. Only 12 channels are feed due to HW limitations

- In the future the GOLD will feed the TP prototype in a similar way

- Improving the communication firmware among the VME extension (BLT module) to the GOLD via SFP fiber

Summary

L1Topo functional demonstrator (GOLD):

- High-speed o/e data paths successfully tested
- MGT Parameters tuned at 6.4 Gb/s for large bit-error free windows
- Latency measurements taken, activity on-going

L1Topo Prototype:

- Design ready, reviewed, schematic capture almost finished
- Modifications due to review incorporated
- Layout well advanced
- Some not yet finalised circuitry to go onto mezzanine module
- PDR follow-up in November
- Considerable effort going into s/w, f/w, system-level integration
- On schedule for installation during shutdown 13/14

-

- Latency measurements done in several configurations at 6.4 Gbs

- (16 bit data width and 8/10 bit encoding)

- Far End PMA loopback: 34 ns latency

- Electrical output: 63 ns latency

- Far End PCS loopback: 78 ns latency

- Parallel loopback in fabric: 86 ns latency

L1Topo : Milestones

Changes in red

Specifications for prototype under way:

- 30.05.2012 PDR
- 29.09.2012 end november prototype layout finished
- End november follow-up to PDR
- 20.02.2012 production/assembly completed

Start preparations for final module production in parallel with prototype module tests. Make prototype module available for initial tests / commissioning @ P1

- 05/2013 prototype tests finished
- 05/2013 PRR
- 08/2013 production finished
- 11/2013 start commissioning at P1
- 07/2014 commissioning finished