jFEX

Mainz

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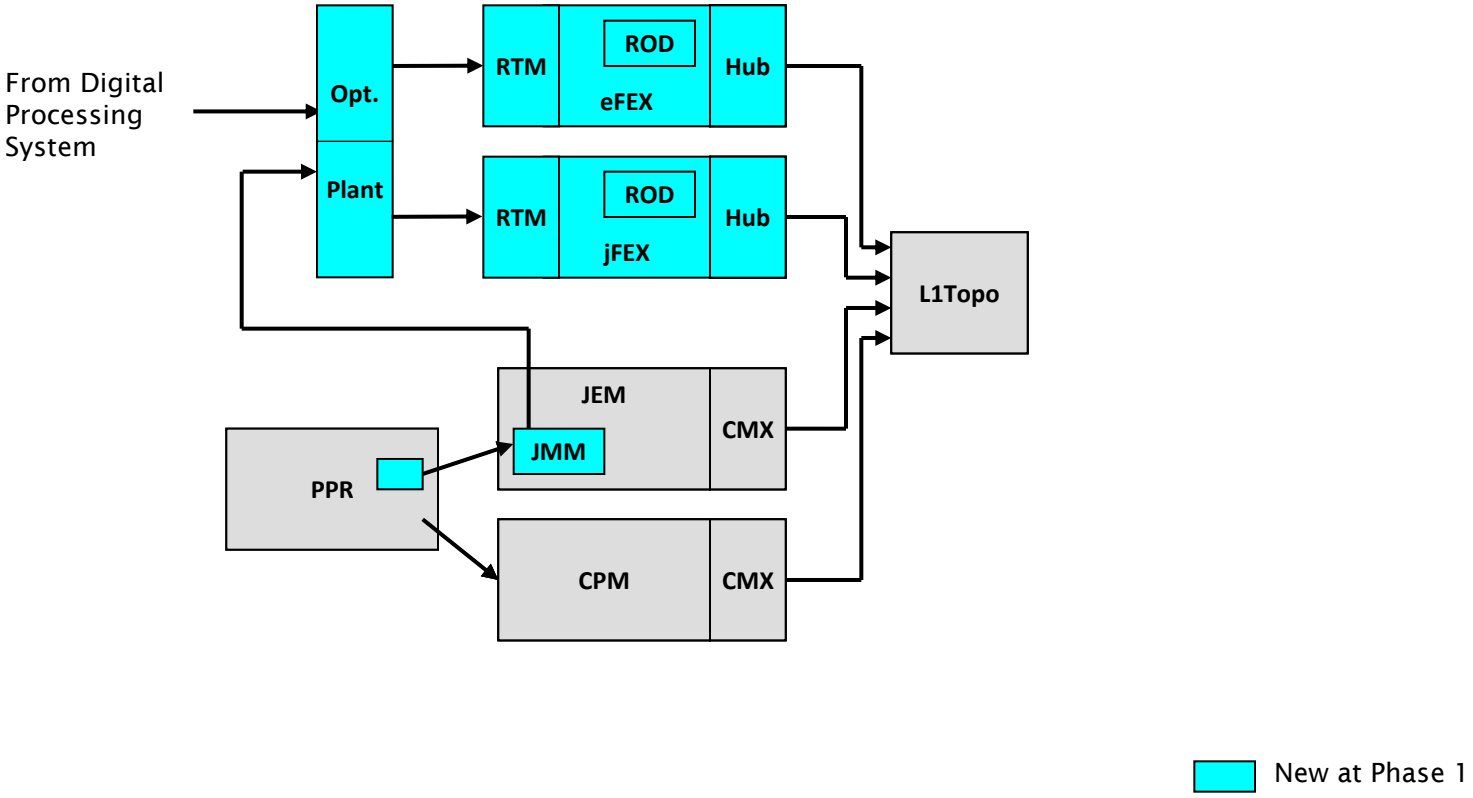
L1Calo Phase-1 System



Data replication

Sliding window algorithm requiring large scale replication of data

- Avoid data re-transmission (latency !)
- → Forward duplication only (fan-out)
- Baseline: no replication of any source into more than two sinks
- Fan-out in eta handled at source only (DPS)
  - Duplication at the parallel end (on-FPGA), using additional Multi-Gigabit Transceivers
  - Allowing for differently composed streams
  - Minimizing latency
- Fan-out in phi handled at destination only
  - "far end PMA loopback" (well, not quite a re-transmission, but…)
  - Alternatively consider passive electrical splitting of multi-Gbps signals
  - Active signal fan-out would compromise design density

jFEX system

ATCA shelf / blades:

- Sharing infrastructure with eFEX
  - Handling / splitting of fibre bundles
  - ROD design
  - Hub design
- Need to handle both high granularity and large jet environment
  → Require high density / high bandwidth per module
- Single crate
- ~ 8 modules (+FCAL ?)

Input signals:

- Granularity .1×.1 (η×φ)
- One electromagnetic, one hadronic tower
- Cannot pre-sum e/h towers before duplication for reason of latency
- Unlike eFEX, no "BCMUX" scheme due to consecutive non-zero data
- 6.4 Gb/s line rate, 8b/10b encoding, → 128 bit per BC
- For now, assume 16bit per tower, 8 towers per fibre

Initial baseline

8+ Modules, each covering full phi, limited eta range

- Environment of 0.9 in eta (core bin +/- 4 neighbours)
- Each module receives fully duplicated data in eta : 1.6 eta worth of data required for a core of 0.8
- 16 eta bins including environment

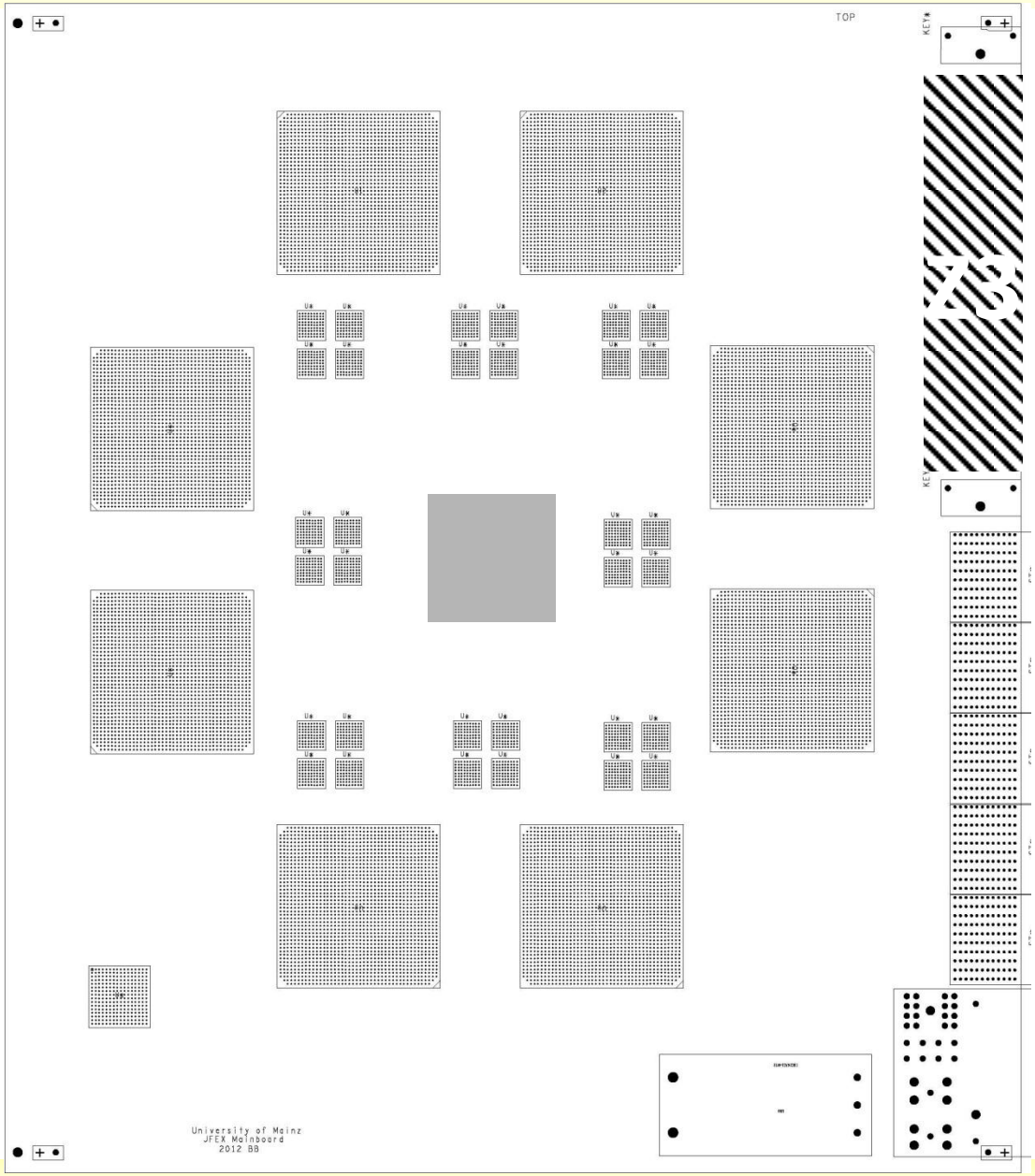
8 FPGAs per module

- Environment 0.9×0.9
- Each FPGA receives fully duplicated data in eta and phi: 1.6×1.6 worth of data required for a core of 0.8×0.8
- 256 bins @ 0.1×0.1 in η×φ, e/m + had → 512 numbers, 64 Multi-Gb/s receivers

→ 512 Multi-Gb/s receivers per module

How to fit on a module ?

- ATCA
- 8 processors (~XC7VX690T)
- ≤ 4 microPODs each
- fan-out passive or "far end PMA loopback"
- Small amount of control logic / non-realtime (ROD)
- Might add 9th processor for consolidation of results
- Electrical backplane basically unused
- Opto connectors in Zone 3



fibre count / density

- Due to full duplication in phi direction, exactly half of all 512 signals are routed into the modules optically on fibres
  - 256 fibres
  - 22 × 12-channel opto receivers
  - 4 × 72-way fibre bundles / MTP connectors
- For larger jets window we would require larger FPGAs, some more fibres and replication factor > ×2
- Horrible ?
  - Reduce number of bits per tower: at 11 bit/tower (11 towers per fibre) it is 186 fibres / 16 microPODs / 4*48-way MTP
  - Aim at higher line rates (currently FPGAs support 13 Gb/s, microPOD 10 Gb/s)
    - Allow for even finer granularity / larger jets / smaller FPGA devices :
    - If digital processor baseline allows for full duplication of 6.4Gb/s signals, the spare capacity, when run at higher rate, can be used to achieve a replication of more than 2-fold, so as to support a larger jet environment.

conclusion

- The 8-module jFEX seems possible with ~2013's technology
- Allows for both rather good granularity and large environment at 6.4Gb/s line rate
- Rather dense circuitry
- For finer granularity and / or larger jets things get even more complicated and we need to explore higher data rates
- DPS needs to handle the required duplication (in eta)

→ Start to work on detailed specifications soon,
in parallel explore higher data rates…